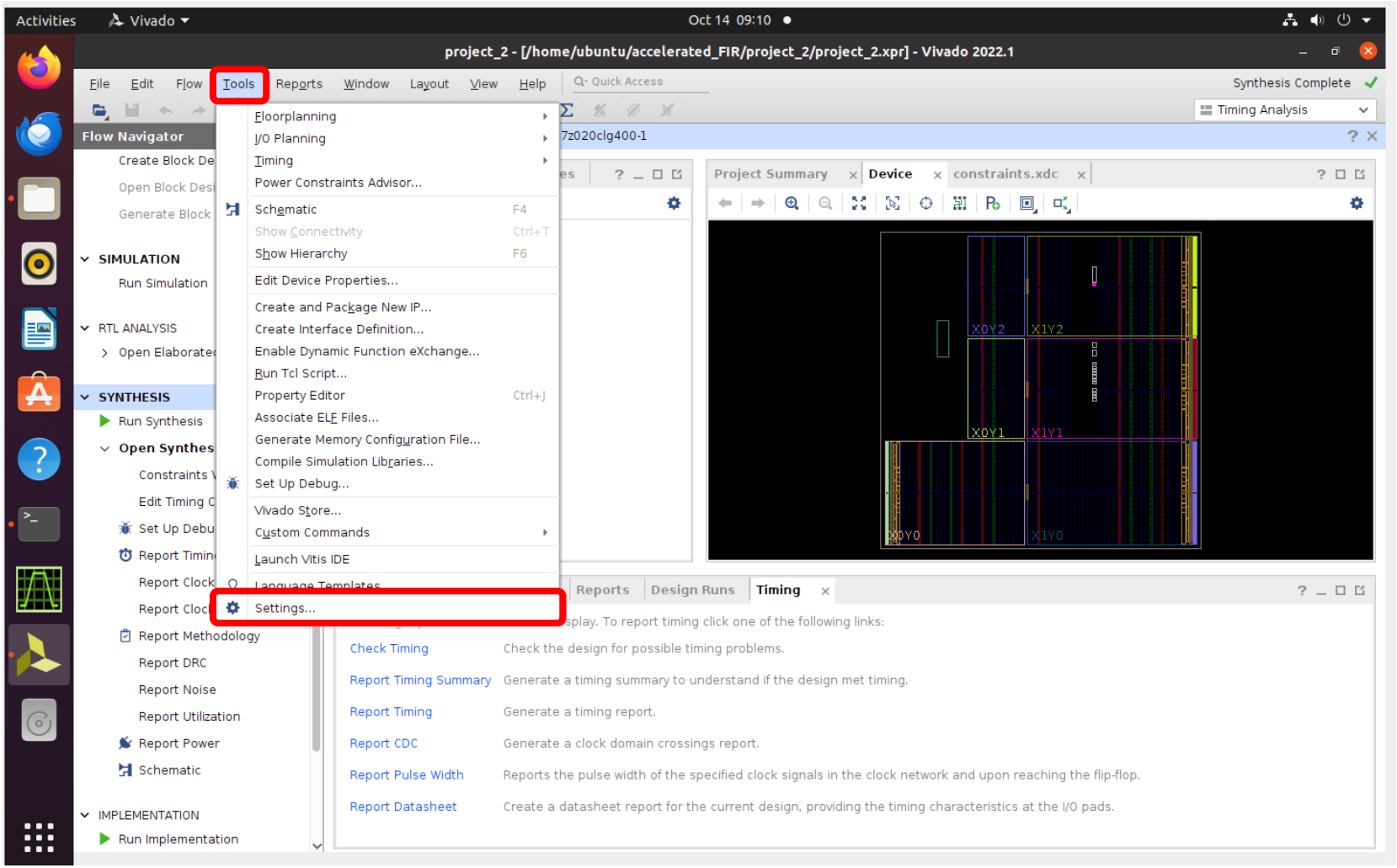
Synthesis Guide

SOC Design

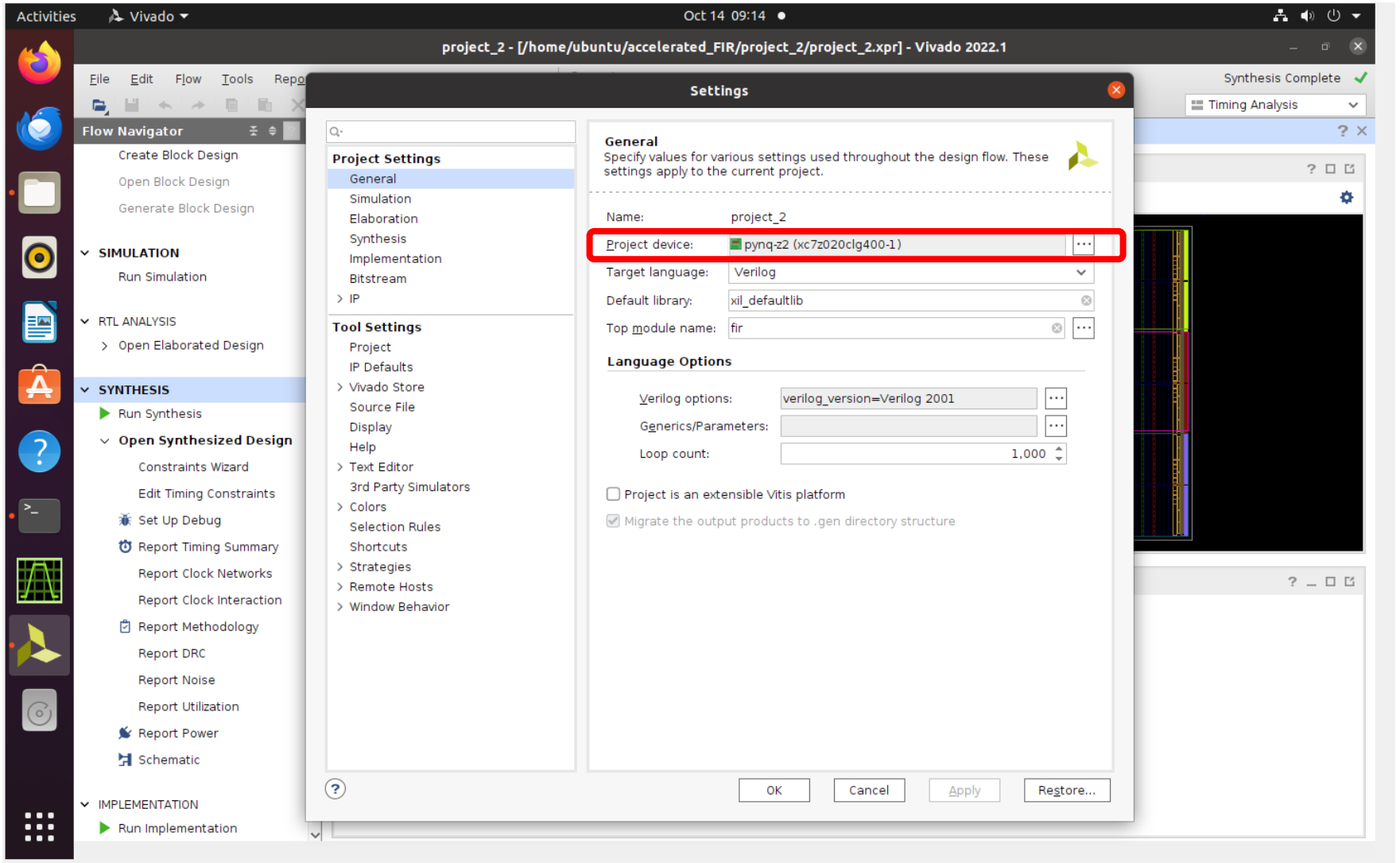
Synthesis Guide

- **We synthesis under【 Vivado GUI 】**
- You need to select the FPGA for Synthesis
  - Follow up the SIM_Workflow to select FPGA Board
  - Edit FPGA Board in the project

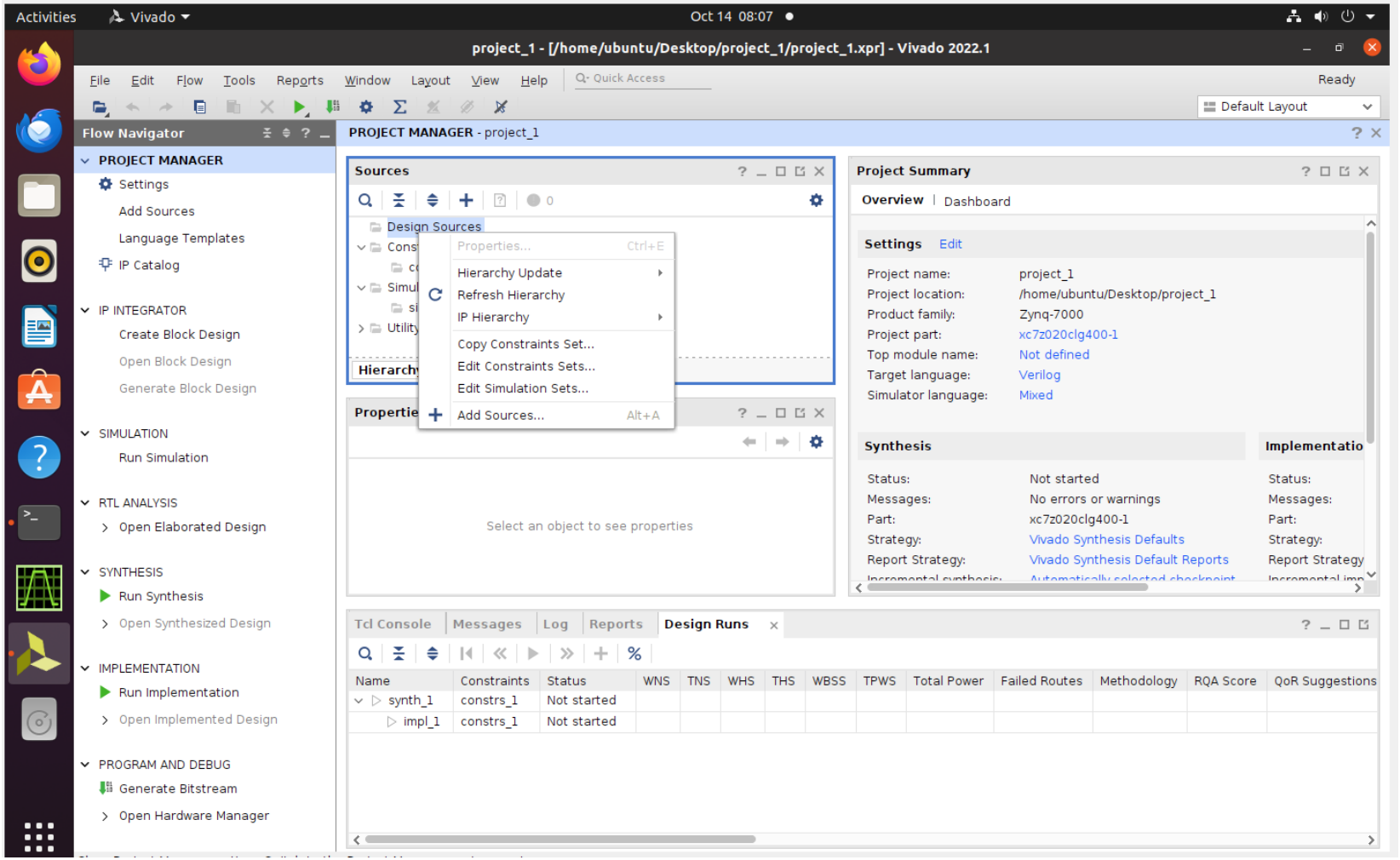
- **0. Select FPGA board**
- **0.1. 左鍵點擊 Tools，並且點擊Settings**



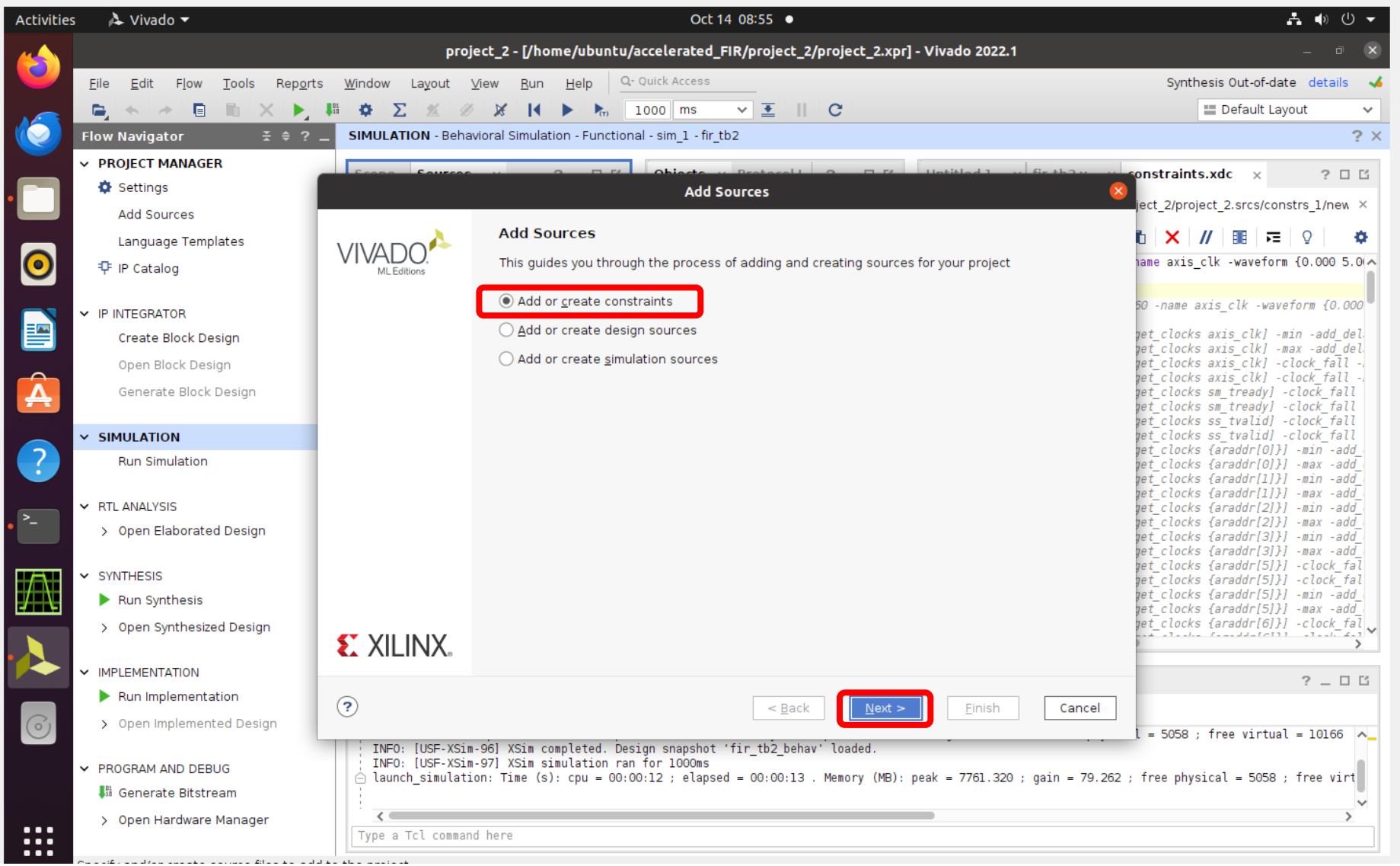
- **0.2. Modify Project Device**
  - **Select PYNQ-Z2 (xc7z020clg400-1)**



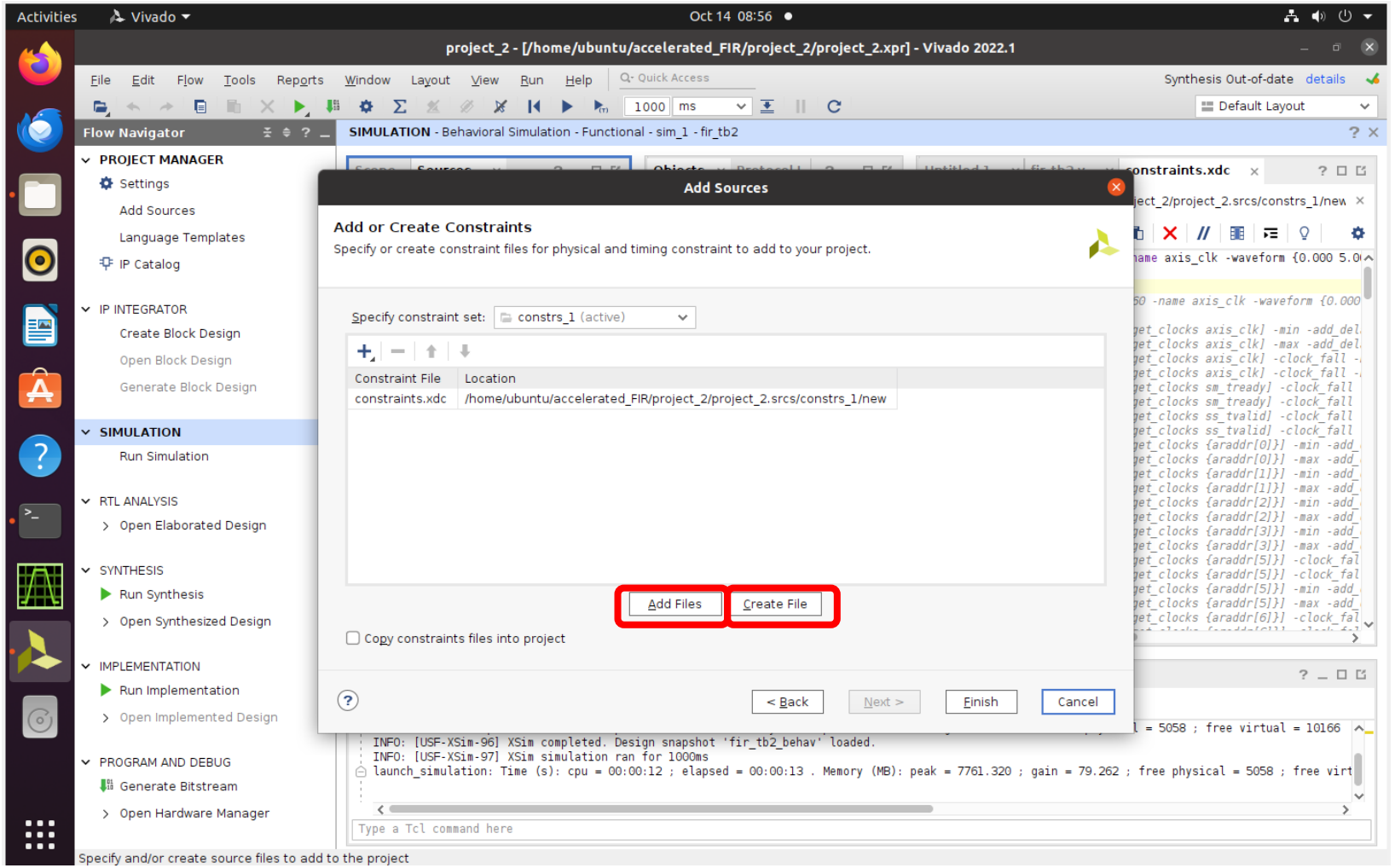
- **1.1 Add Constraints**
- **1.1.1 Add Sources**
  - **【右鍵點擊Design Sources，選擇Add Sources 】**



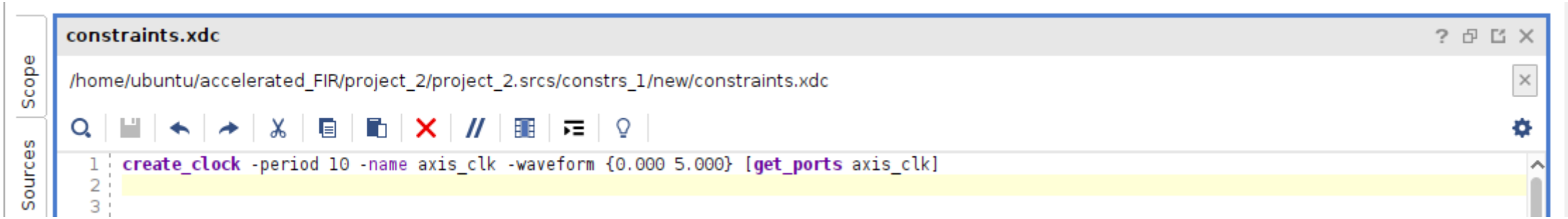
- **1.1.2 Add or Create constraints**
  - **【選取Add or Create constraints】**



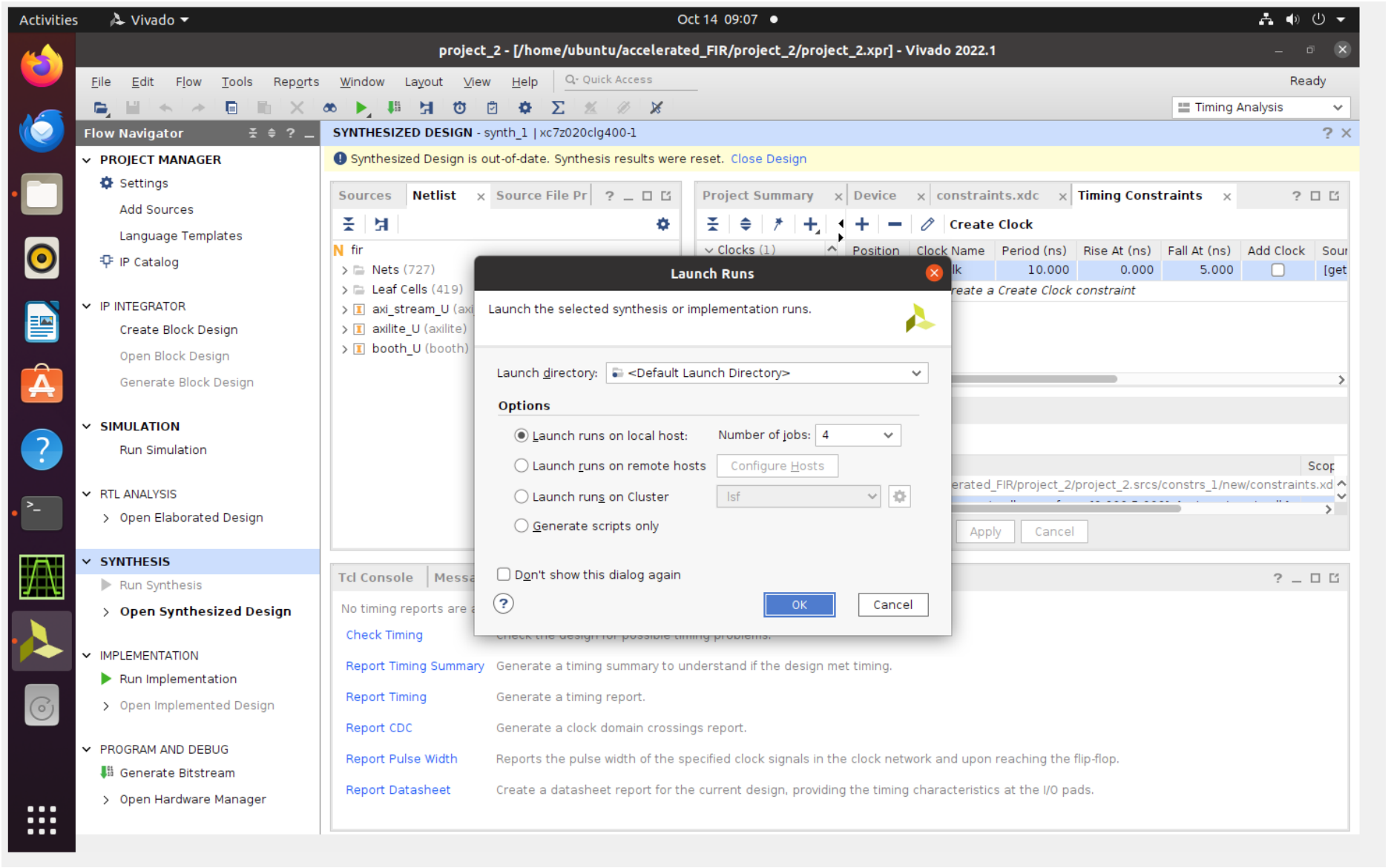
- **1.1.3 Add Files**
  - 【如果已有Constraints，選取Add files】
  - 【如果沒有Constraints，選取Create file】



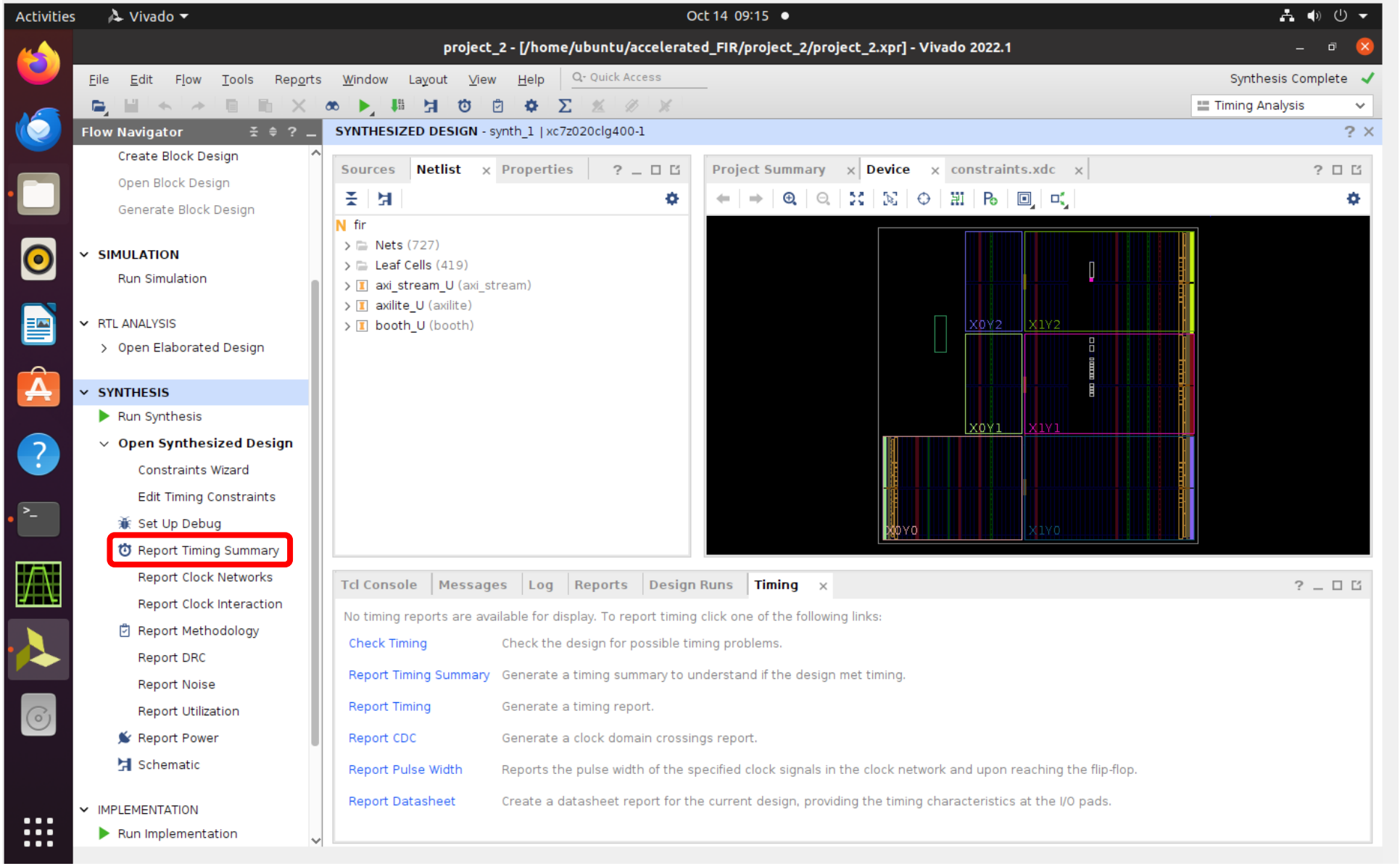
- **1.2 Modify Clock Constraints**
  - **1.2.1 設定Clock 的Constraints**
  - **create_clock –period period_time –name axis_clk –waveform {Rise_time Fall_time} [get_ports axis_clk]**



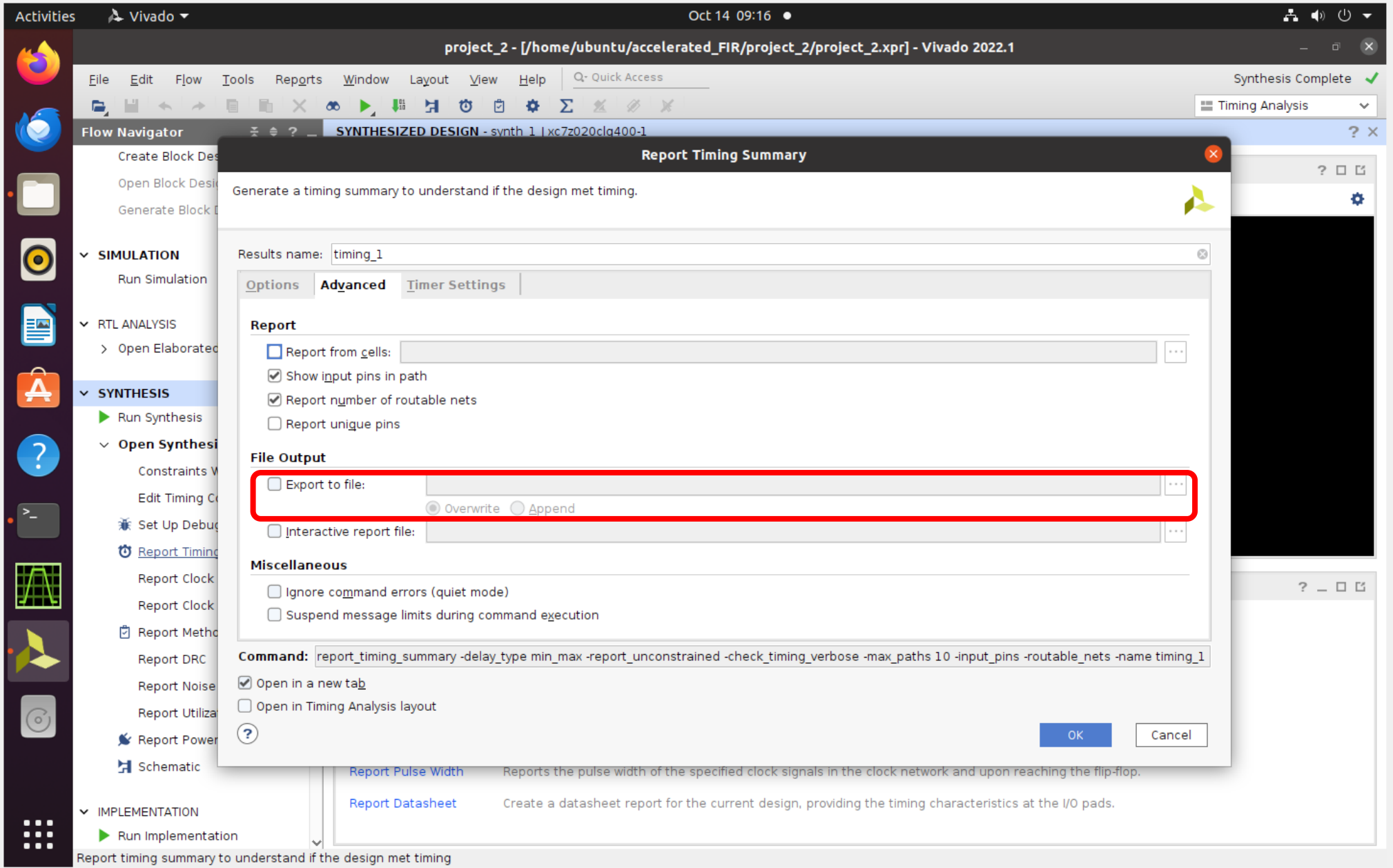
• 1.2.2 Run Synthesis



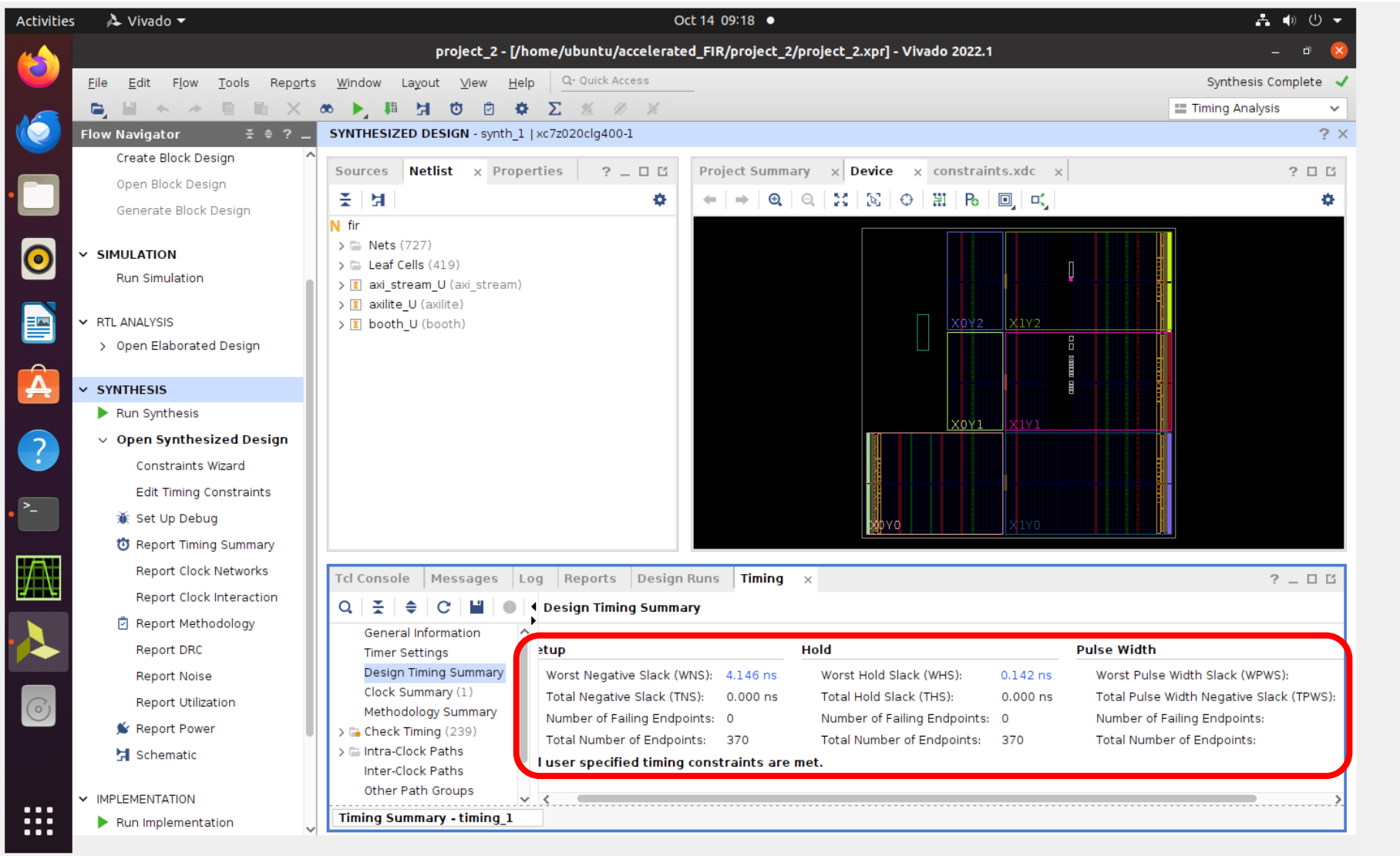
• 1.2.3 Report Timing Summary



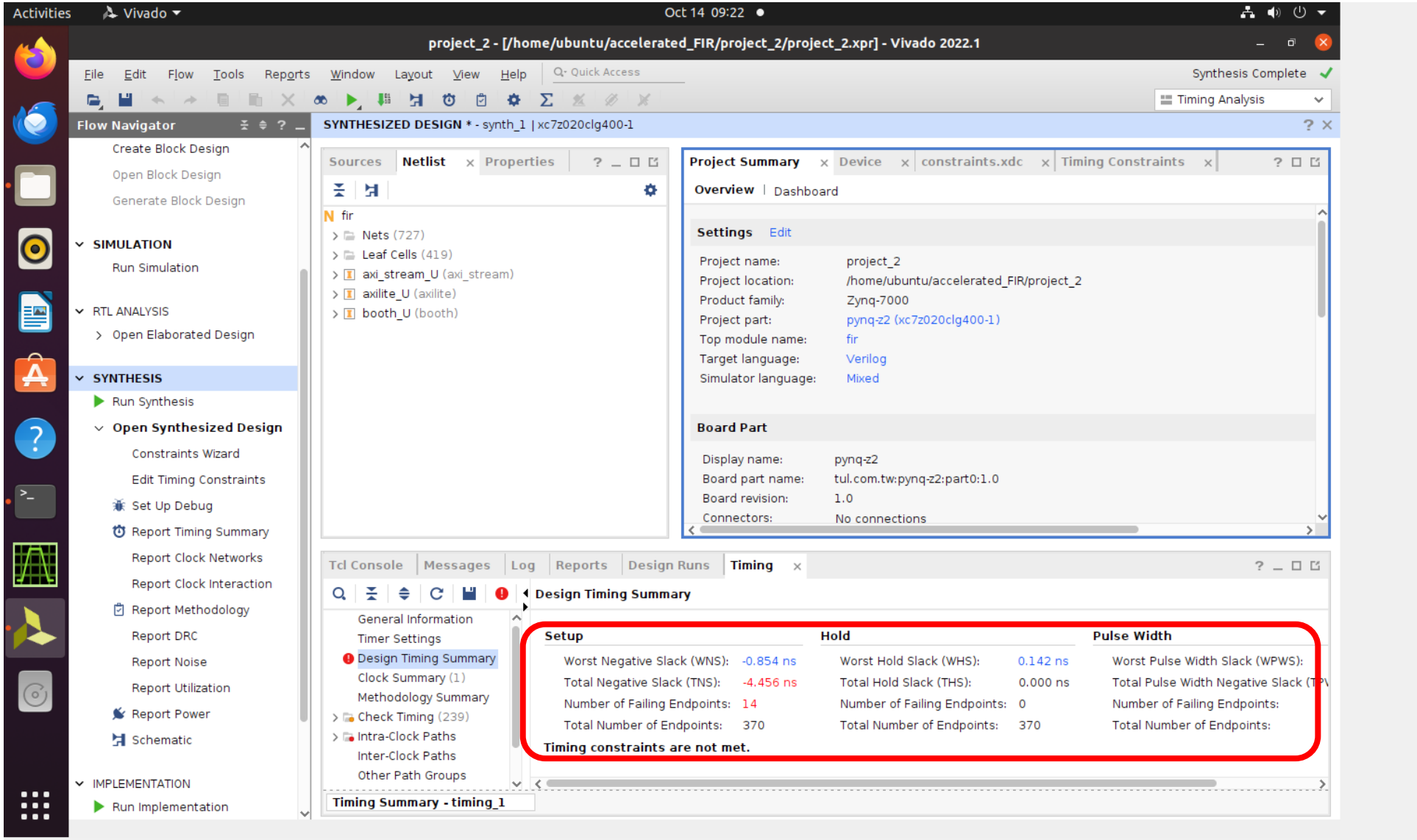
- **Export to timing summary file**



- **1.2.4 Check the Design Timing Summary**
  - **Slack time has to be positive integer**



- # 1.2.5 Edit Timing Constraints
  - ## If there is negative slack time, you need to increase timing constraints



- **Edit the axis_clk constraints, then re-run the timing summary.**