# SoC Design Lab1

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- Brief introduction about the overall system
  - Learn the hls flow
  - Learn how to integrate the IP from vitis_hls to zynq
  - Learn how to generate bitstream on vivado
  - Learn how to rent the onlineFPGA
  - Learn how the kv260 read the bitstream by library of overlay
  - Learn how to write code on OnlineFPGA by Jupyter

- **What is observed & learned**

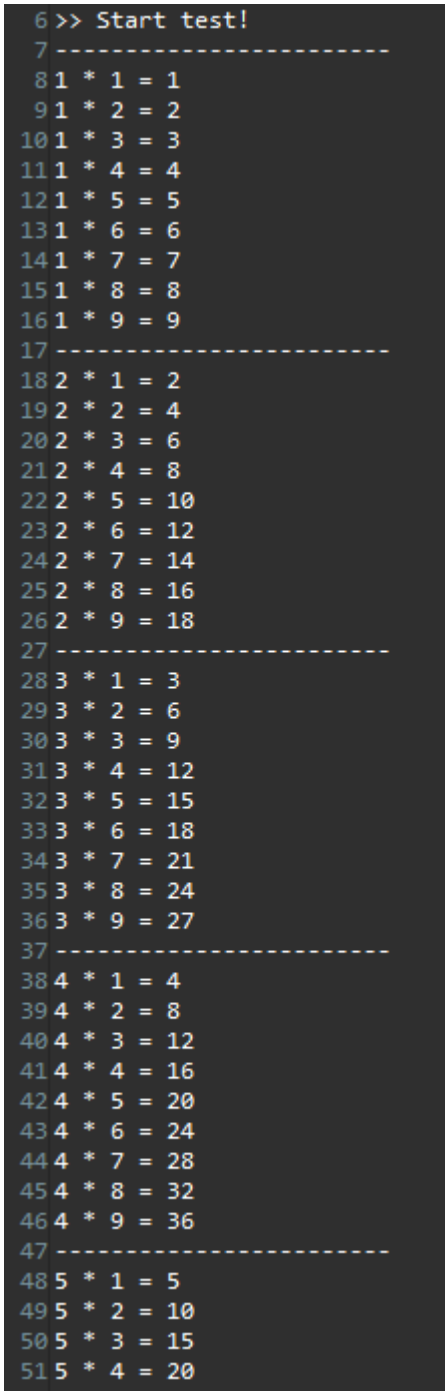
In this lab, I try may way to install vitis_hls ubuntu which run on the docker.
I try the version of 2022.1、2022.2、2023.1. They can be install well but it will have error when I run the co-simulation. This error log is tool bug which I find the comment from the website. So I try may version of vitis_hls.
Finally, I still install the tool 2022.1 on my windows, the error does not happen again.

From this lab, I go through the basic flow of HLS by C++ to a Vivado IP. In this process, I simulation my c++ code, try to synthesis the design, co-simulation design and testbench and finally export the Verilog IP. In each step, I try to find some information from the report to understand the implementation view the design not just the abstractive view of c++ code.

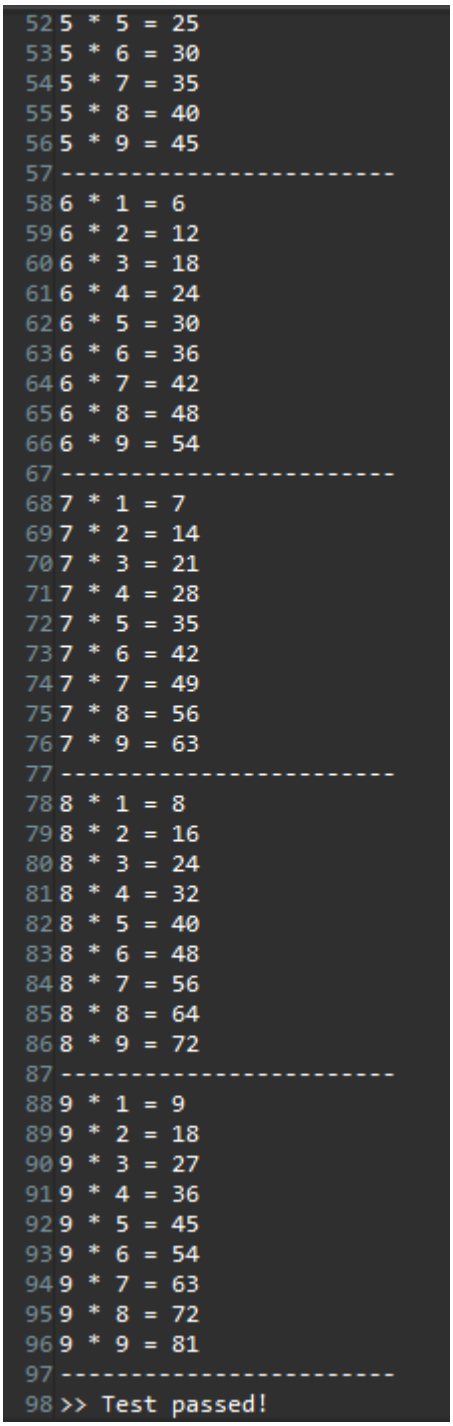
And also I never view the summary report from Solution1->syn->report->multip_2num_csynth.rpt. It is more detail than Flow Navigator-> C SYNTHESIS-> Report & Viewers->Report.

And I learned the flow of hls and integrate to the vivado design. Generating bitstream and upload to the FPGA. The FPGA can control online. I upload the bitstream and edit the python code on Jupyter. I adjust the related file path and compile the code to get the python code result by hw design.

- **C Simulation Result**



```
>> Start test!
------------------------
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
------------------------
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
------------------------
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
------------------------
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
------------------------
5 * 1 = 5
5 * 2 = 10
5 * 3 = 15
5 * 4 = 20
```

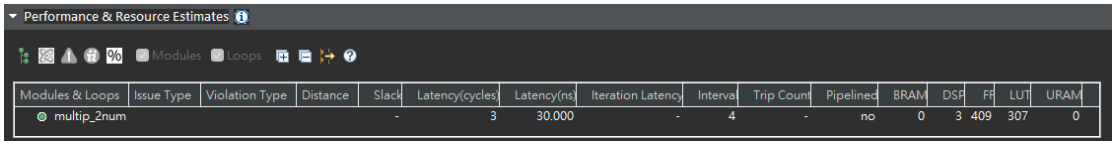


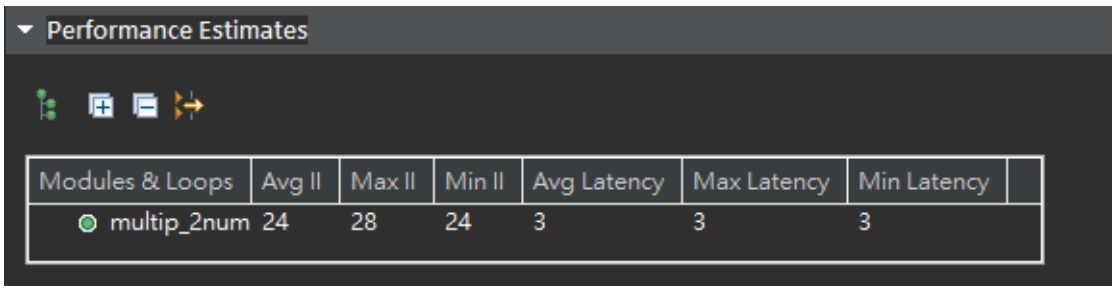
```
5 * 5 = 25
5 * 6 = 30
5 * 7 = 35
5 * 8 = 40
5 * 9 = 45
------------------------
6 * 1 = 6
6 * 2 = 12
6 * 3 = 18
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
------------------------
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
------------------------
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
------------------------
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
------------------------
>> Test passed!
```

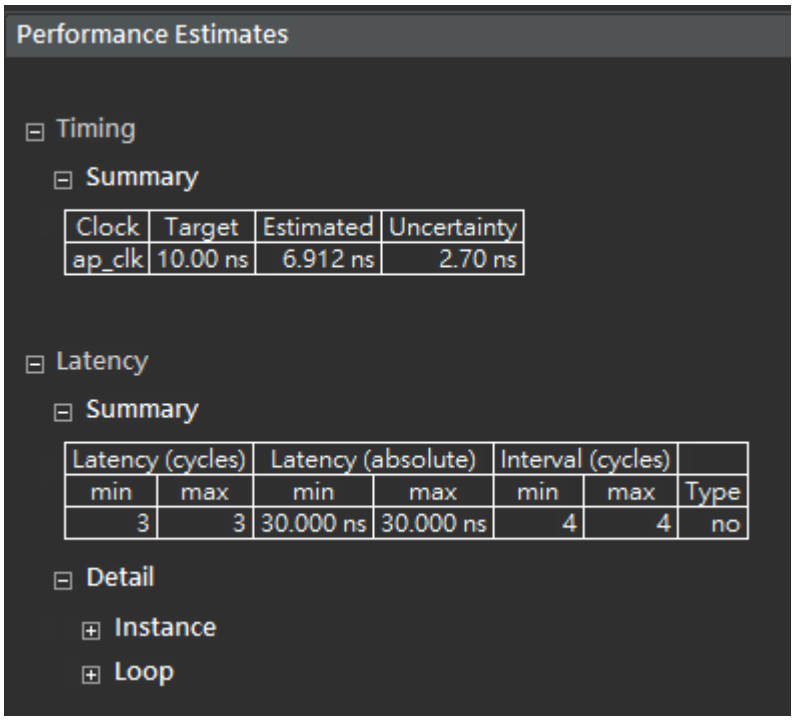
- **Performance**:

FF: 409

LUT: 307



- **Utilization**

Utilization Estimates

Summary

| Name | BRAM_18K | DSP | FF | LUT | URAM |
|---|---|---|---|---|---|
| DSP | - | - | - | - | - |
| Expression | - | - | - | - | - |
| FIFO | - | - | - | - | - |
| Instance | 0 | 3 | 309 | 282 | - |
| Memory | - | - | - | - | - |
| Multiplexer | - | - | - | 25 | - |
| Register | - | - | 100 | - | - |
| Total | 0 | 3 | 409 | 307 | 0 |
| Available | 280 | 220 | 106400 | 53200 | 0 |
| Utilization (%) | 0 | 1 | ~0 | ~0 | 0 |

Detail

- Instance
- DSP
- Memory
- FIFO
- Expression
- Multiplexer
- Register

- **Interface**

HW Interfaces

S_AXILITE Interfaces

| Interface | Data Width | Address Width | Offset | Register | |
|---|---|---|---|---|---|
| s_axi_control | 32 | 6 | 16 | 0 | |
| | | | | | |

S_AXILITE Registers

| Interface | Register | Offset | Width | Access | Description | Bit Fields | |
|---|---|---|---|---|---|---|---|
| s_axi_control | n32In1 | 0x10 | 32 | W | Data signal of n32In1 | | |
| s_axi_control | n32In2 | 0x18 | 32 | W | Data signal of n32In2 | | |
| s_axi_control | pn32ResOut | 0x20 | 32 | R | Data signal of pn32ResOut | | |
| s_axi_control | pn32ResOut_ctrl | 0x24 | 32 | R | Control signal of pn32ResOut | 0=pn32ResOut_ap_vld | |
| | | | | | | | |

TOP LEVEL CONTROL

| Interface | Type | Ports | |
|---|---|---|---|
| ap_clk | clock | ap_clk | |
| ap_rst_n | reset | ap_rst_n | |
| ap_ctrl | ap_ctrl_hs | ap_done ap_idle ap_ready ap_start | |
| | | | |

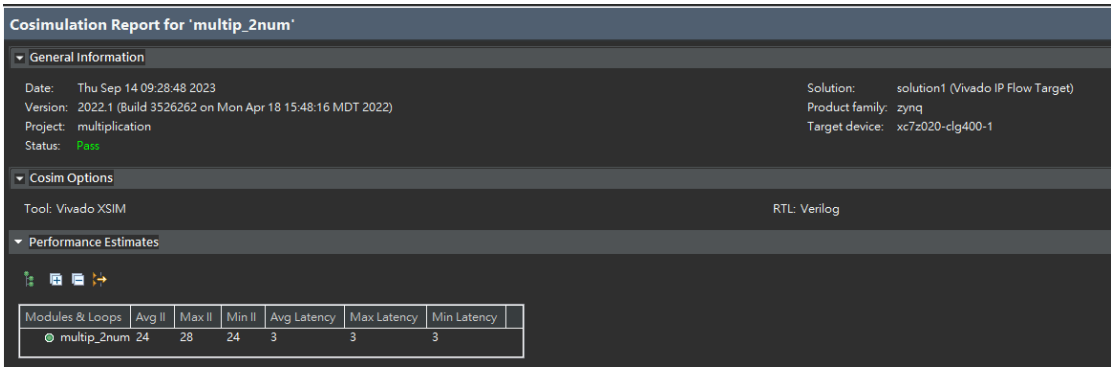
## Interface

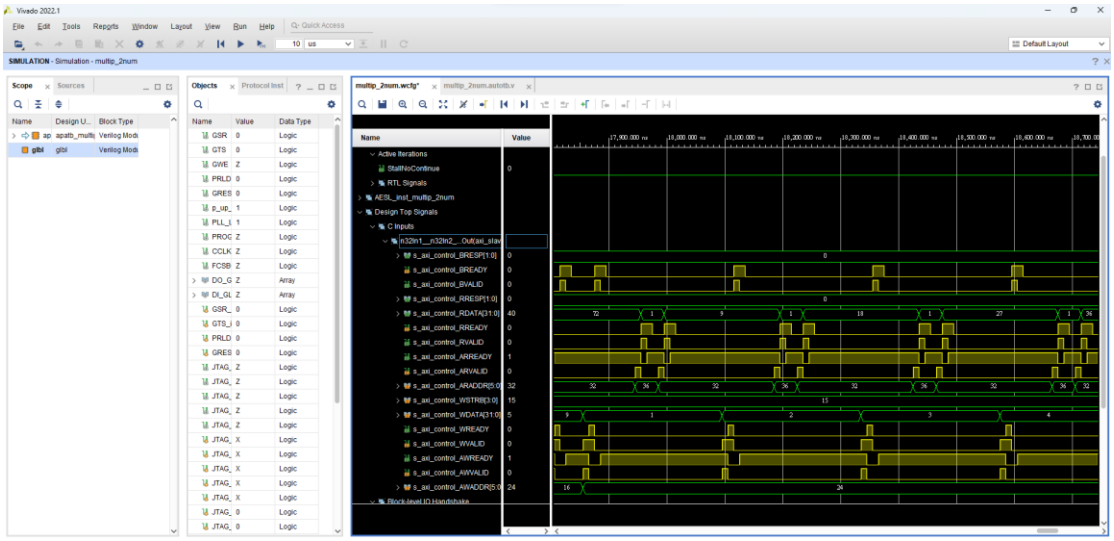
### Summary

| RTL Ports | Dir | Bits | Protocol | Source Object | C Type |
|---|---|---|---|---|---|
| s_axi_control_AWVALID | in | 1 | s_axi | control | pointer |
| s_axi_control_AWREADY | out | 1 | s_axi | control | pointer |
| s_axi_control_AWADDR | in | 6 | s_axi | control | pointer |
| s_axi_control_WVALID | in | 1 | s_axi | control | pointer |
| s_axi_control_WREADY | out | 1 | s_axi | control | pointer |
| s_axi_control_WDATA | in | 32 | s_axi | control | pointer |
| s_axi_control_WSTRB | in | 4 | s_axi | control | pointer |
| s_axi_control_ARVALID | in | 1 | s_axi | control | pointer |
| s_axi_control_ARREADY | out | 1 | s_axi | control | pointer |
| s_axi_control_ARADDR | in | 6 | s_axi | control | pointer |
| s_axi_control_RVALID | out | 1 | s_axi | control | pointer |
| s_axi_control_RREADY | in | 1 | s_axi | control | pointer |
| s_axi_control_RDATA | out | 32 | s_axi | control | pointer |
| s_axi_control_RRESP | out | 2 | s_axi | control | pointer |
| s_axi_control_BVALID | out | 1 | s_axi | control | pointer |
| s_axi_control_BREADY | in | 1 | s_axi | control | pointer |
| s_axi_control_BRESP | out | 2 | s_axi | control | pointer |
| ap_clk | in | 1 | ap_ctrl_hs | multip_2num | return value |
| ap_rst_n | in | 1 | ap_ctrl_hs | multip_2num | return value |
| ap_start | in | 1 | ap_ctrl_hs | multip_2num | return value |
| ap_done | out | 1 | ap_ctrl_hs | multip_2num | return value |
| ap_idle | out | 1 | ap_ctrl_hs | multip_2num | return value |
| ap_ready | out | 1 | ap_ctrl_hs | multip_2num | return value |

Export the report(.html) using the Export Dialog

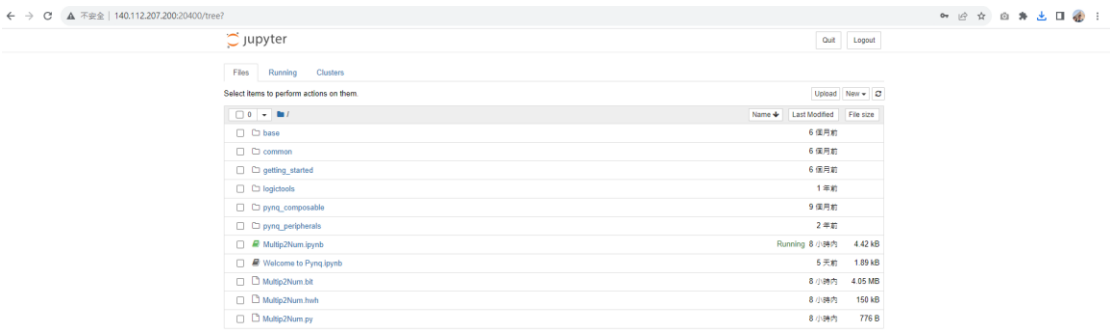
- Co-simulation transcript/Waveform





- **Jupyter Notebook execution results**

```
[1] list all online device boards
[2] rent a specified device board
[3] return your rented device board
[0] exit OnlineFPGA service


please enter your option:
>> 2


[1] pynq
[2] kv260


please enter your option:
>> 1


[1] rent a device board by choice
[2] rent a device board by assignment


please enter your option:
>> 2
device pynq_04 is available
do you want to rent this device? (y/n)
>> y
user michael61112.ee12@nycu.edu.tw rented device pynq_04 successfully
jupyter web ip port is 140.112.207.200:20400, web passwd is fvOvnY and timeup at 09/20/2023 23:43:10
```



```
// Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
// ==========================================================
// control
// 0x00 : reserved
// 0x04 : reserved
// 0x08 : reserved
// 0x0c : reserved
// 0x10 : Data signal of n32In1
//        bit 31~0 - n32In1[31:0] (Read/Write)
// 0x14 : reserved
// 0x18 : Data signal of n32In2
//        bit 31~0 - n32In2[31:0] (Read/Write)
// 0x1c : reserved
// 0x20 : Data signal of pn32ResOut
//        bit 31~0 - pn32ResOut[31:0] (Read)
// 0x24 : Control signal of pn32ResOut
//        bit 0  - pn32ResOut_ap_vld (Read/COR)
//        others - reserved
// (SC = Self Clear, COR = Clear on Read, TOW = Toggle on Write, COH = Clear on Handshake)

#define XMULTIP_2NUM_CONTROL_ADDR_N32IN1_DATA     0x10
#define XMULTIP_2NUM_CONTROL_BITS_N32IN1_DATA     32
#define XMULTIP_2NUM_CONTROL_ADDR_N32IN2_DATA     0x18
#define XMULTIP_2NUM_CONTROL_BITS_N32IN2_DATA     32
#define XMULTIP_2NUM_CONTROL_ADDR_PN32RESOUT_DATA 0x20
#define XMULTIP_2NUM_CONTROL_BITS_PN32RESOUT_DATA 32
#define XMULTIP_2NUM_CONTROL_ADDR_PN32RESOUT_CTRL 0x24
```

jupyter Multip2Num Last Checkpoint: 2 分鐘前 (autosaved)

Logout

File Edit View Insert Cell Kernel Widgets Help

Not Trusted | Python 3

Run Code Vollä

In [1]:

```
# coding: utf-8

# In[ ]:


from __future__ import print_function

import sys, os

sys.path.append('/home/xilinx')
os.environ['XILINX_XRT'] = '/usr'
from pynq import Overlay

if __name__ == "__main__":
    print("Entry:", sys.argv[0])
    print("System argument(s):", len(sys.argv))

    print("Start of \"" + sys.argv[0] + "\"")

    ol = Overlay("/home/xilinx/jupyter_notebooks/Multip2Num.bit")
    regIP = ol.multip_2num_0

    for i in range(9):
        print("============================")
        for j in range(9):
            regIP.write(0x10, i + 1)
            regIP.write(0x18, j + 1)
            Res = regIP.read(0x20)
            print(str(i + 1) + " * " + str(j + 1) + " = " + str(Res))
    print("============================")
    print("Exit process")
```

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
============================
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
============================
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
============================
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
============================
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
============================
5 * 1 = 5
5 * 2 = 10
5 * 3 = 15
5 * 4 = 20
5 * 5 = 25
5 * 6 = 30
5 * 7 = 35
5 * 8 = 40
5 * 9 = 45
============================
6 * 1 = 6
6 * 2 = 12
6 * 3 = 18
6 * 4 = 24
6 * 5 = 30
6 * 6 = 36
6 * 7 = 42
6 * 8 = 48
6 * 9 = 54
============================
7 * 1 = 7
7 * 2 = 14
7 * 3 = 21
7 * 4 = 28
7 * 5 = 35
7 * 6 = 42
7 * 7 = 49
7 * 8 = 56
7 * 9 = 63
============================
8 * 1 = 8
8 * 2 = 16
8 * 3 = 24
8 * 4 = 32
8 * 5 = 40
8 * 6 = 48
8 * 7 = 56
8 * 8 = 64
8 * 9 = 72
============================
9 * 1 = 9
9 * 2 = 18
9 * 3 = 27
9 * 4 = 36
9 * 5 = 45
9 * 6 = 54
9 * 7 = 63
9 * 8 = 72
9 * 9 = 81
============================
Exit process
```

In [ ]: