SoC Design Lab2

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- **Brief introduction about the overall system**

  We use hls to design a FIR hardware. We try to add MAXI and Stream interface to the ZYNQ. The interface is created by hls but we have to connect ZYNQ by adding HP Slave AXI Interface. If all the connection is done, we should generate bitstream and upload it to the FPGA. We use python code the send the input data of samples_triangular_wave, n32Taps and length of data. And we get back fir result to compare with golden data. The filter will change a little the waveform, but we still can see the triangle.

- **What is observed & learned**

  - Differences between MAXI and Stream interface

    By using Stream interface, we add the DMA ip beyond and behind our FIR IP.

    We can see the python code result, the kernel execution time of Stream is larger than MAXI.

  - Differences between csim and cosim

    For the cosim, the simulation use the synthesis result to run the testbench. It will spend more time than csim which totally software simulation. Because when we run the cosim, it should do synthesis first.
    For the cosim report, the avg latency of Stream is larger than MAXI.

FIRN11MAXI/

- **C Simulation Result**

```
<terminated> (exit value: 0) FIRN11MAXI_ip.Debug [C/C++ Application] csim.exe
>> Start test!
>> Comparing against output data...
正在比較檔案 .\out.dat 和 ..\..\..\OUT_GOLD.DAT
FC: 找不到相異處
>> Test passed!
-------------------------
```

- **Performance**:

FF: 3081

LUT: 1151

Modules & Loops	Issue Type	Viol	Distance	Latency(cycles)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
fir_n11_maxi				-	-	-	-	no	0	33	3081	1151	0
fir_n11_maxi_Pipeline_XFER_LOOP				-	-	-	-	no	0	33	2689	986	0

Timing Estimate

Target	Estimated	Uncertainty	
10.00 ns	6.923 ns	2.70 ns	

- **Utilization**

```
================================================================
== Utilization Estimates
================================================================
* Summary:
+-----------------+---------+-----+--------+-------+-----+
|       Name      | BRAM_18K| DSP |   FF   |  LUT  | URAM|
+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     40|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    3806|   2838|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|    175|    -|
|Register         |        -|    -|     650|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    4456|   3053|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       4|      5|    0|
+-----------------+---------+-----+--------+-------+-----+
```

- **Interface**

HW Interfaces

M_AXI

Interface	Data Width (SW->HW)	Address Width	Latency	Offset	Register	Max Widen Bitwidth	Max Read Burst Length	Max Write Burst Length	Num Read Outstanding	Num Write Outstanding
m_axi_gmem	32 -> 32	64	0	slave	0	0	16	16	16	16

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
s_axi_control	32	7	16	0

S_AXILITE Registers

Interface	Register	Offset	Width	Access	Description	Bit Fields
s_axi_control	CTRL	0x00	32	RW	Control signals	0=AP_START 1=AP_DONE 2=AP_IDLE 3=AP_READY 7=AUTO_RESTART 9=INTERRUPT
s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	pn32HPInput_1	0x10	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPInput_2	0x14	32	W	Data signal of pn32HPInput	
s_axi_control	pn32HPOutput_1	0x1c	32	W	Data signal of pn32HPOutput	
s_axi_control	pn32HPOutput_2	0x20	32	W	Data signal of pn32HPOutput	
s_axi_control	regXferLeng	0x28	32	W	Data signal of regXferLeng	

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt
ap_ctrl	ap_ctrl_hs	

- Co-simulation transcript/Waveform

Cosimulation Report for 'fir_n11_maxi'

General Information

Date: Tue Oct 17 20:58:20 2023
Version: 2022.1 (Build 3526262 on Mon Apr 18 15:48:16 MDT 2022)
Project: FIRN11MAXI_ip
Status: Pass

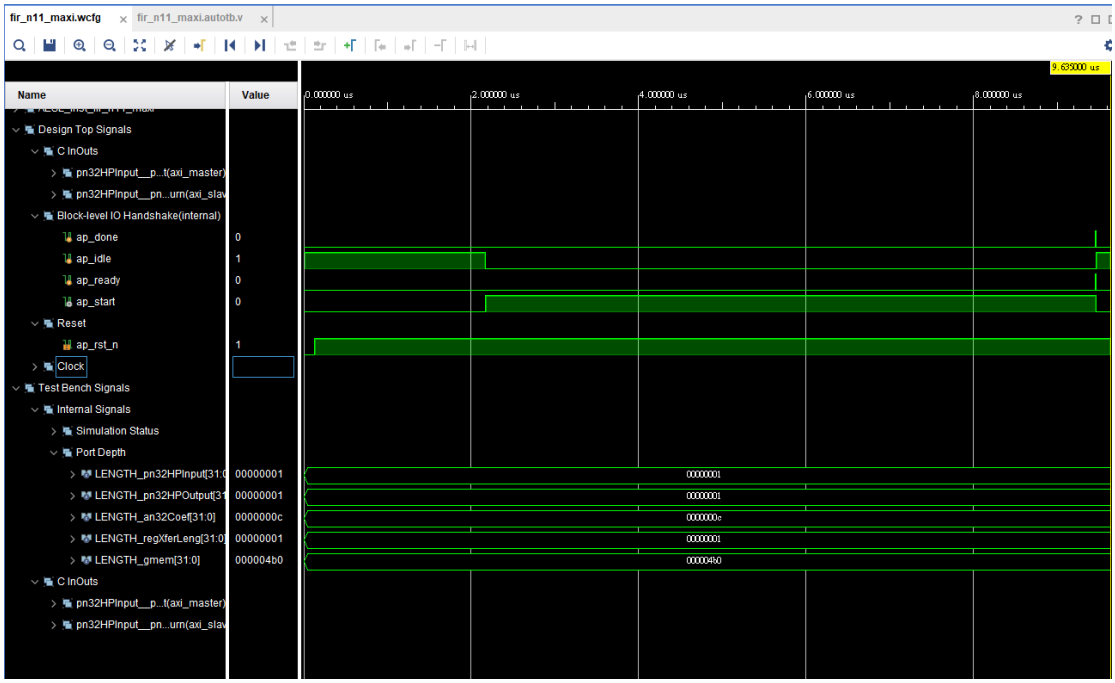
Solution: solution1 (Vivado IP Flow Target)
Product family: zynq
Target device: xc7z020-clg400-1

Cosim Options

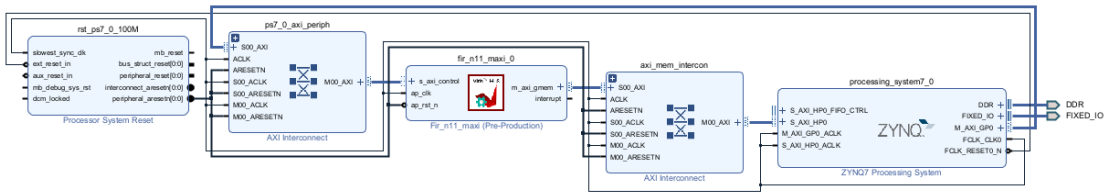
Tool: Vivado XSIM
RTL: Verilog

Performance Estimates

Modules & Loops	Avg II	Max II	Min II	Avg Latency	Max Latency	Min Latency
fir_n11_maxi				728	728	728
fir_n11_maxi_Pipeline_XFER_LOOP				715	715	715

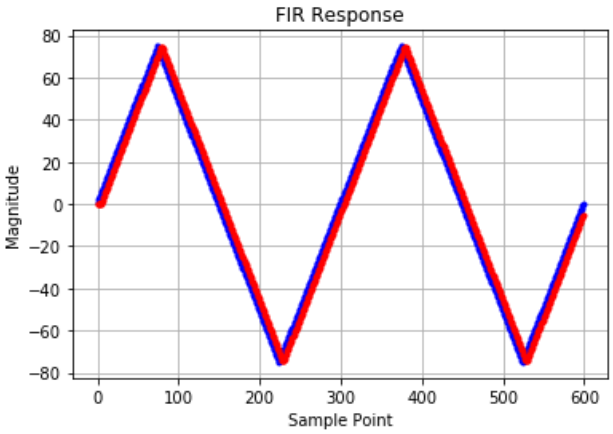


- Vivado block desgin



- **Jupyter Notebook execution results**

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.000675201416015625 s
```




```
============================
Exit process
```

FIRN11Stream/

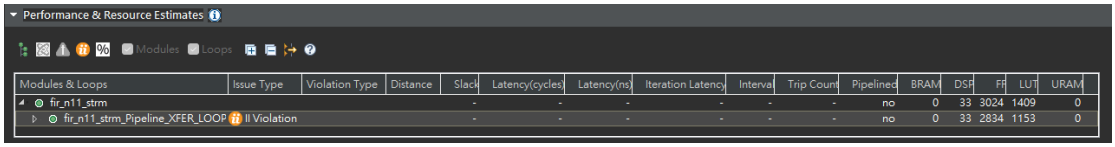
- **C Simulation Result**

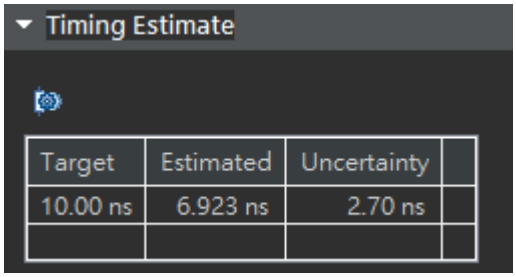
```
Vitis HLS Console
                from ../../../FIR.cpp:2:
C:/Xilinx/Vitis_HLS/2022.1/include/floating_point_v7_0_bitacc_cmodel.h:136:0: note: this is the location of the previous definition
 #define __GMP_LIBGMP_DLL 1

>> Start test!
>> Comparing against output data...
♦♦♦b♦♦♦♦b♦ .\out.dat @M ..\..\..\OUT_GOLD.DAT
FC: ♦♯♯♦♦r♦♦B

>> Test passed!
------------------------
```

- **Performance、Utilization**

FF: 3024

LUT: 1409





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* Summary:
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+-----------------+---------+-----+--------+-------+-----+
|DSP              |        -|    -|       -|      -|    -|
|Expression       |        -|    -|       0|     42|    -|
|FIFO             |        -|    -|       -|      -|    -|
|Instance         |        0|   33|    2988|   1333|    -|
|Memory           |        -|    -|       -|      -|    -|
|Multiplexer      |        -|    -|       -|     34|    -|
|Register         |        -|    -|      36|      -|    -|
+-----------------+---------+-----+--------+-------+-----+
|Total            |        0|   33|    3024|   1409|    0|
+-----------------+---------+-----+--------+-------+-----+
|Available        |      280|  220|  106400|  53200|    0|
+-----------------+---------+-----+--------+-------+-----+
|Utilization (%)  |        0|   15|       2|      2|    0|
+-----------------+---------+-----+--------+-------+-----+
```

- **Interface**

HW Interfaces

S_AXILITE Interfaces

Interface	Data Width	Address Width	Offset	Register
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S_AXILITE Registers

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s_axi_control	GIER	0x04	32	RW	Global Interrupt Enable Register	0=Enable
s_axi_control	IP_IER	0x08	32	RW	IP Interrupt Enable Register	0=CHAN0_INT_EN 1=CHAN1_INT_EN
s_axi_control	IP_ISR	0x0c	32	RW	IP Interrupt Status Register	0=CHAN0_INT_ST 1=CHAN1_INT_ST
s_axi_control	regXferLeng	0x10	32	W	Data signal of regXferLeng	

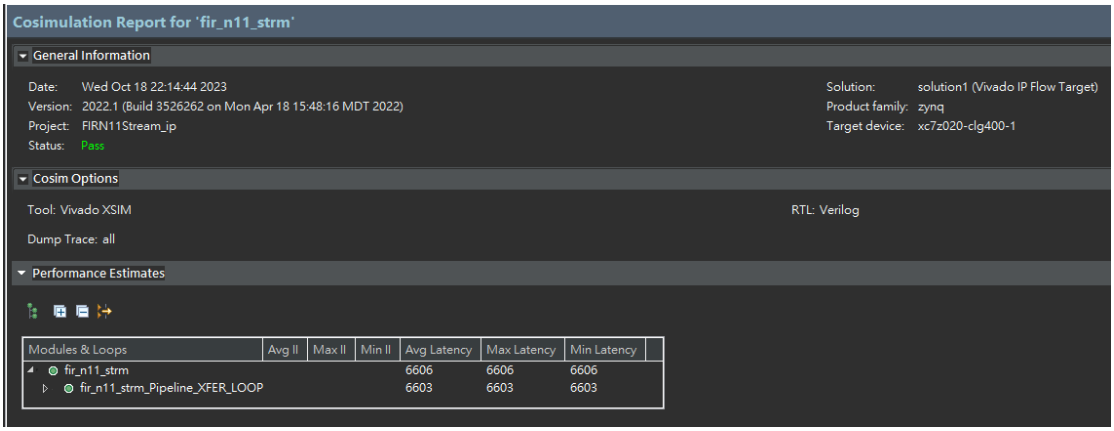
AXIS

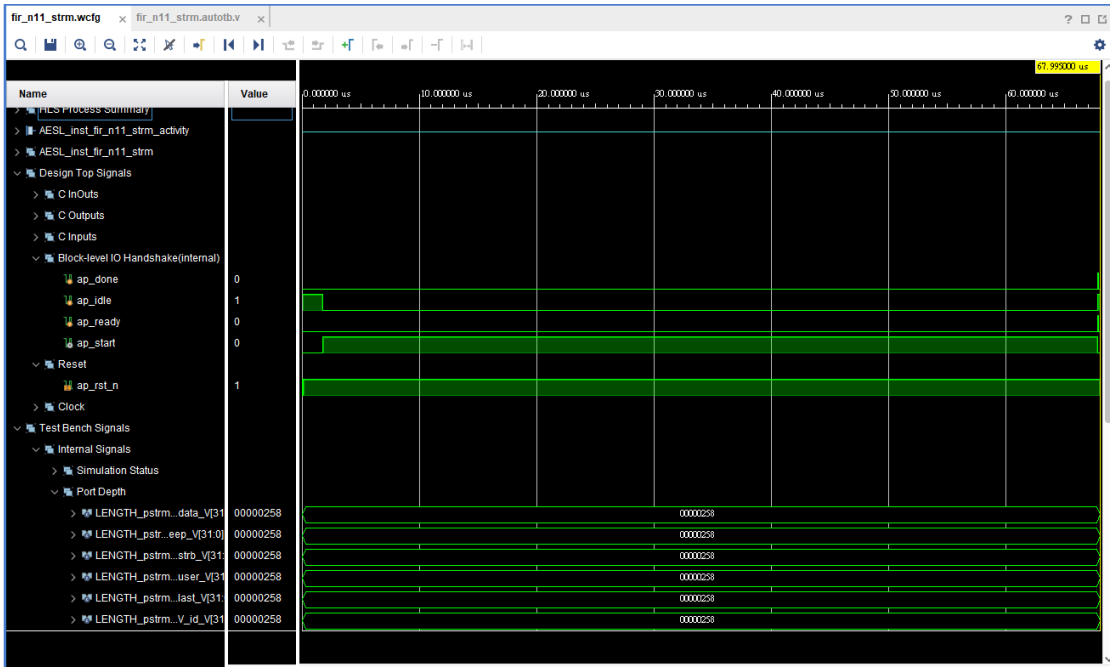
Interface	Register Mode	TDATA	TDEST	TID	TKEEP	TLAST	TREADY	TSTRB	TUSER	TVALID
pstrmInput	both	32	1	1	4	1	1	4	1	1
pstrmOutput	both	32	1	1	4	1	1	4	1	1

TOP LEVEL CONTROL

Interface	Type	Ports
ap_clk	clock	ap_clk
ap_rst_n	reset	ap_rst_n
interrupt	interrupt	interrupt
ap_ctrl	ap_ctrl_hs	

- Co-simulation transcript/Waveform

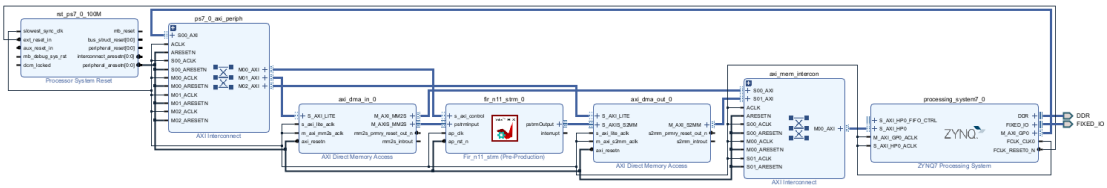




- Vivado block desgin

FIR_N11_STRM的pstrminput接到axi_dma_in_0的M_AXIS_MM2S

FIR_N11_STRM 的 pstrmoutput 接到 axi_dma_out_0 的 S_AXIS_S2MM



Name	Interface	Slave Segment	Master Base Address	Range	Master High Address
Network 0					
/axi_dma_in_0					
/axi_dma_in_0/Data_MM2S (32 address bits : 4G)					
/processing_system7_0/S_AXI_HP0	S_AXI_HP0	HP0_DDR_LOWOCM	0x0000_0000	512M	0x1FFF_FFFF
/axi_dma_out_0					
/axi_dma_out_0/Data_MM2S (32 address bits : 4G)					
/processing_system7_0/S_AXI_HP0	S_AXI_HP0	HP0_DDR_LOWOCM	0x0000_0000	512M	0x1FFF_FFFF
Network 1					
/processing_system7_0					
/processing_system7_0/Data (32 address bits : 0x40000000 [1G])					
/axi_dma_in_0/S_AXI_LITE	S_AXI_LITE	Reg	0x41E0_0000	64K	0x41E0_FFFF
/axi_dma_out_0/S_AXI_LITE	S_AXI_LITE	Reg	0x41E1_0000	64K	0x41E1_FFFF
/fir_n11_strm_0/s_axi_control	s_axi_control	Reg	0x4000_0000	64K	0x4000_FFFF

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Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
Kernel execution time: 0.0017936229705810547 s
```

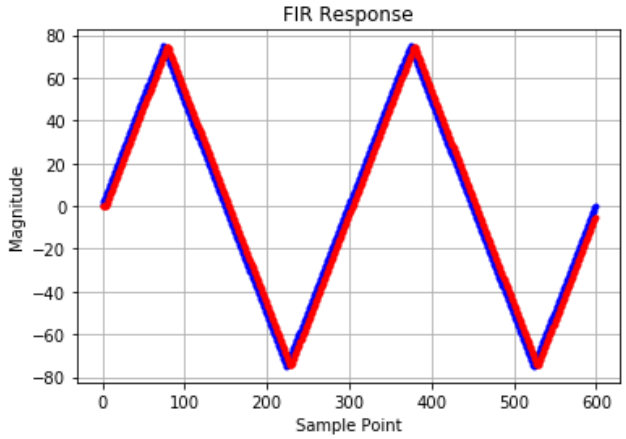


```
============================
Exit process
```