

Simulation Guide

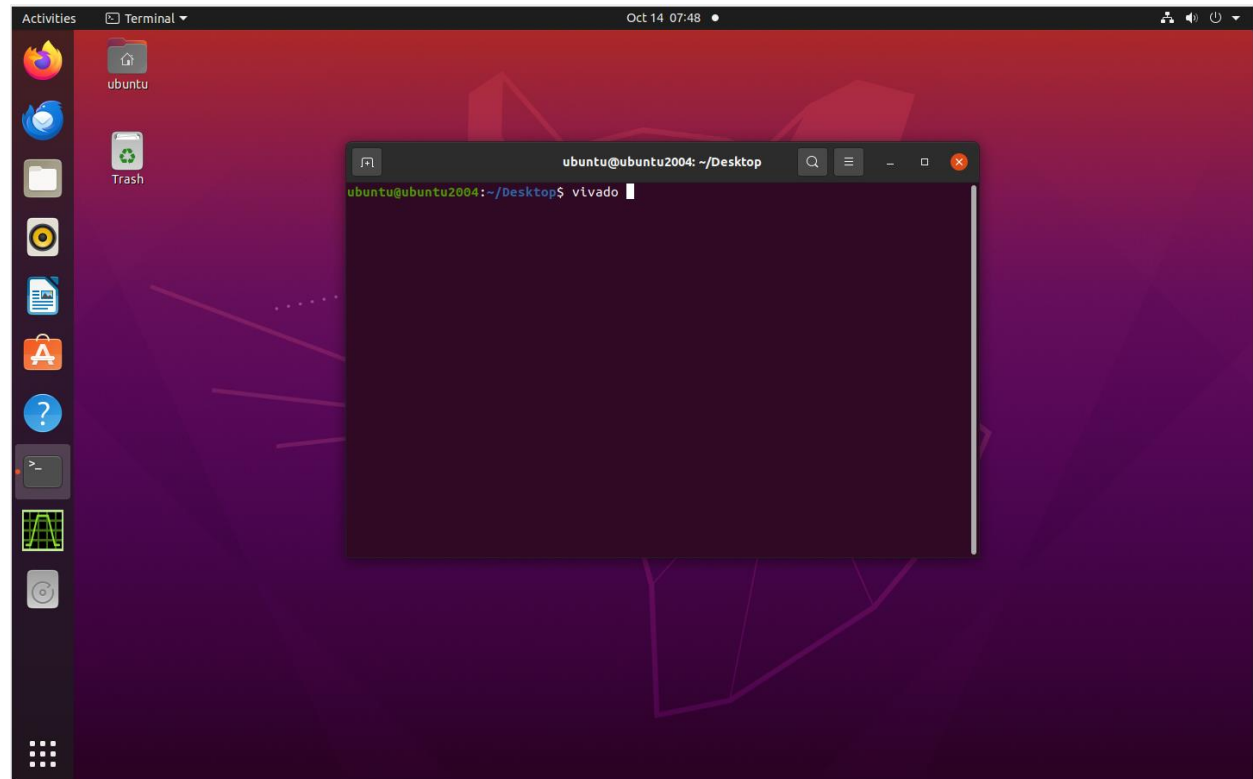
SOC Design

Simulation Guide

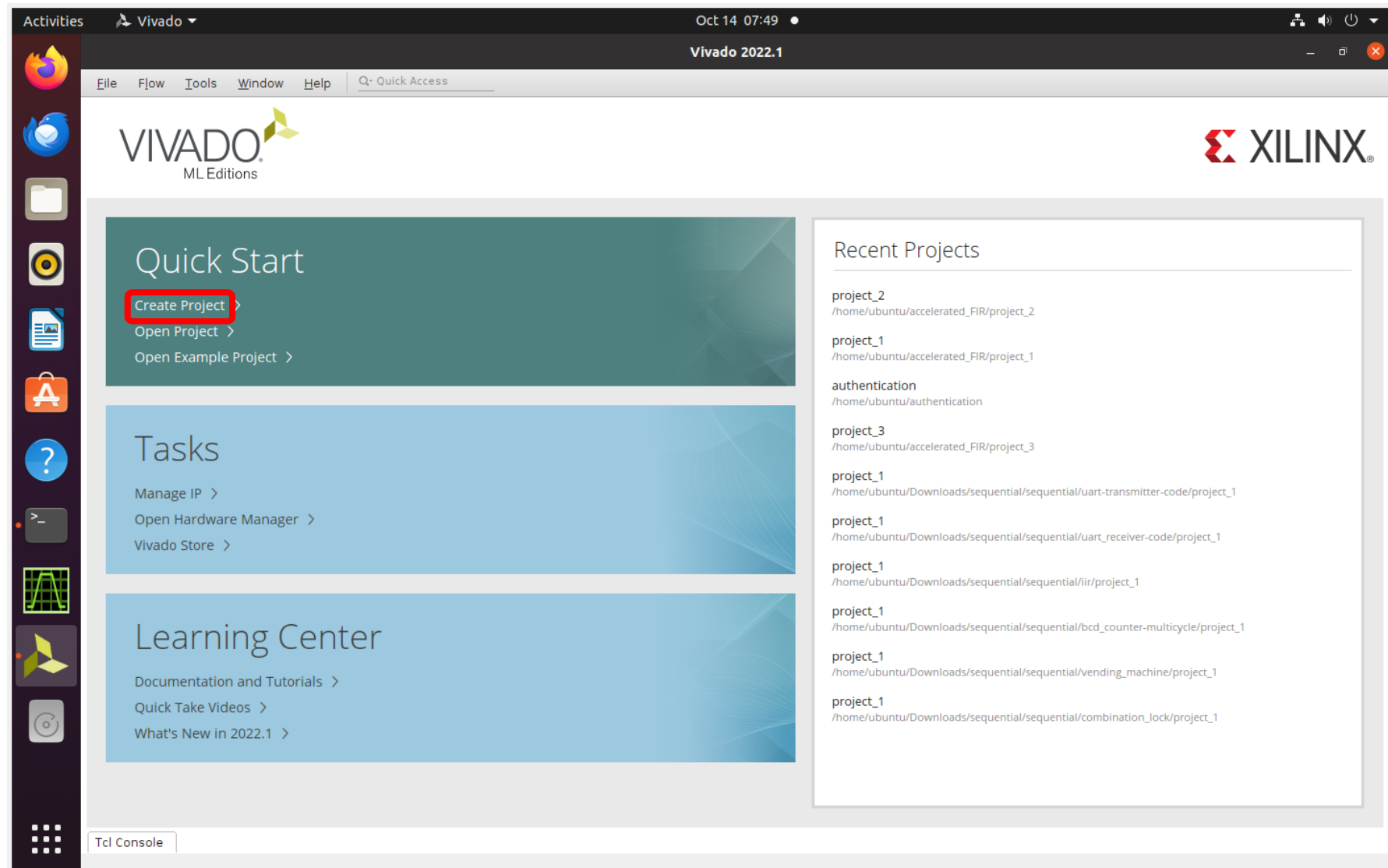
- **There are two methods for simulation**
 - **Vivado GUI**
 - **Makefile (only work on linux system)**
- You only need to choose one method for simulation.

1. Implement Flow (Vivado GUI)

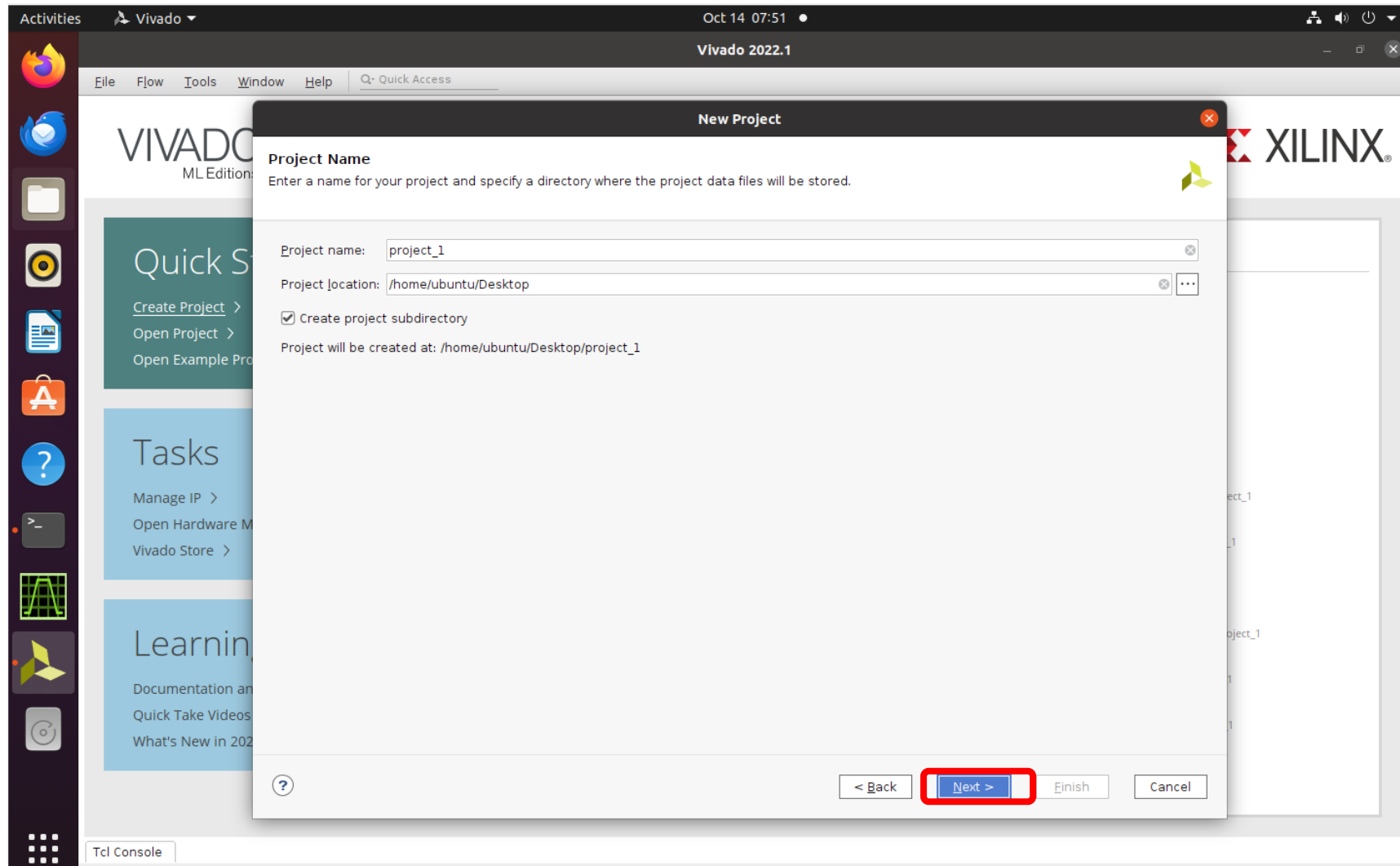
- 1.1. Vivado
 - 【施作環境為Windows/ Linux】
 - 啟動Vivado



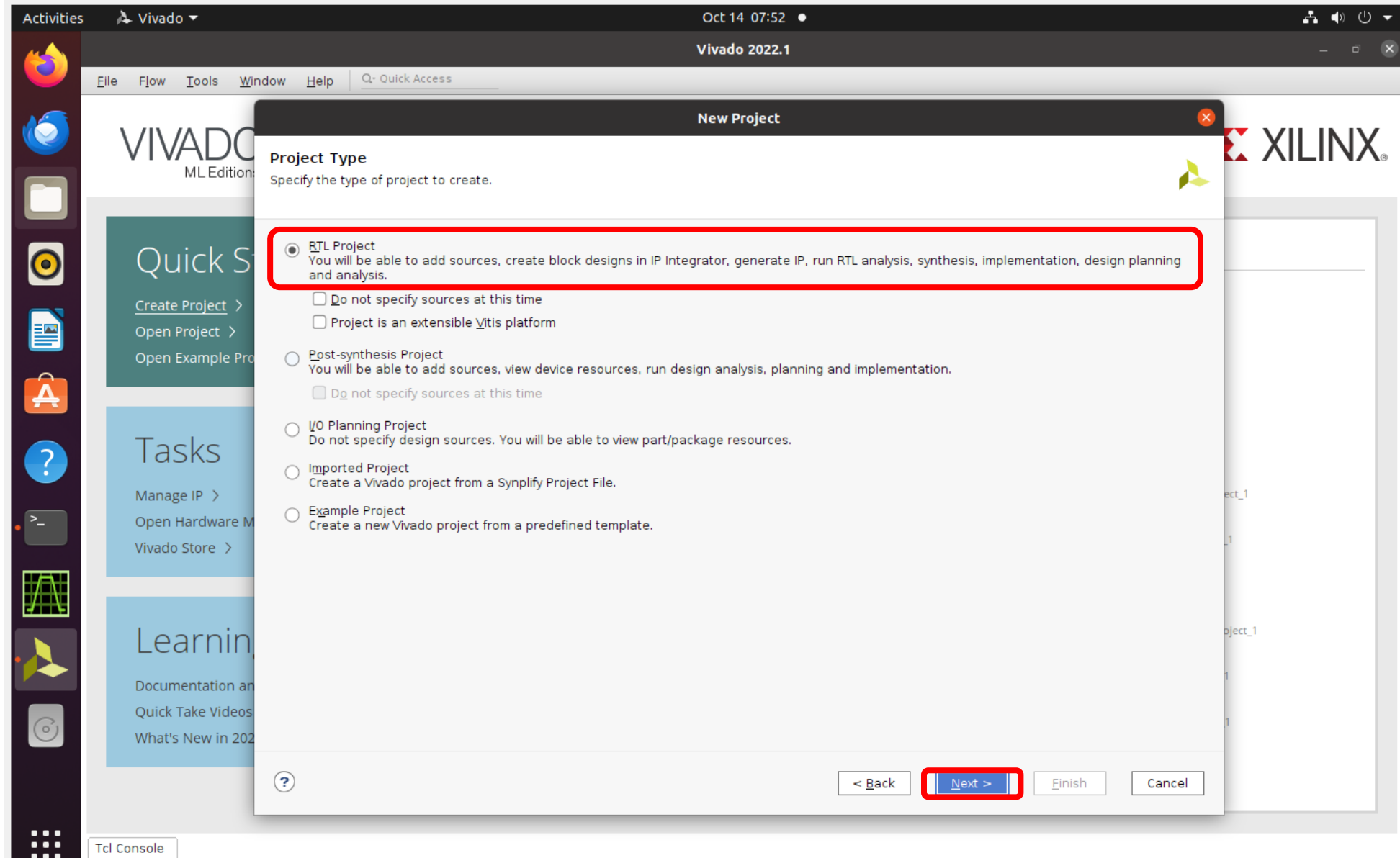
• 1.1.1 Create Project



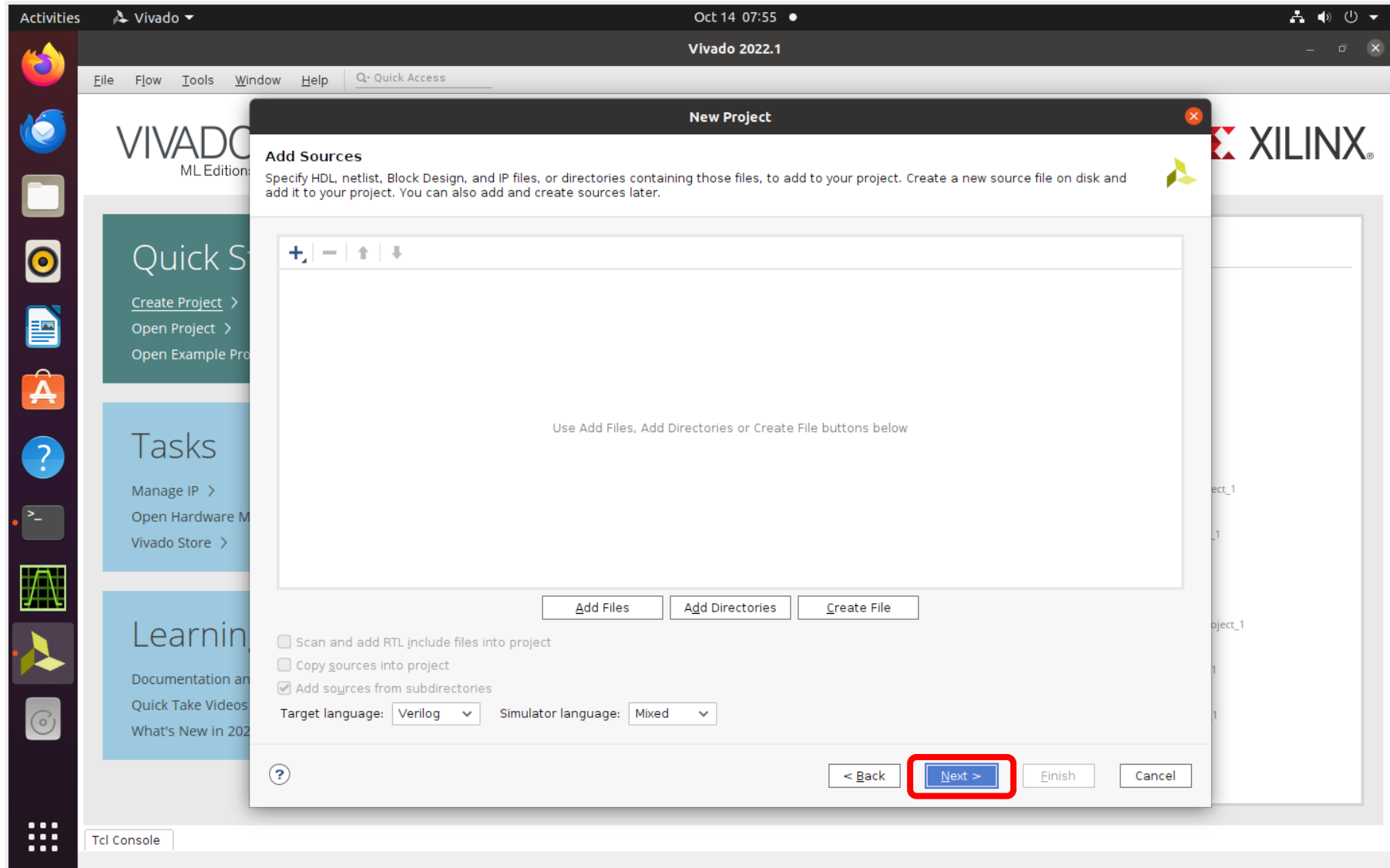
- **1.1.2 Follow the step to create the project**



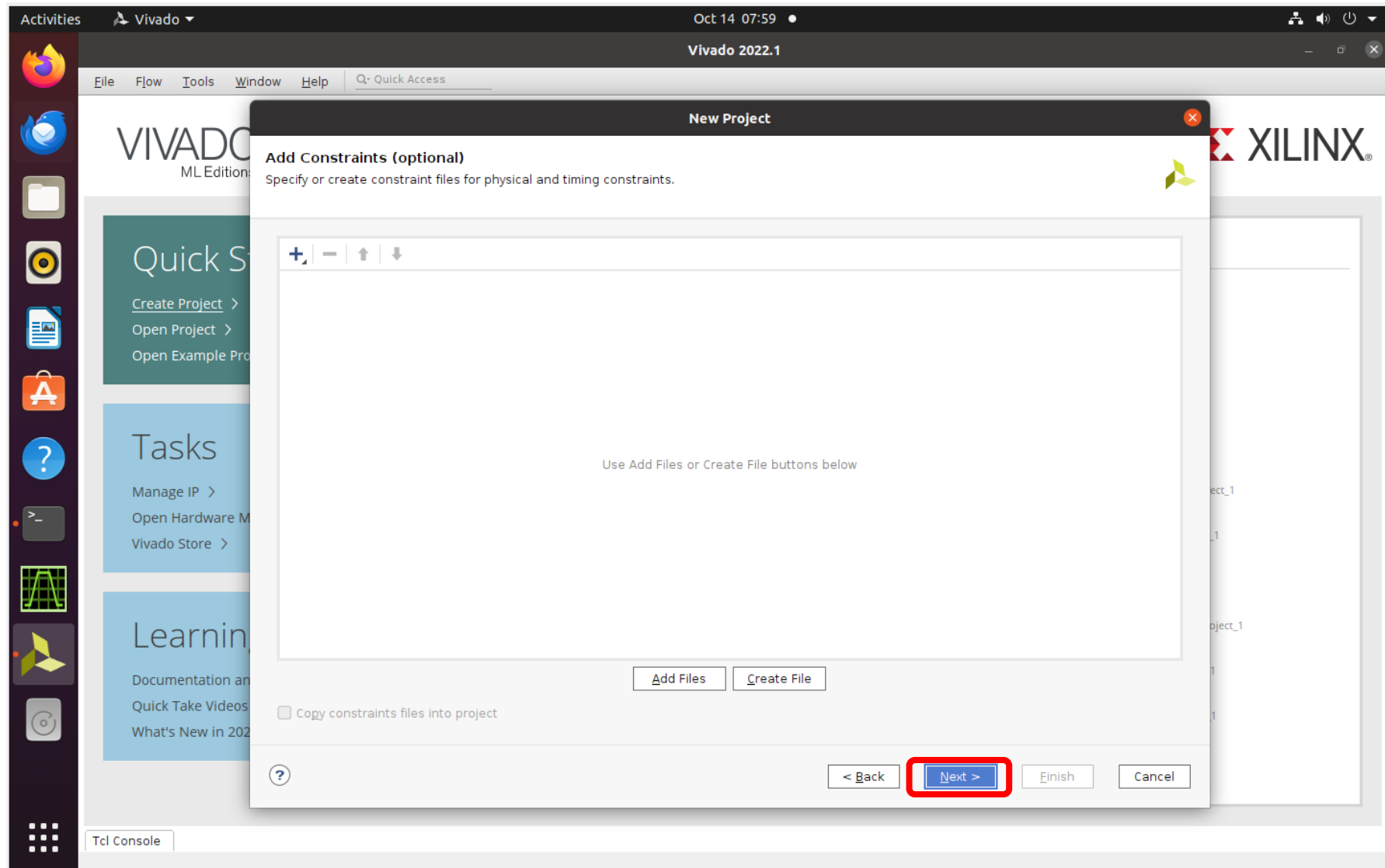
• 1.1.3 Select RTL Project



- **1.1.4 Add the design file**
 - **【如果還沒進行設計，可直接點擊next】**

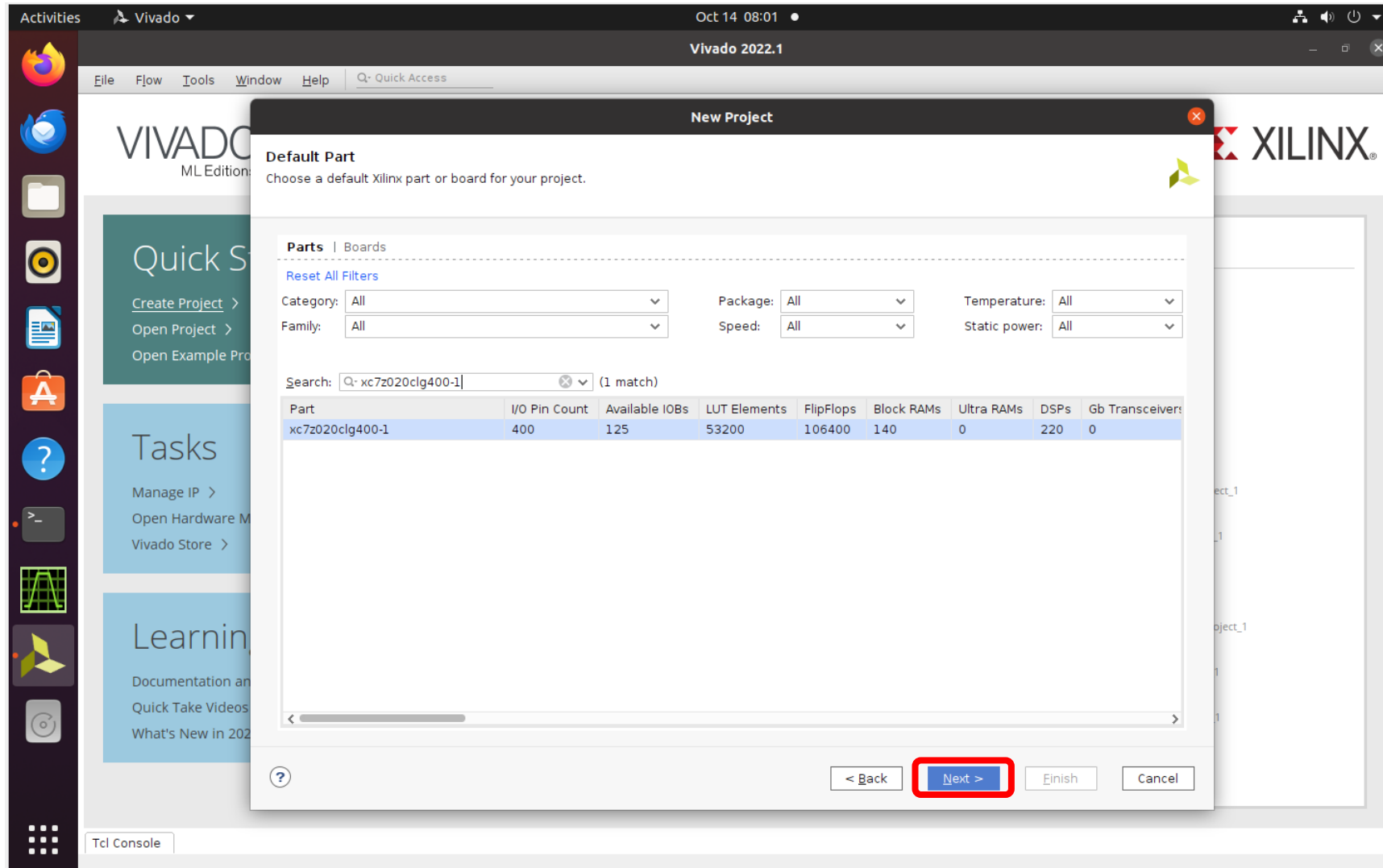


- 1.1.5 Add the constraints file
 - 【如果沒有constraints file，可直接點擊next】

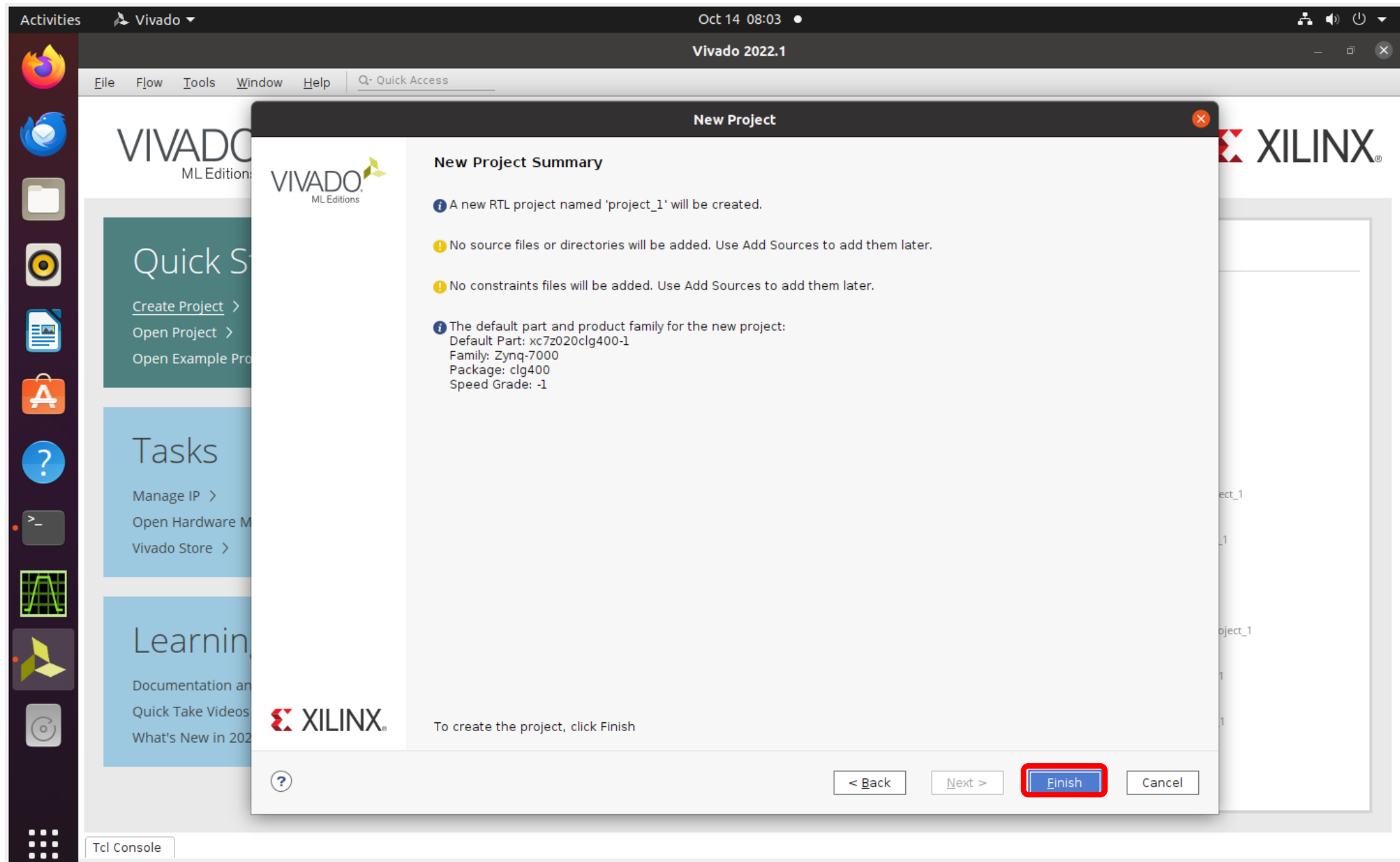


- **1.1.6 Select FPGA board**

- **【根據需求選取FPGA板，這裡選用pynq-z2】**

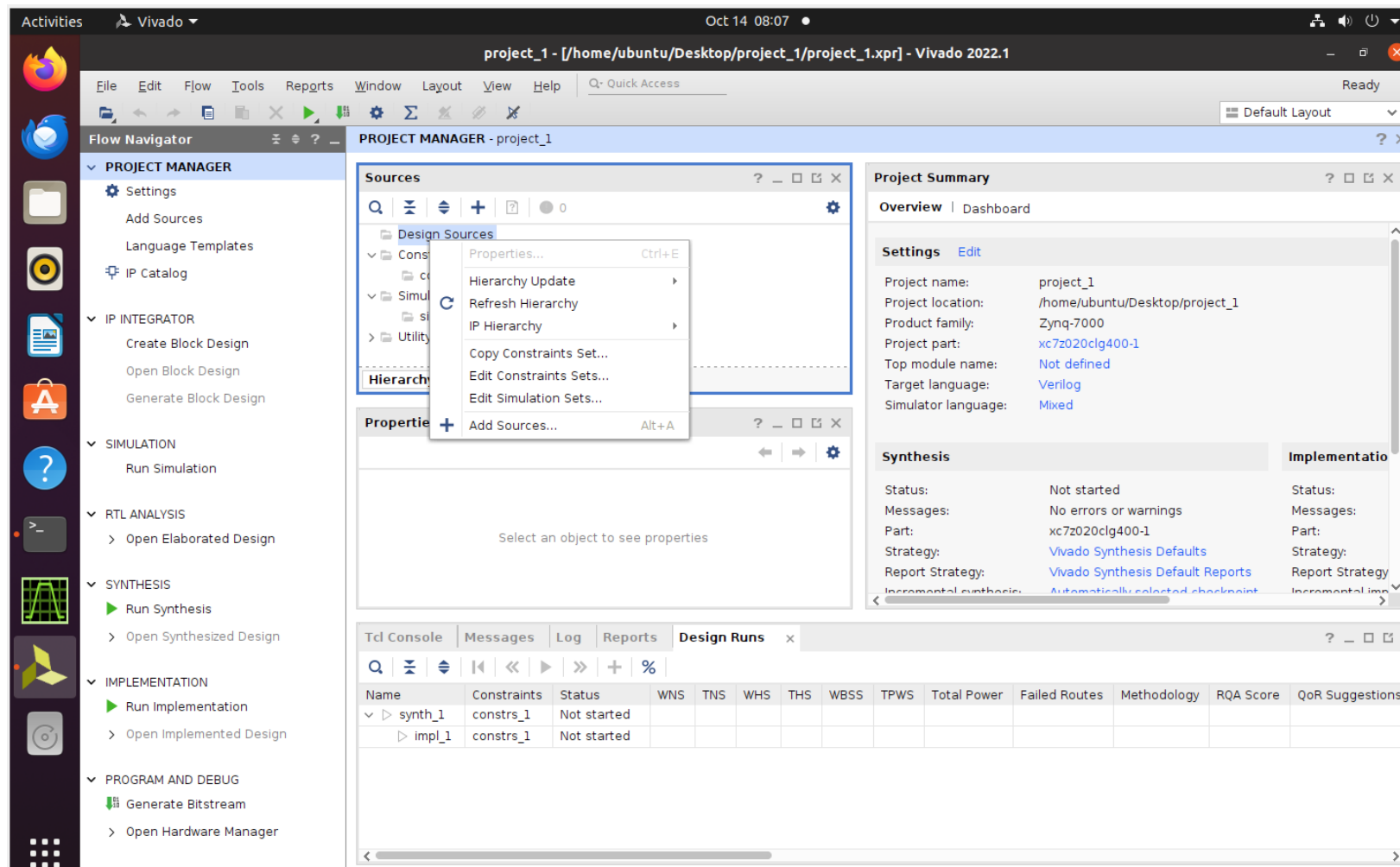


• 1.1.7 Create the project

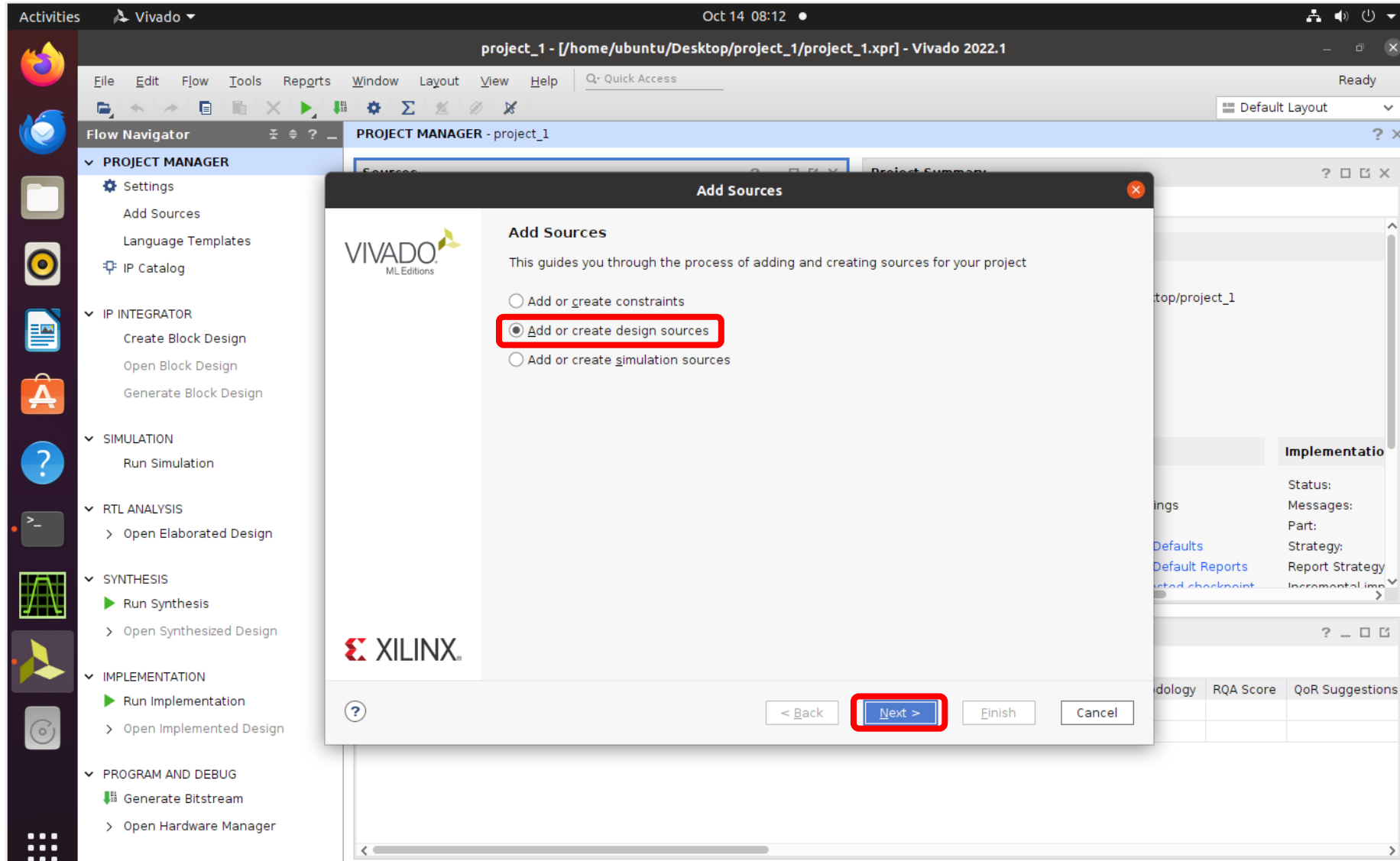


- **1.2.1 Add Sources**

- **【右鍵點擊Design Sources，選擇Add Sources】**

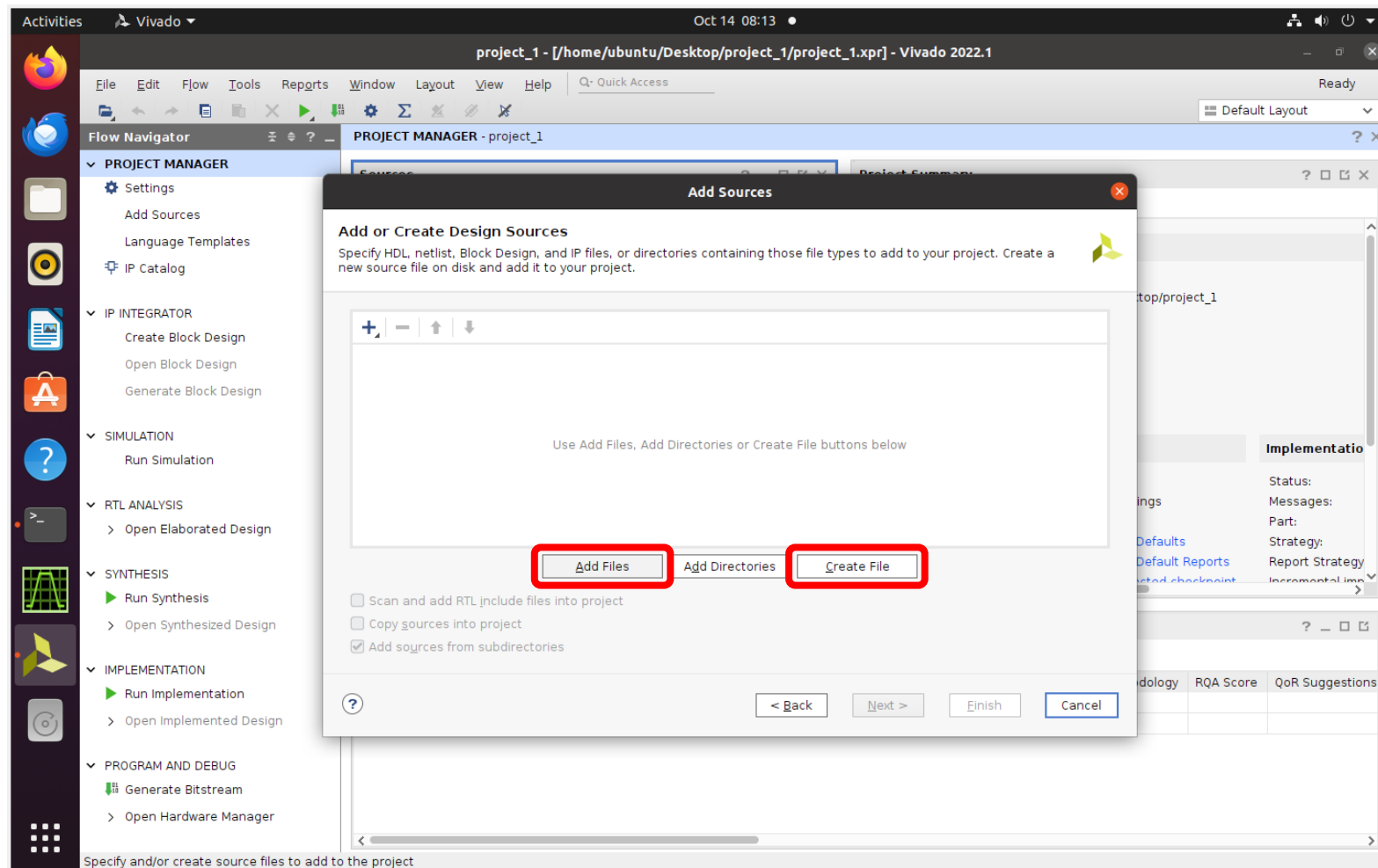


- 1.2.2 Add or Create Design Source
 - 【選取Add or Create Design Sources】



• 1.2.3 Add Files

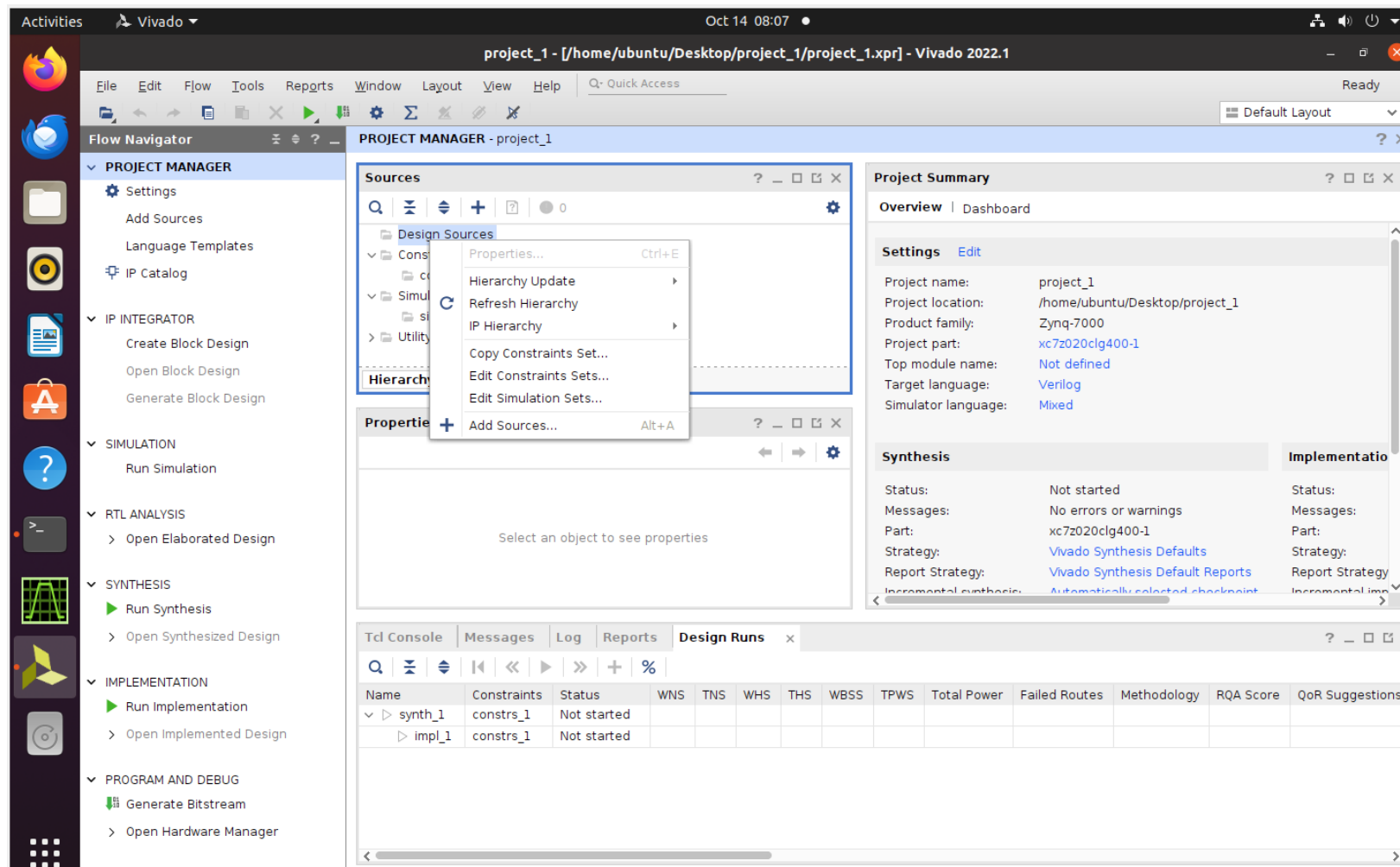
- 【如果已有設計檔，選取Add files】
- 【如果沒有設計檔，選取Create file】



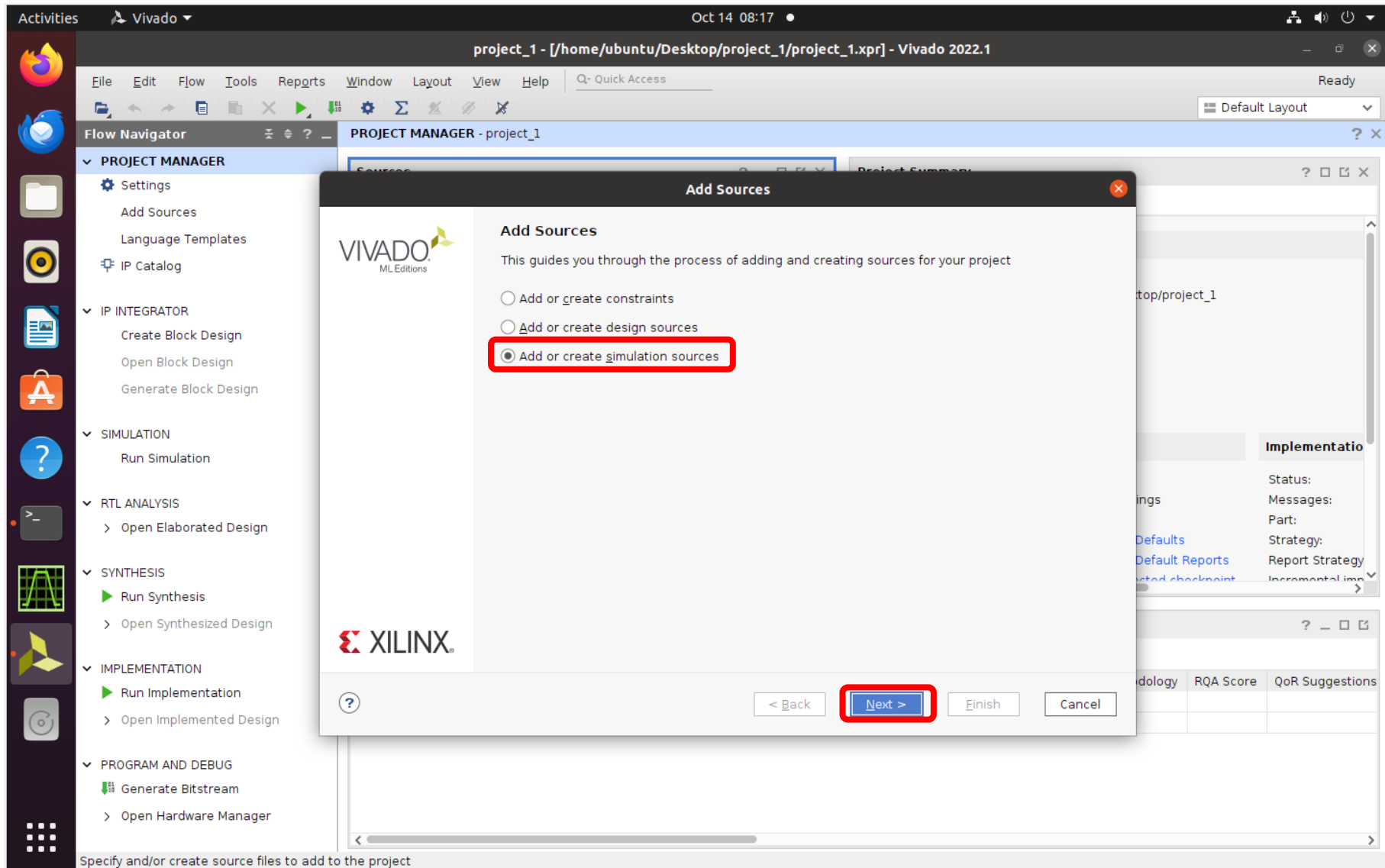
- **1.3 Add Testbench**

- **1.3.1 Add Sources**

- **【右鍵點擊Design Sources，選擇Add Sources】**

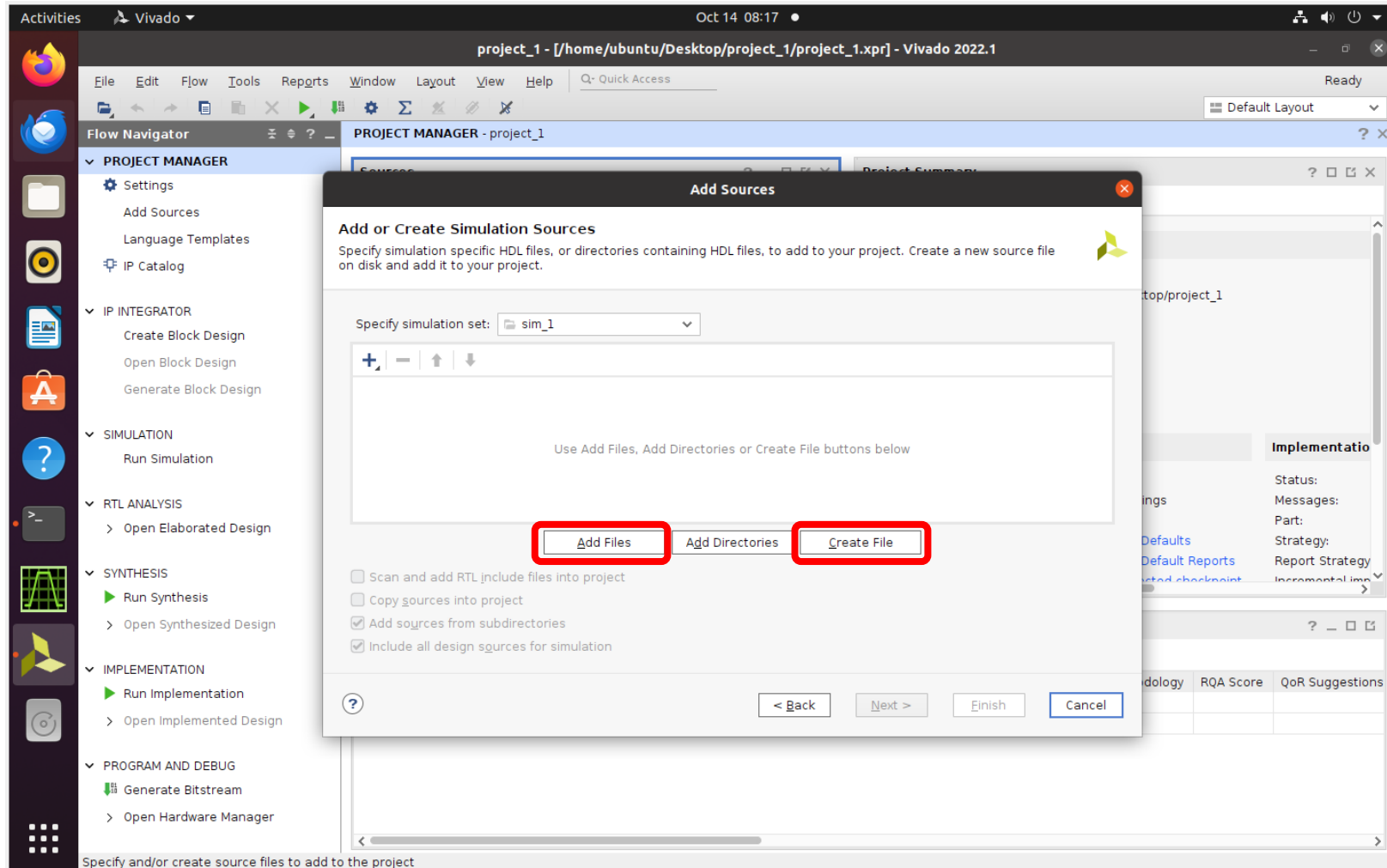


- 1.3.2 Add or Create Simulation Source
 - 【選取Add or Create Simulation Sources】



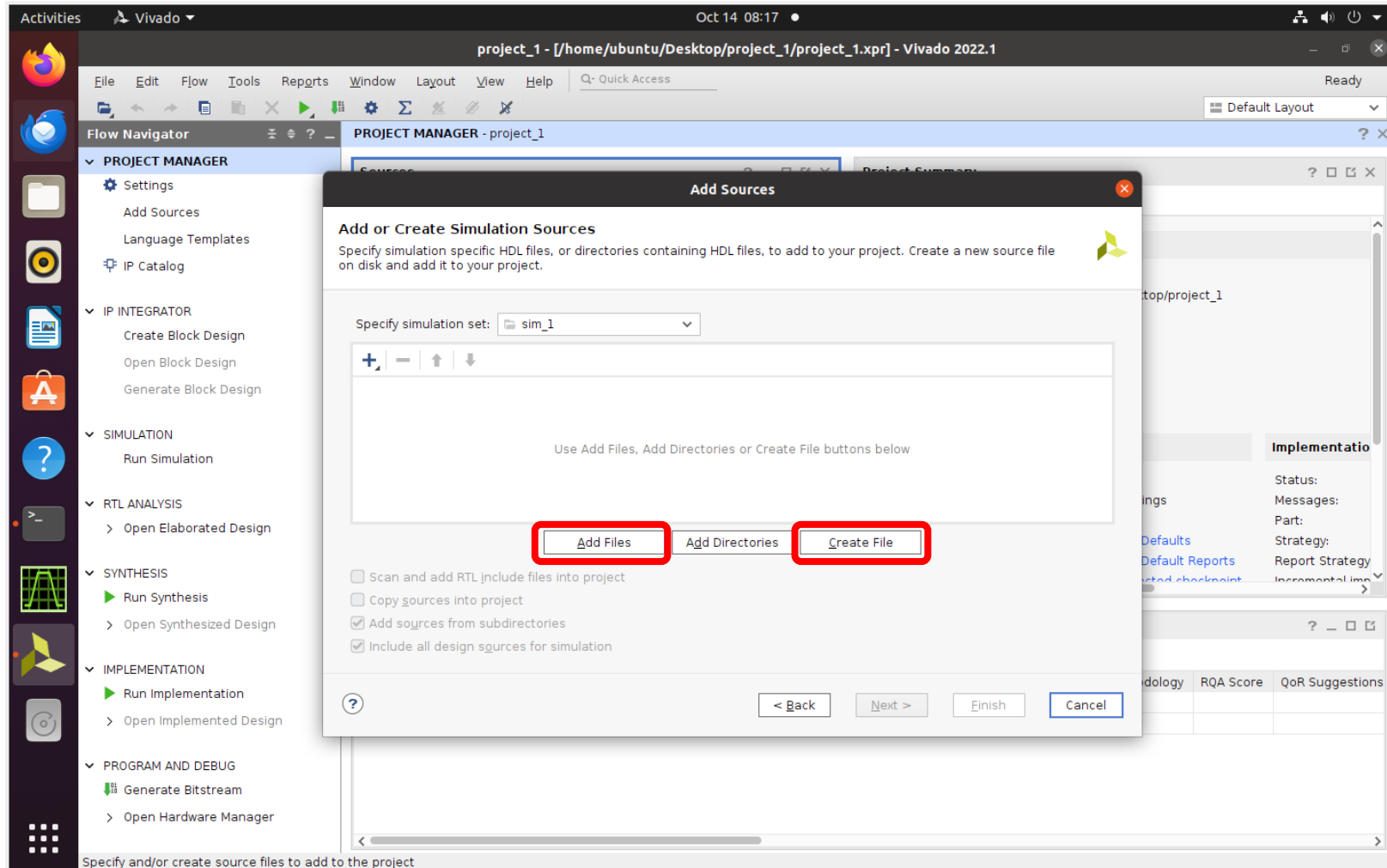
• 1.3.3 Add Files

- 【如果已有Testbench，選取Add files】
- 【如果沒有Testbench，選取Create file】

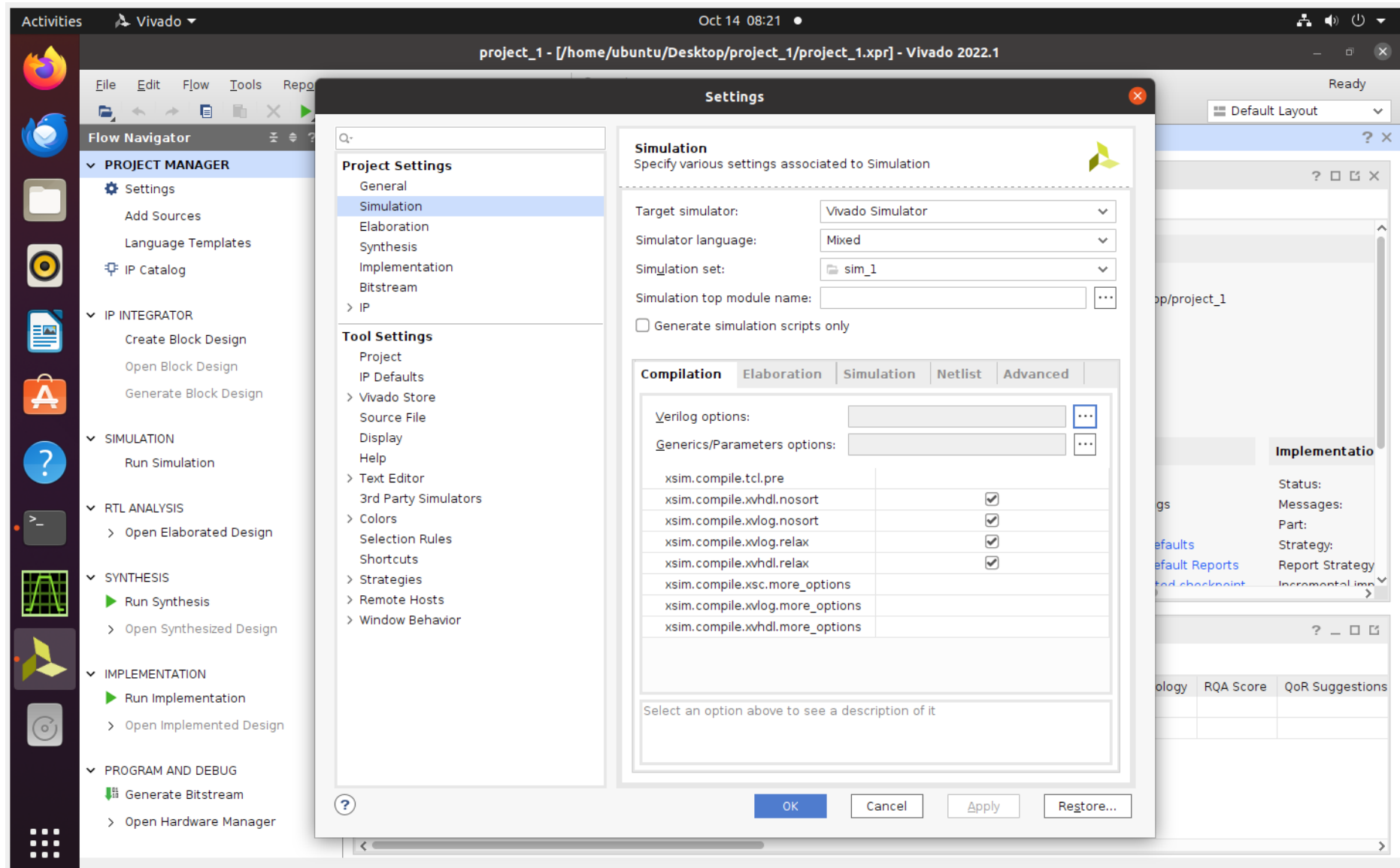


- **1.4 Add Files**

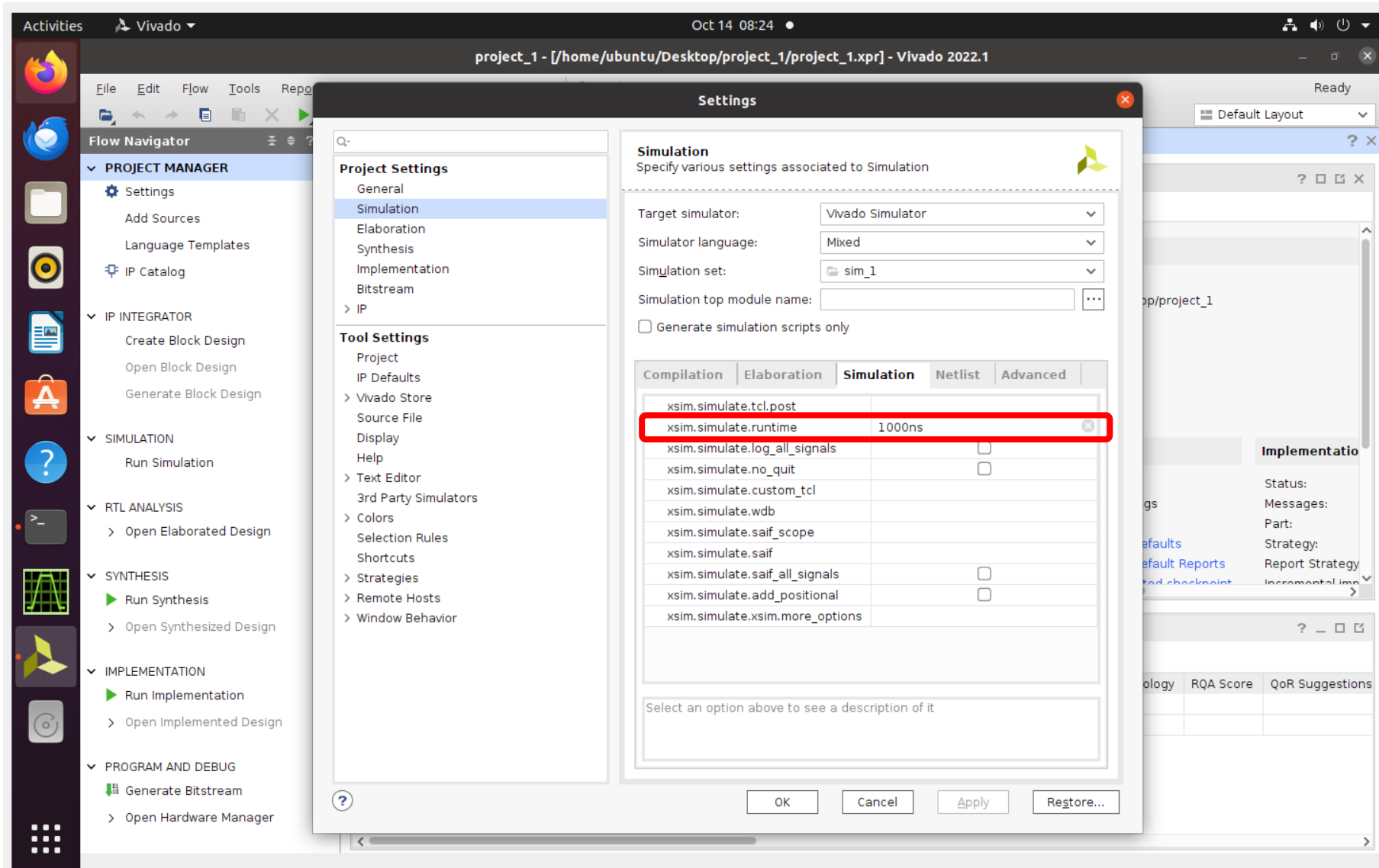
- **【如果已有Testbench，選取Add files】**
- **【如果沒有Testbench，選取Create file】**



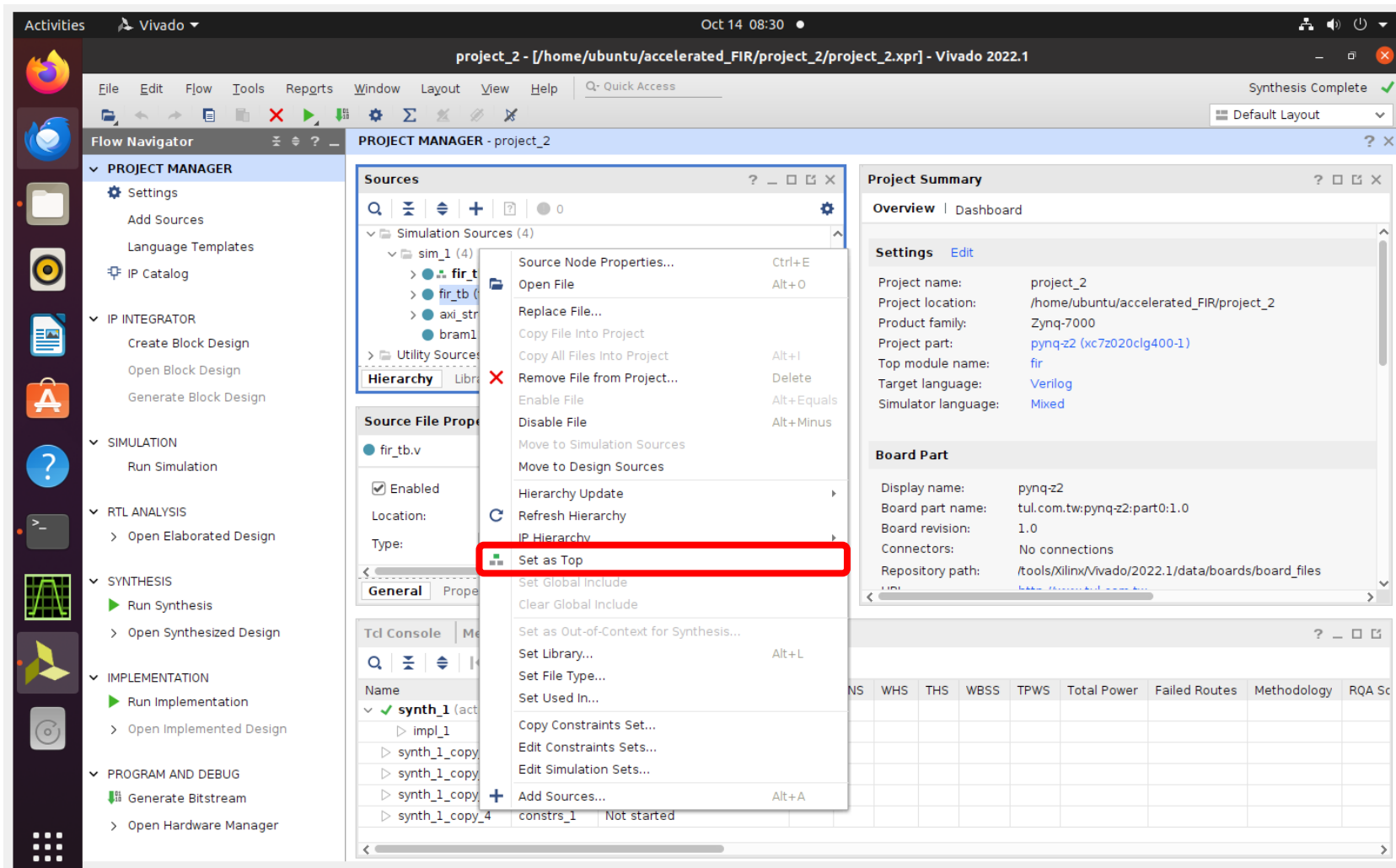
- 1.4.2 Modify Simulation Settings
 - 【根據testbench的需求調整Simulation settings】



- 1.4.3 Modify Simulation runtime
 - 【在Lab3中，可能需要調整simulation runtime】

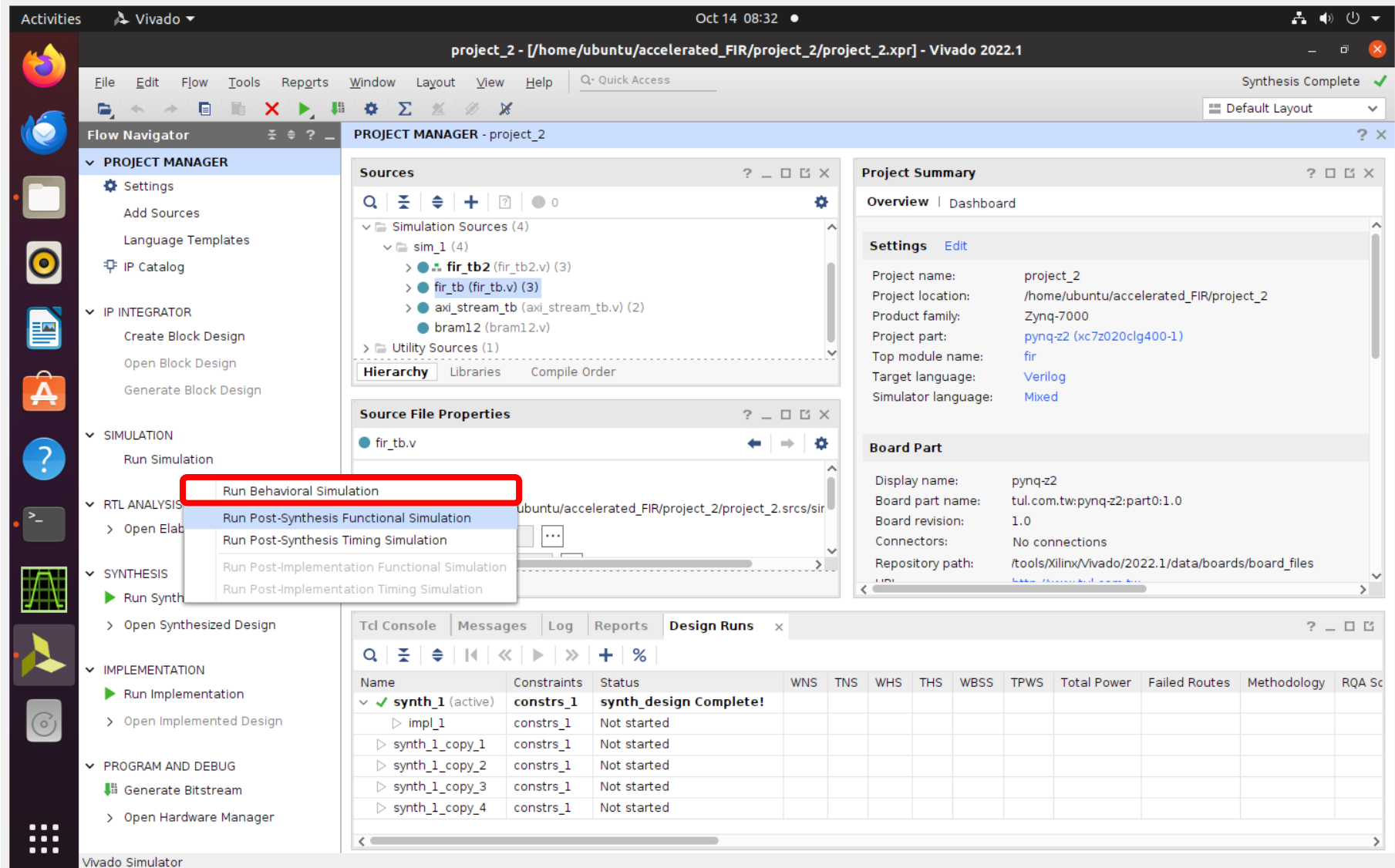


- 1.5 Run Simulation
- 1.5.1 Set the testbench file as top
 - 【右鍵點擊testbench，點擊Set as Top】



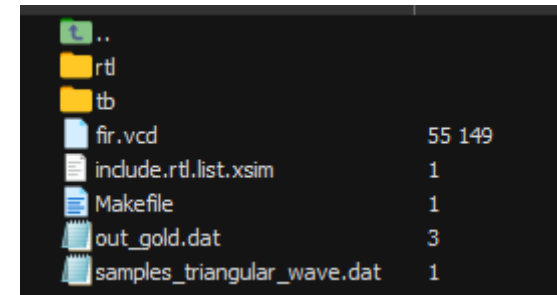
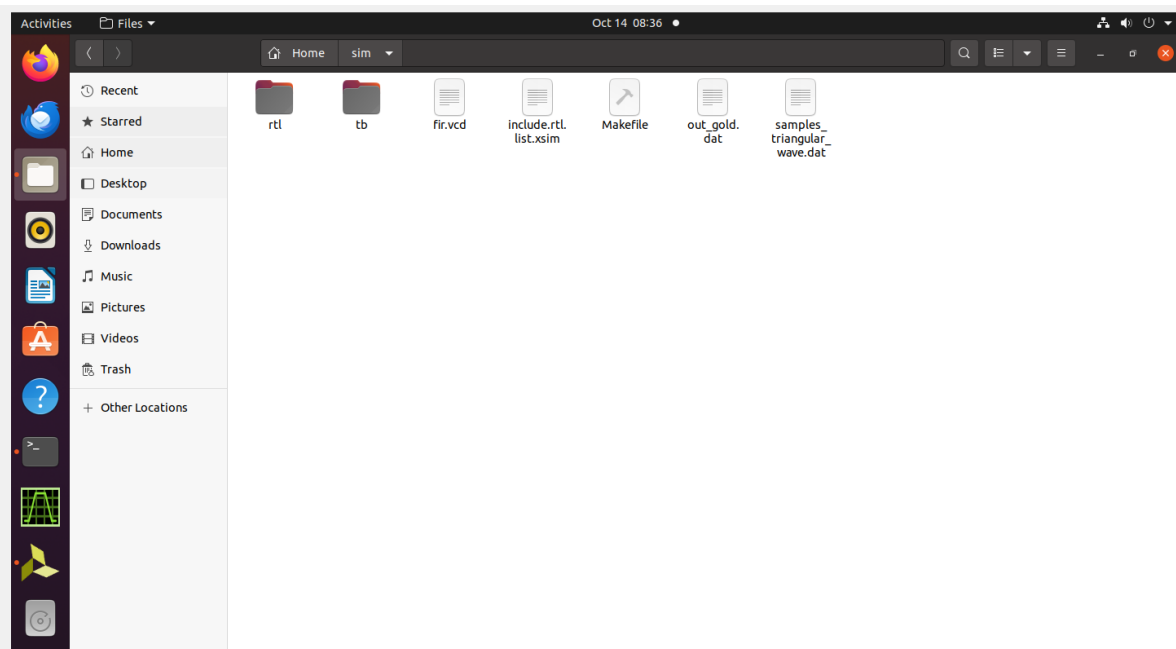
- **1.5.2 Run Simulation**

- **【左鍵點擊Run Simulation，點擊Run Behavioral Simulation】**

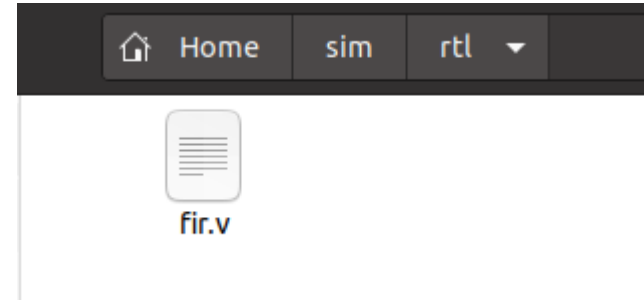
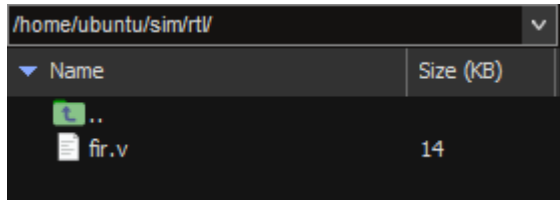


2. Implement Flow (Makefile)

- 2.1. Makefile
 - 【施作環境為 Linux】
 - 可以透過MobaXterm或是Ubuntu執行



- 2.2 Add the design sources to rtl folder



- 2.3 Add the design sources to `include.rtl.list.xsim`
 - 【將設計檔的路徑寫入`include.rtl.list.xsim`】

```
include.rtl.list.xsim X
C: > Users > Bill > AppData > Roaming > MobaXterm > slash > RemoteFiles > 2492622_2_1 > include.rtl.list.xsim
1 # design sources
2 ./rtl/fir.v
```


- 2.4 Run the makefile
 - Under the directory of Makefile
 - Command **make**

