

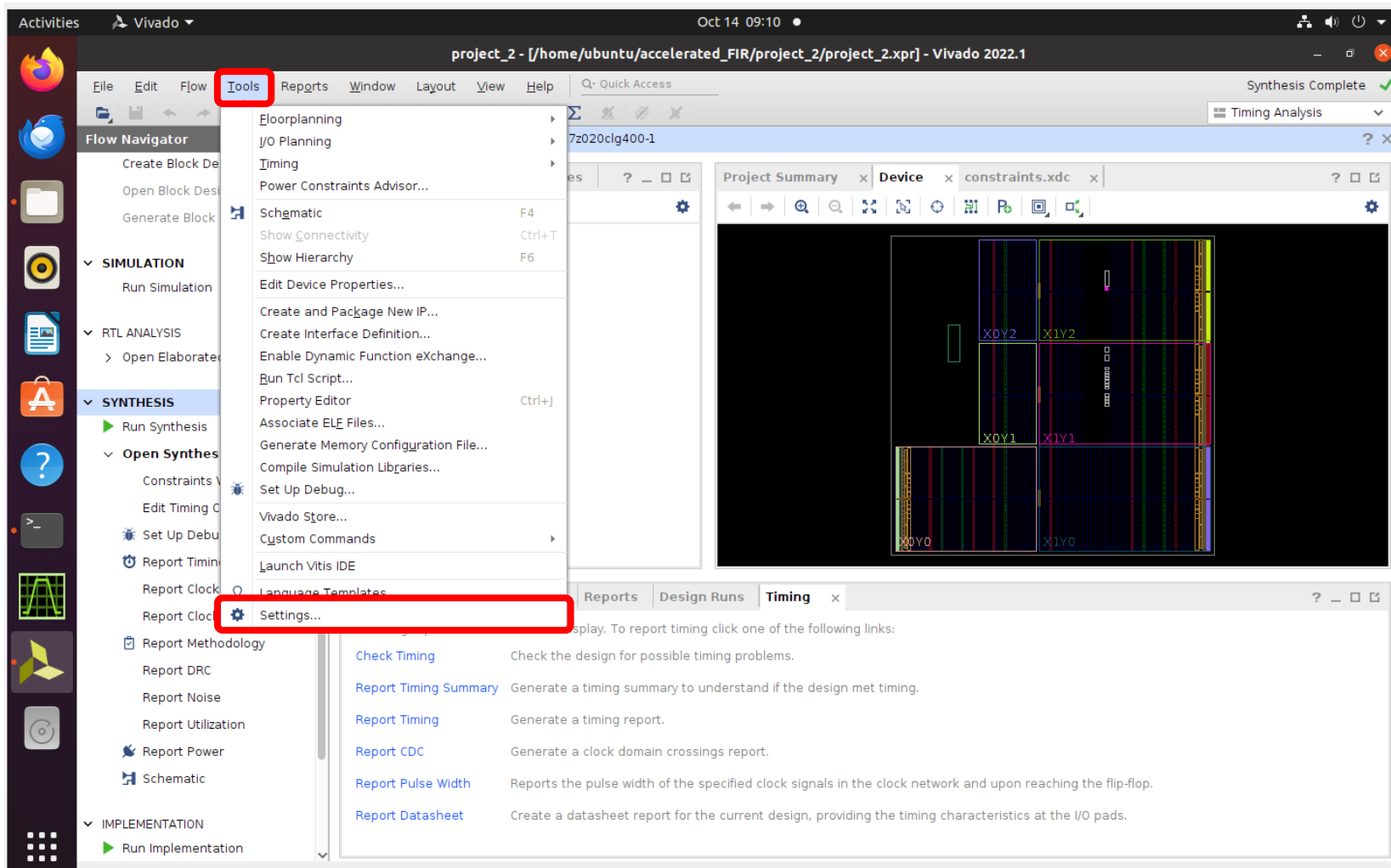
# Synthesis Guide

SOC Design

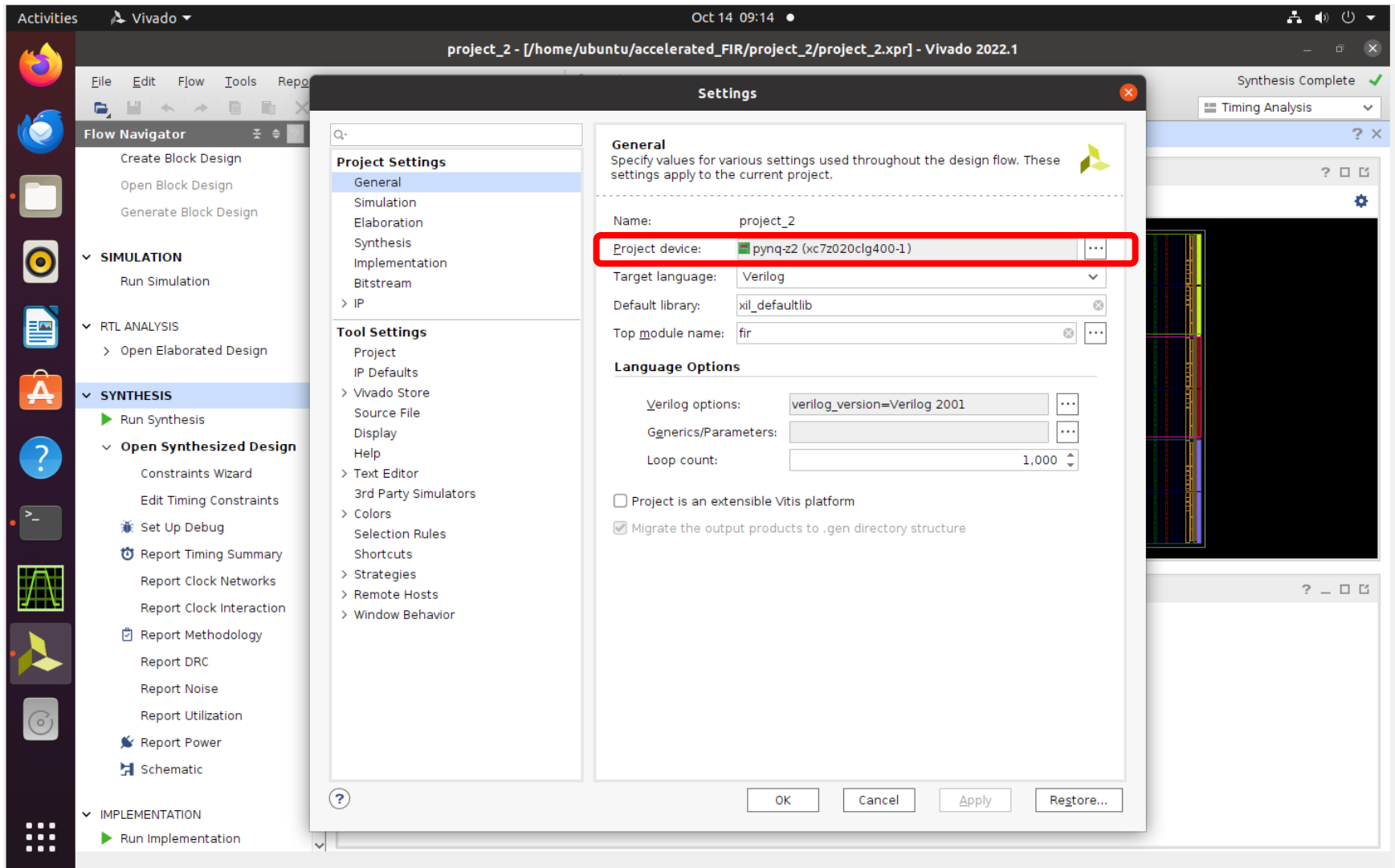
# Synthesis Guide

- **We synthesis under 【 Vivado GUI 】**
- You need to select the FPGA for Synthesis
  - Follow up the SIM\_Workflow to select FPGA Board
  - Edit FPGA Board in the project

- 0. Select FPGA board
- 0.1. 左鍵點擊 Tools ，並且點擊Settings



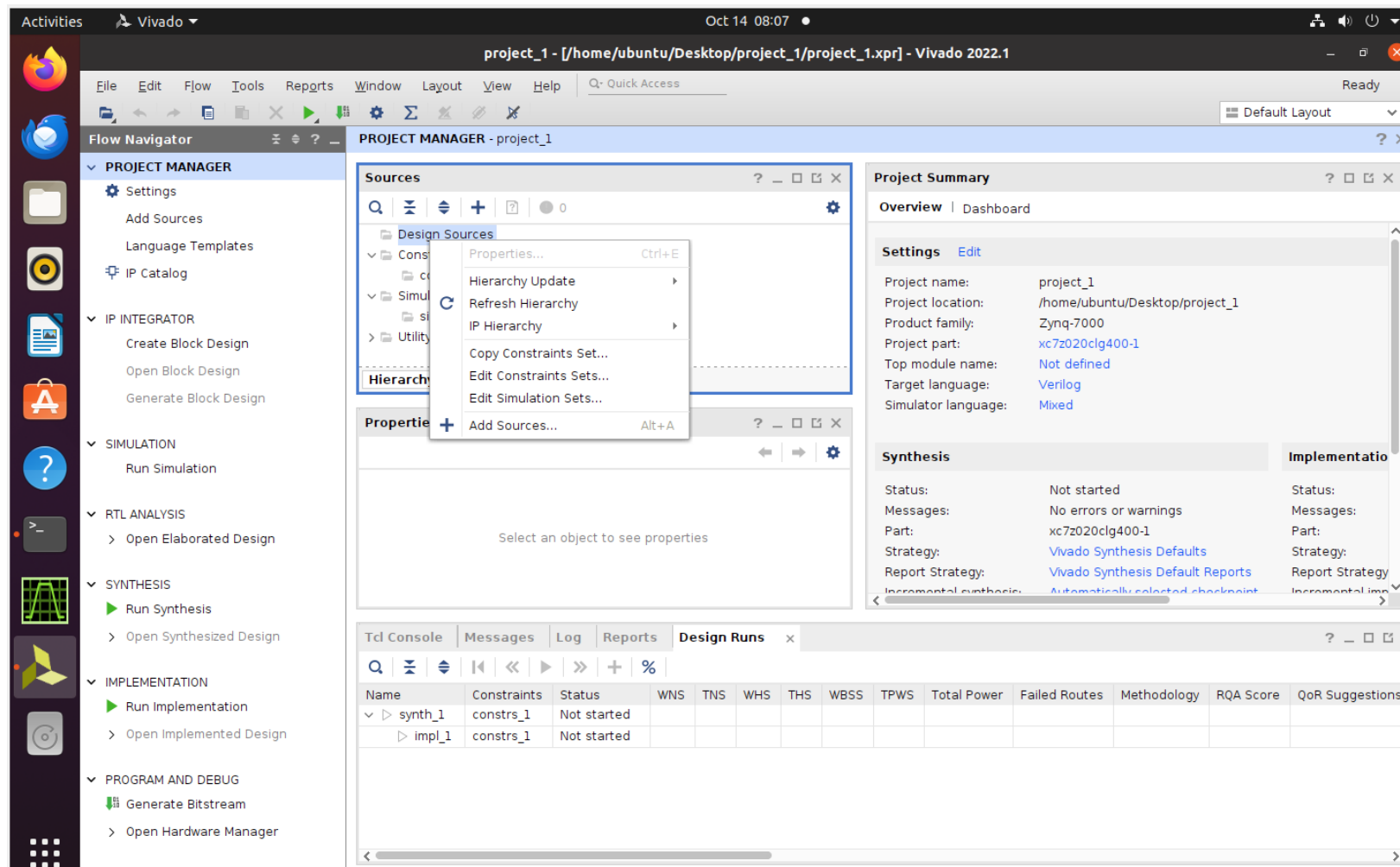
- 0.2. Modify Project Device
  - Select PYNQ-Z2 (xc7z020clg400-1)



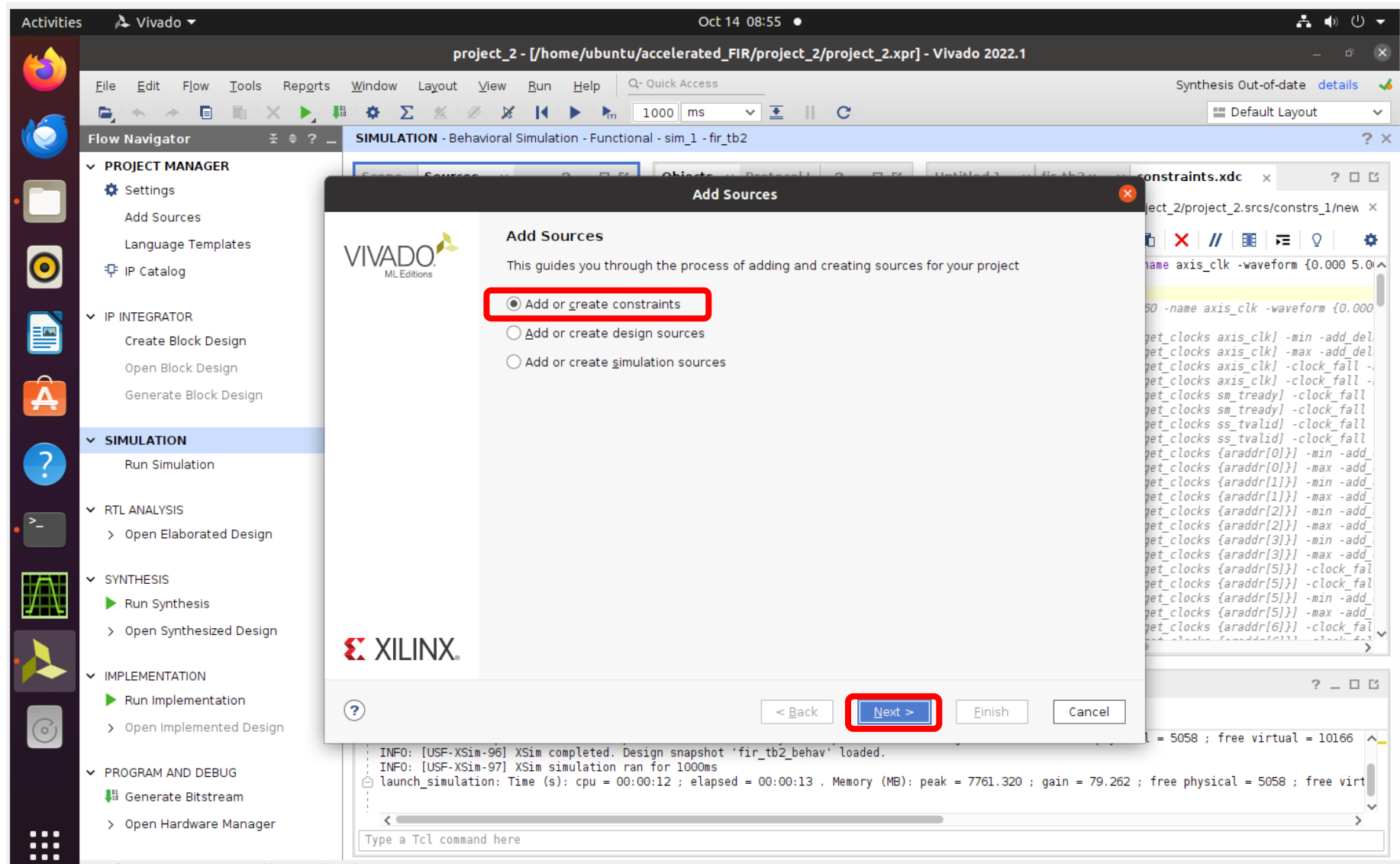
- **1.1 Add Constraints**

- **1.1.1 Add Sources**

- **【右鍵點擊Design Sources，選擇Add Sources】**

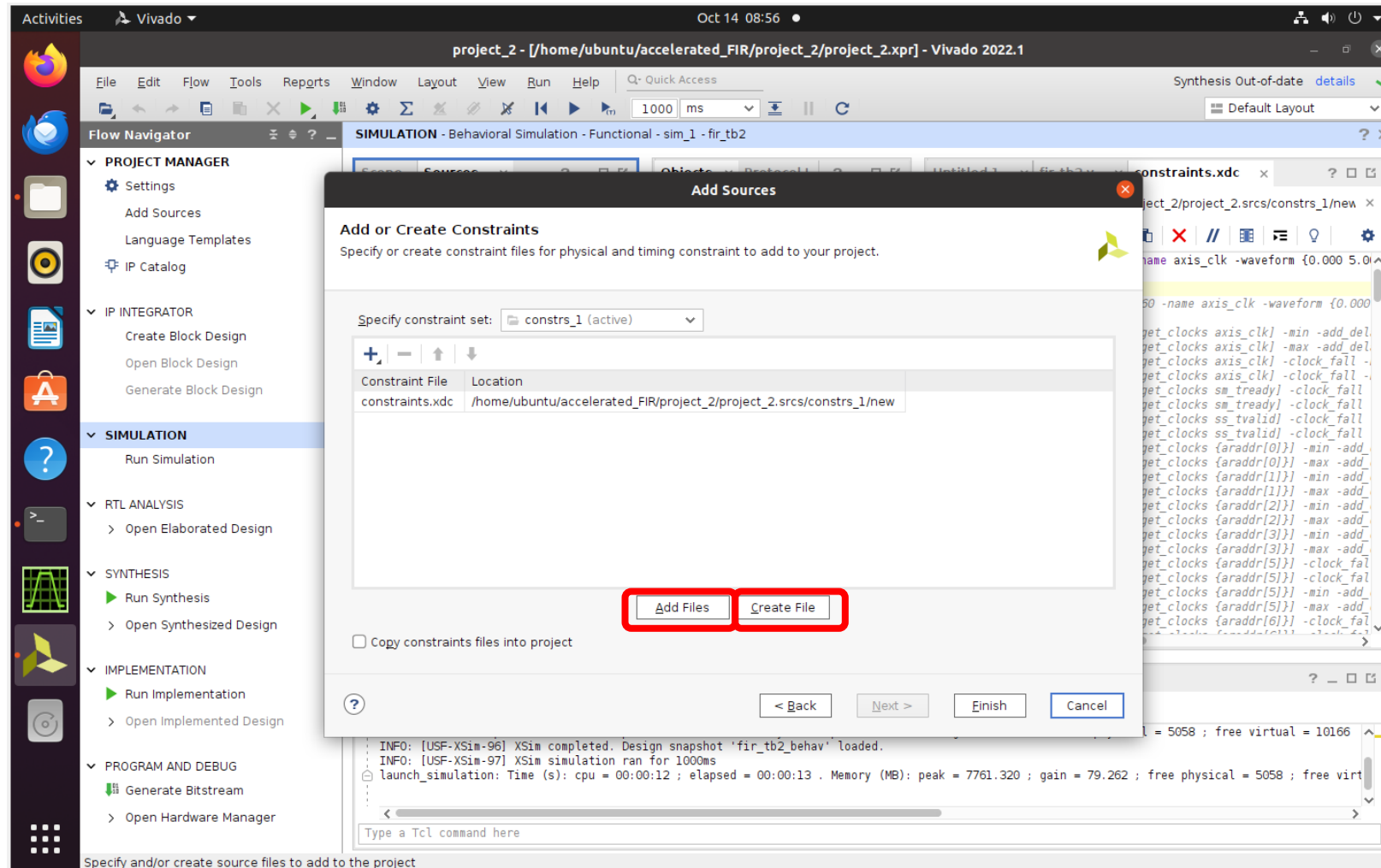


- 1.1.2 Add or Create constraints
  - 【選取Add or Create constraints】



## • 1.1.3 Add Files

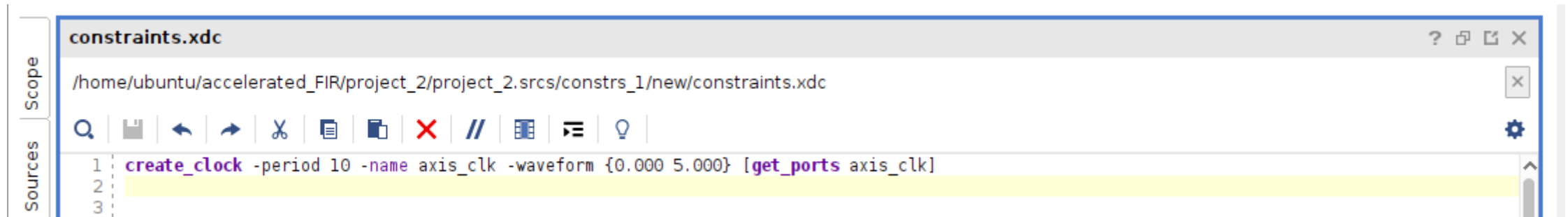
- 【如果已有Constraints，選取Add files】
- 【如果沒有Constraints，選取Create file】



- 1.2 Modify Clock Constraints

- 1.2.1 設定Clock 的Constraints

- `create_clock -period period_time -name axis_clk -waveform {Rise_time Fall_time} [get_ports axis_clk]`

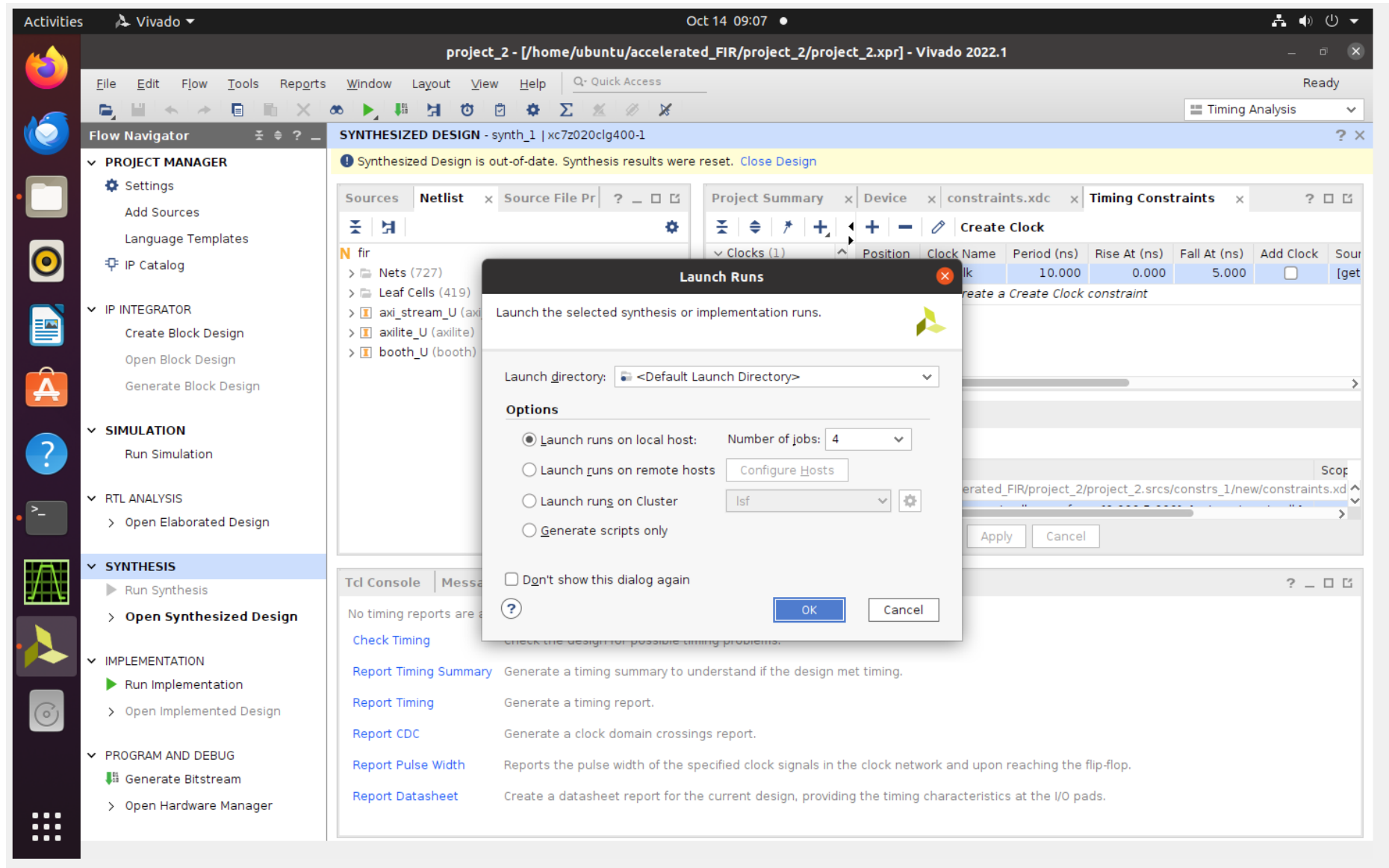


The screenshot shows a code editor window titled "constraints.xdc" with the file path "/home/ubuntu/accelerated\_FIR/project\_2/project\_2.srscs/constrs\_1/new/constraints.xdc". The editor contains a single line of code: `create_clock -period 10 -name axis_clk -waveform {0.000 5.000} [get_ports axis_clk]`. The code is syntax-highlighted, with "create\_clock" in purple, "-period 10" in black, "-name axis\_clk" in purple, "-waveform {0.000 5.000}" in black, and "[get\_ports axis\_clk]" in purple. The line is highlighted in yellow. The left sidebar shows "Sources" and "Scope" tabs. The bottom of the editor shows line numbers 1, 2, and 3.

```
constraints.xdc
/home/ubuntu/accelerated_FIR/project_2/project_2.srscs/constrs_1/new/constraints.xdc
1 create_clock -period 10 -name axis_clk -waveform {0.000 5.000} [get_ports axis_clk]
2
3
```



## • 1.2.2 Run Synthesis



## • 1.2.3 Report Timing Summary

The screenshot displays the Vivado 2022.1 IDE interface. The top status bar indicates 'Synthesis Complete' with a green checkmark. The 'Timing Analysis' dropdown is visible in the top right. The left sidebar shows the 'Flow Navigator' with the 'SYNTHESIS' section expanded. The 'Report Timing Summary' option is highlighted with a red rectangle. The main workspace shows the 'SYNTHESIZED DESIGN - synth\_1 | xc7z020clg400-1' project. The 'Netlist' tab is active, showing a hierarchy of components: fir, Nets (727), Leaf Cells (419), axi\_stream\_U (axi\_stream), axilite\_U (axilite), and booth\_U (booth). The 'Project Summary' tab is also visible, showing a timing diagram with signals X0Y0, X0Y1, X0Y2, X1Y0, and X1Y1. The bottom status bar shows the 'Timing' tab selected, displaying a message: 'No timing reports are available for display. To report timing click one of the following links: Check Timing, Report Timing Summary, Report Timing, Report CDC, Report Pulse Width, Report Datasheet.'

Activities | Vivado | Oct 14 09:15

project\_2 - [/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr] - Vivado 2022.1

File Edit Flow Tools Reports Window Layout View Help | Quick Access

Synthesis Complete ✓

Timing Analysis

Flow Navigator

- Create Block Design
- Open Block Design
- Generate Block Design
- SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design**
    - Constraints Wizard
    - Edit Timing Constraints
    - Set Up Debug
    - Report Timing Summary**
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- IMPLEMENTATION
  - Run Implementation

SYNTHESIZED DESIGN - synth\_1 | xc7z020clg400-1

Sources Netlist Properties

fir

- > Nets (727)
- > Leaf Cells (419)
- > axi\_stream\_U (axi\_stream)
- > axilite\_U (axilite)
- > booth\_U (booth)

Project Summary Device constraints.xdc

Timing diagram showing signals X0Y0, X0Y1, X0Y2, X1Y0, and X1Y1.

Tcl Console Messages Log Reports Design Runs Timing

No timing reports are available for display. To report timing click one of the following links:

- [Check Timing](#) Check the design for possible timing problems.
- [Report Timing Summary](#) Generate a timing summary to understand if the design met timing.
- [Report Timing](#) Generate a timing report.
- [Report CDC](#) Generate a clock domain crossings report.
- [Report Pulse Width](#) Reports the pulse width of the specified clock signals in the clock network and upon reaching the flip-flop.
- [Report Datasheet](#) Create a datasheet report for the current design, providing the timing characteristics at the I/O pads.

- Export to timing summary file

The screenshot shows the Vivado 2022.1 IDE interface. The top bar indicates the project is 'project\_2' located at '[/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr]'. The 'Synthesis Complete' status is shown in the top right. The 'Timing Analysis' dropdown is visible. The 'Flow Navigator' on the left shows the project structure, with 'SYNTHESIS' selected. The 'Report Timing Summary' dialog box is open, displaying the 'Options' tab. The 'Results name' is 'timing\_1'. The 'Report' section has 'Show input pins in path' and 'Report number of routable nets' checked. The 'File Output' section has 'Export to file:' checked and highlighted with a red rectangle. The 'Command' field at the bottom contains the command: 'report\_timing\_summary -delay\_type min\_max -report\_unconstrained -check\_timing\_verbose -max\_paths 10 -input\_pins -routable\_nets -name timing\_1'. The 'OK' and 'Cancel' buttons are at the bottom right.

Report Timing Summary

Generate a timing summary to understand if the design met timing.

Results name: timing\_1

Options Advanced Timer Settings

**Report**

- ☐ Report from cells:
- ☒ Show input pins in path
- ☒ Report number of routable nets
- ☐ Report unique pins

**File Output**

- ☒ Export to file:
- ☐ Interactive report file:

**Miscellaneous**

- ☐ Ignore command errors (quiet mode)
- ☐ Suspend message limits during command execution

**Command:** report\_timing\_summary -delay\_type min\_max -report\_unconstrained -check\_timing\_verbose -max\_paths 10 -input\_pins -routable\_nets -name timing\_1

☒ Open in a new tab

☐ Open in Timing Analysis layout

OK Cancel

- 1.2.4 Check the Design Timing Summary
  - Slack time has to be positive integer

The screenshot shows the Vivado 2022.1 IDE interface. The top bar indicates the project is 'project\_2' located at '[/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr]'. The 'Synthesis Complete' status is shown with a green checkmark. The 'Timing Analysis' dropdown is visible in the top right.

The left sidebar contains the 'Flow Navigator' with the following sections:

- Create Block Design
- Open Block Design
- Generate Block Design
- SIMULATION**
  - Run Simulation
- RTL ANALYSIS**
  - Open Elaborated Design
- SYNTHESIS**
  - Run Synthesis
  - Open Synthesized Design**
    - Constraints Wizard
    - Edit Timing Constraints
    - Set Up Debug
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- IMPLEMENTATION
  - Run Implementation

The main workspace displays the 'SYNTHESIZED DESIGN - synth\_1 | xc7z020clg400-1'. The 'Netlist' tab is active, showing a hierarchy of components: fir, Nets (727), Leaf Cells (419), axi\_stream\_U (axi\_stream), axilite\_U (axilite), and booth\_U (booth).

The 'Timing' tab is selected in the bottom panel, showing the 'Design Timing Summary' report. The report is highlighted with a red rectangle. The summary includes the following data:

Setup		Hold	Pulse Width		
Worst Negative Slack (WNS):	4.146 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	370	Total Number of Endpoints:	370	Total Number of Endpoints:	

The report concludes with the statement: **User specified timing constraints are met.**

## • 1.2.5 Edit Timing Constraints

- If there is **negative** slack time, you need to increase timing constraints

The screenshot displays the Vivado 2022.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The title bar shows the project path: project\_2 - [/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr] - Vivado 2022.1. The status bar indicates 'Synthesis Complete' and 'Timing Analysis'.

The left sidebar contains the Flow Navigator with options like 'Create Block Design', 'Open Block Design', and 'Generate Block Design'. The 'SYNTHESIS' section is expanded, showing 'Run Synthesis', 'Open Synthesized Design', 'Constraints Wizard', 'Edit Timing Constraints', 'Set Up Debug', 'Report Timing Summary', 'Report Clock Networks', 'Report Clock Interaction', 'Report Methodology', 'Report DRC', 'Report Noise', 'Report Utilization', 'Report Power', and 'Schematic'.

The main workspace is divided into several panes. The 'Sources' pane shows the project hierarchy: fir, Nets (727), Leaf Cells (419), axi\_stream\_U (axi\_stream), axilite\_U (axilite), and booth\_U (booth). The 'Project Summary' pane displays project details: Project name: project\_2, Project location: /home/ubuntu/accelerated\_FIR/project\_2, Product family: Zynq-7000, Project part: pynq-z2 (xc7z020clg400-1), Top module name: fir, Target language: Verilog, and Simulator language: Mixed. The 'Board Part' section shows Display name: pynq-z2, Board part name: tul.com.tw:pynq-z2:part0:1.0, Board revision: 1.0, and Connectors: No connections.

The 'Timing' pane is active, showing the 'Design Timing Summary' table. The table is divided into three columns: Setup, Hold, and Pulse Width. The 'Setup' column shows Worst Negative Slack (WNS) as -0.854 ns, Total Negative Slack (TNS) as -4.456 ns, and Number of Failing Endpoints as 14. The 'Hold' column shows Worst Hold Slack (WHS) as 0.142 ns, Total Hold Slack (THS) as 0.000 ns, and Number of Failing Endpoints as 0. The 'Pulse Width' column shows Worst Pulse Width Slack (WPWS) as 0.000 ns, Total Pulse Width Negative Slack (TPWS) as 0.000 ns, and Number of Failing Endpoints as 0. The table also shows the Total Number of Endpoints as 370 for all three categories. A red box highlights the 'Setup' and 'Hold' columns, and a message at the bottom states 'Timing constraints are not met.'

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -0.854 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 0.000 ns
Total Negative Slack (TNS): -4.456 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 14	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 370	Total Number of Endpoints: 370	Total Number of Endpoints: 370

Timing constraints are not met.

- Edit the axis\_clk constraints, then re-run the timing summary.

The screenshot displays the Vivado 2022.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The title bar shows the project name 'project\_2' and the path '/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr'. The left sidebar contains the Flow Navigator, which is currently set to 'SYNTHESIS'. The 'Edit Timing Constraints' option is highlighted with a red rectangle. The main workspace is divided into several panes. The 'Sources' pane on the left shows the project hierarchy, including 'fir', 'Nets (727)', 'Leaf Cells (419)', and various components like 'axi\_stream\_U', 'axilite\_U', and 'booth\_U'. The 'Timing Constraints' pane on the right shows a table of constraints. A red rectangle highlights the 'Create Clock' button and the 'axis\_clk' constraint entry. The 'All Constraints' pane below it shows the command 'create\_clock -period 5.000 -name axis\_clk -waveform {0.000 2.500} [get\_ports axis\_clk]'. The bottom pane shows the 'Timing Summary' report, which includes a table of timing metrics and a warning that 'Timing constraints are not met.'.

Activities Vivado Oct 14 09:23

project\_2 - [/home/ubuntu/accelerated\_FIR/project\_2/project\_2.xpr] - Vivado 2022.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Synthesis Complete ✓

Timing Analysis

Flow Navigator

- Create Block Design
- Open Block Design
- Generate Block Design

▼ SIMULATION

- Run Simulation

▼ RTL ANALYSIS

- Open Elaborated Design

▼ SYNTHESIS

- Run Synthesis
- Open Synthesized Design
  - Constraints Wizard
  - Edit Timing Constraints**
  - Set Up Debug
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic
- Run Implementation

SYNTHESIZED DESIGN \* - synth\_1 | xc7z020clg400-1

Sources Netlist Properties

N fir

- > Nets (727)
- > Leaf Cells (419)
- > axi\_stream\_U (axi\_stream)
- > axilite\_U (axilite)
- > booth\_U (booth)

Project Summary Device constraints.xdc Timing Constraints

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source
1	axis_clk	5.000	0.000	2.500	<input type="checkbox"/>	[get_ports axis_clk]

Double click to create a Create Clock constraint

All Constraints

Position Command Scope

constraints.xdc (/home/ubuntu/accelerated\_FIR/project\_2/project\_2.srcs/constrs\_1/new/constraints.xdc)

1 create\_clock -period 5.000 -name axis\_clk -waveform {0.000 2.500} [get\_ports axis\_clk]

Apply Cancel

Tcl Console Messages Log Reports Design Runs Timing

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Methodology Summary

- > Check Timing (239)
- > Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Timing Summary - timing\_1

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -0.854 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS):
Total Negative Slack (TNS): -4.456 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPV):
Number of Failing Endpoints: 14	Number of Failing Endpoints: 0	Number of Failing Endpoints:
Total Number of Endpoints: 370	Total Number of Endpoints: 370	Total Number of Endpoints:

Timing constraints are not met.