SoC Design Lab1

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* Brief introduction about the overall system
  + Learn the hls flow
  + Learn how to integrate the IP from vitis\_hls to zynq
  + Learn how to generate bitstream on vivado
  + Learn how to rent the onlineFPGA
  + Learn how the kv260 read the bitstream by library of overlay
  + Learn how to write code on OnlineFPGA by Jupyter
* **What is observed & learned**

In this lab, I try may way to install vitis\_hls ubuntu which run on the docker.

I try the version of 2022.1、2022.2、2023.1. They can be install well but it will have error when I run the co-simulation. This error log is tool bug which I find the comment from the website. So I try may version of vitis\_hls.

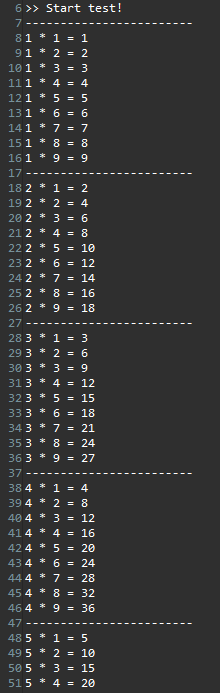
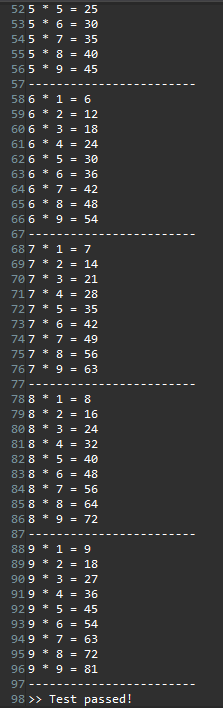
Finally, I still install the tool 2022.1 on my windows, the error does not happen again.

From this lab, I go through the basic flow of HLS by C++ to a Vivado IP. In this process, I simulation my c++ code, try to synthesis the design, co-simulation design and testbench and finally export the Verilog IP. In each step, I try to find some information from the report to understand the implementation view the design not just the abstractive view of c++ code.

And also I never view the summary report from Solution1->syn->report->multip\_2num\_csynth.rpt. It is more detail than Flow Navigator-> C SYNTHESIS-> Report & Viewers->Report.

And I learned the flow of hls and integrate to the vivado design. Generating bitstream and upload to the FPGA. The FPGA can control online. I upload the bitstream and edit the python code on Jupyter. I adjust the related file path and compile the code to get the python code result by hw design.

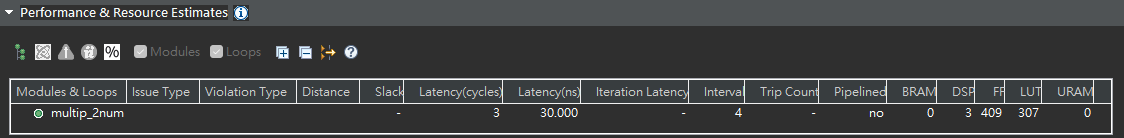
* **C Simulation Result**

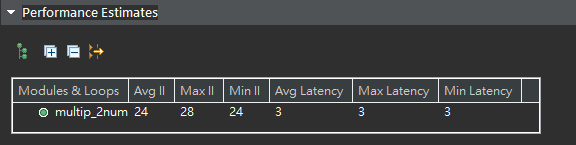
 

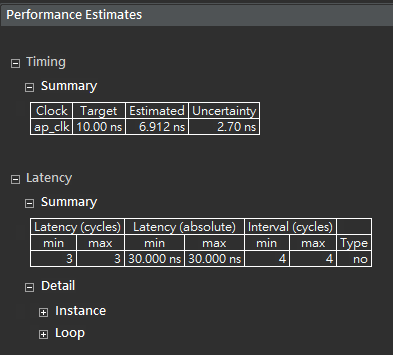
* **Performance**:

FF: 409

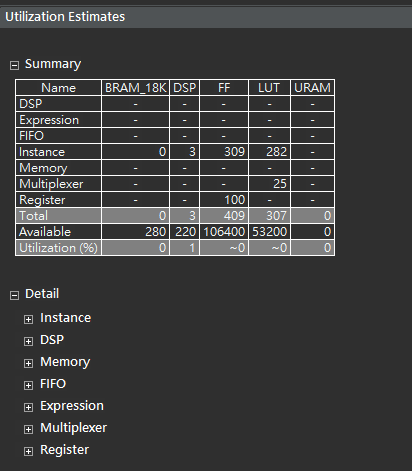
LUT: 307



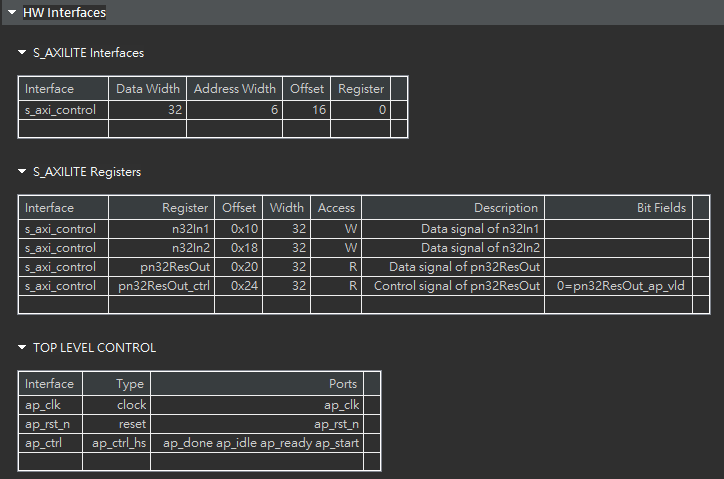


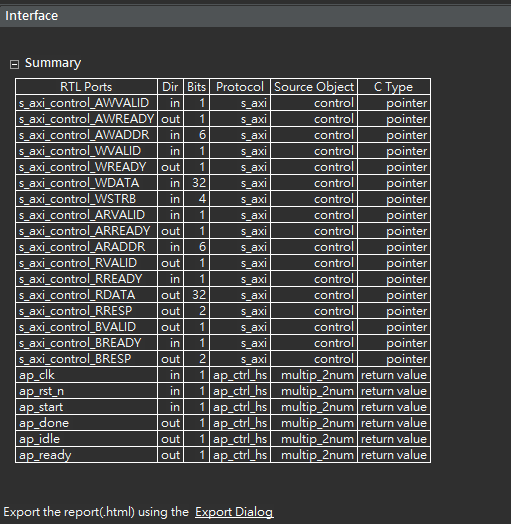


* **Utilization**

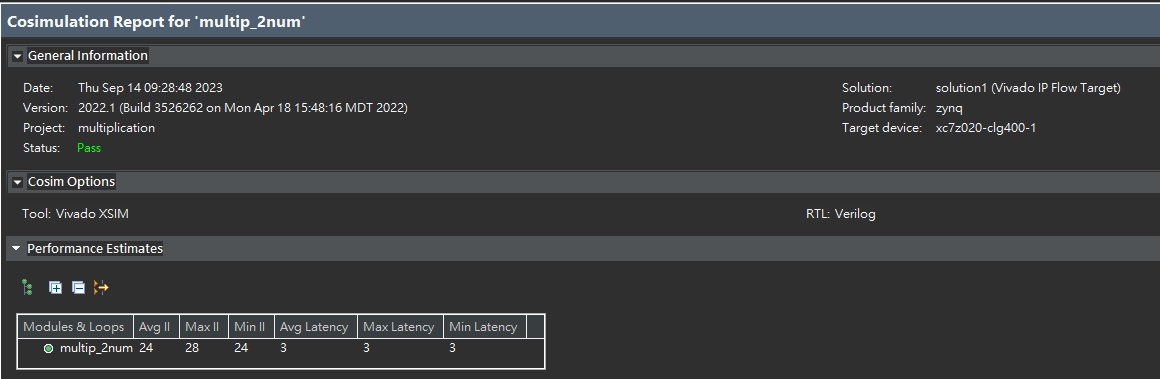


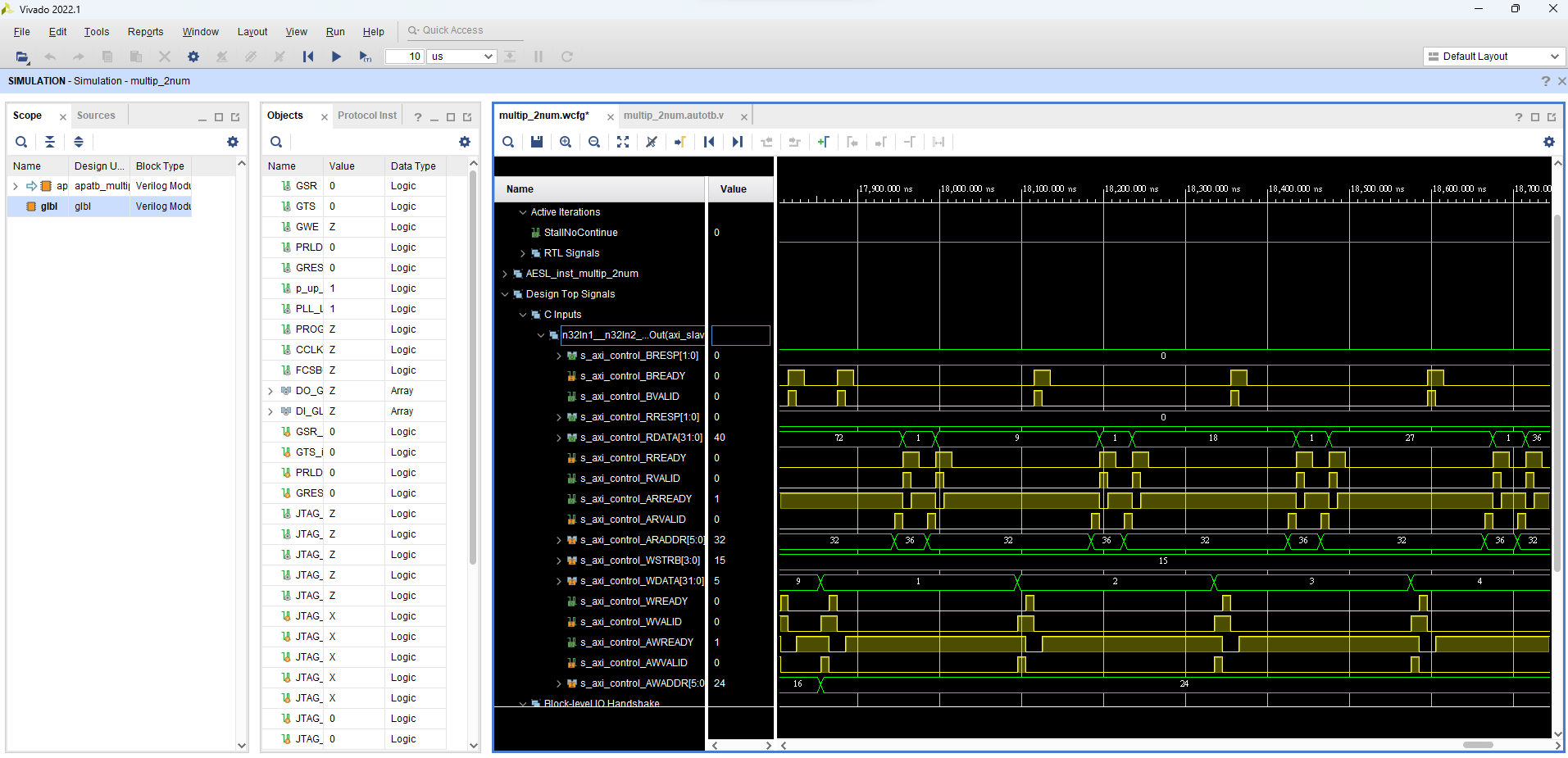
* **Interface**





* Co-simulation transcript/Waveform





* **Jupyter Notebook execution results**

