SoC Design Lab2

Institute of Electronics,

National Yang Ming Chiao Tung University

412510020 高振翔

* **Brief introduction about the overall system**

We use hls to design a FIR hardware. We try to add MAXI and Stream interface to the ZYNQ. The interface is created by hls but we have to connect ZYNQ by adding HP Slave AXI Interface. If all the connection is done, we should generate bitstream and upload it to the FPGA. We use python code the send the input data of samples\_triangular\_wave, n32Taps and length of data. And we get back fir result to compare with golden data. The filter will change a little the waveform, but we still can see the triangle.

* **What is observed & learned**
* Differences between MAXI and Stream interface

By using Stream interface, we add the DMA ip beyond and behind our FIR IP.

We can see the python code result, the kernel execution time of Stream is larger than MAXI.

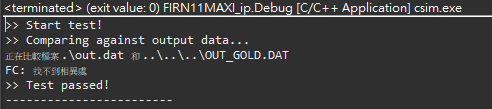
* Differences between csim and cosim

For the cosim, the simulation use the synthesis result to run the testbench. It will spend more time than csim which totally software simulation. Because when we run the cosim, it should do synthesis first.

For the cosim report, the avg latency of Stream is larger than MAXI.

# FIRN11MAXI/

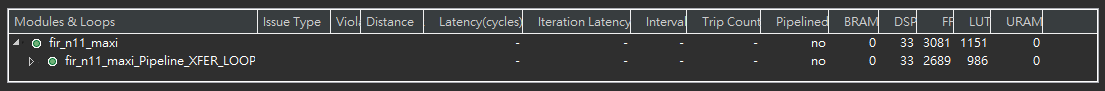
* **C Simulation Result**

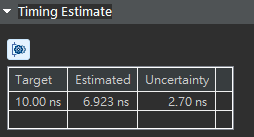


* **Performance**:

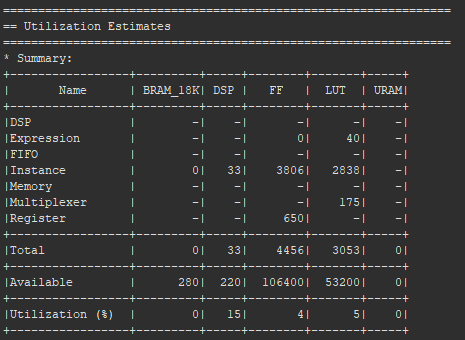
FF: 3081

LUT: 1151

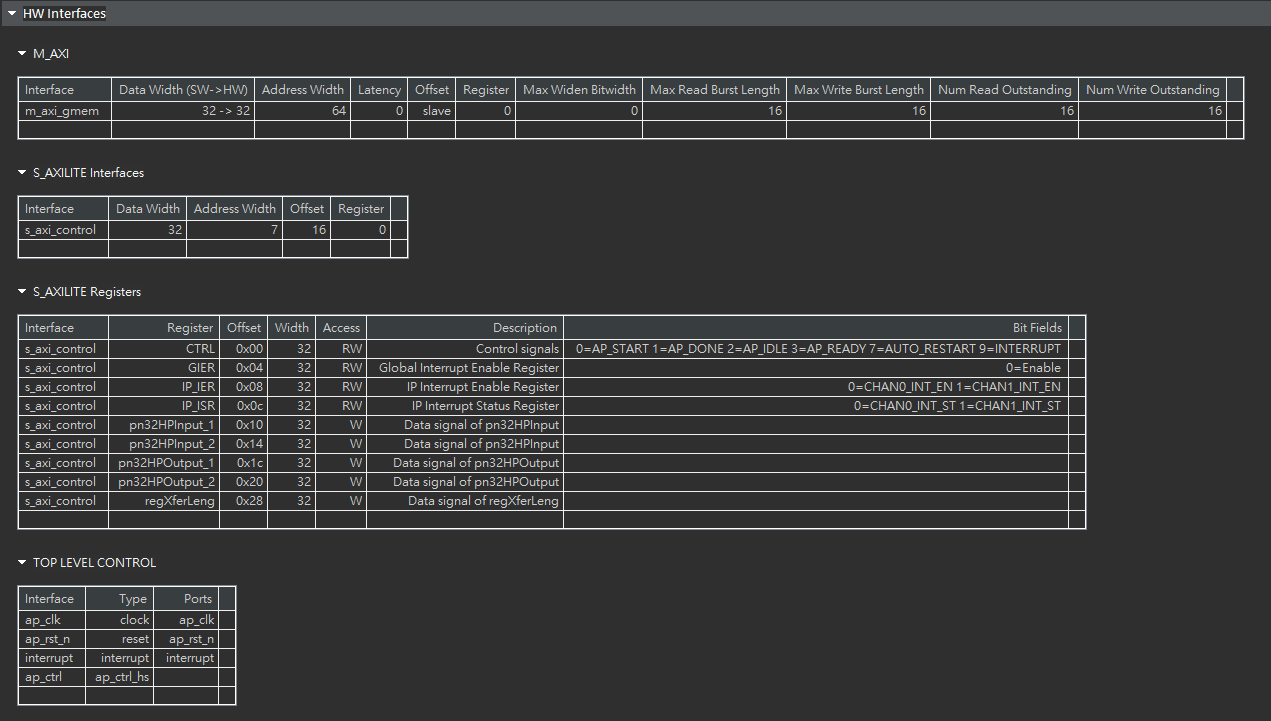




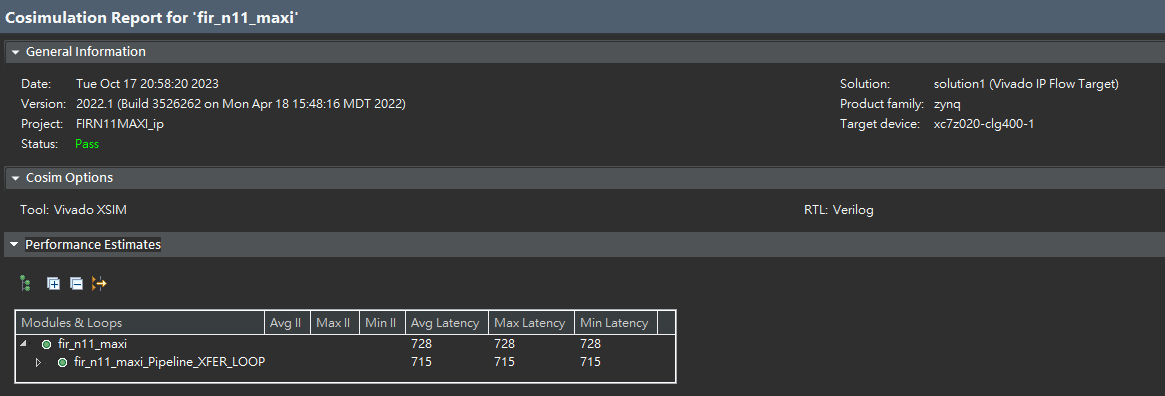
* **Utilization**

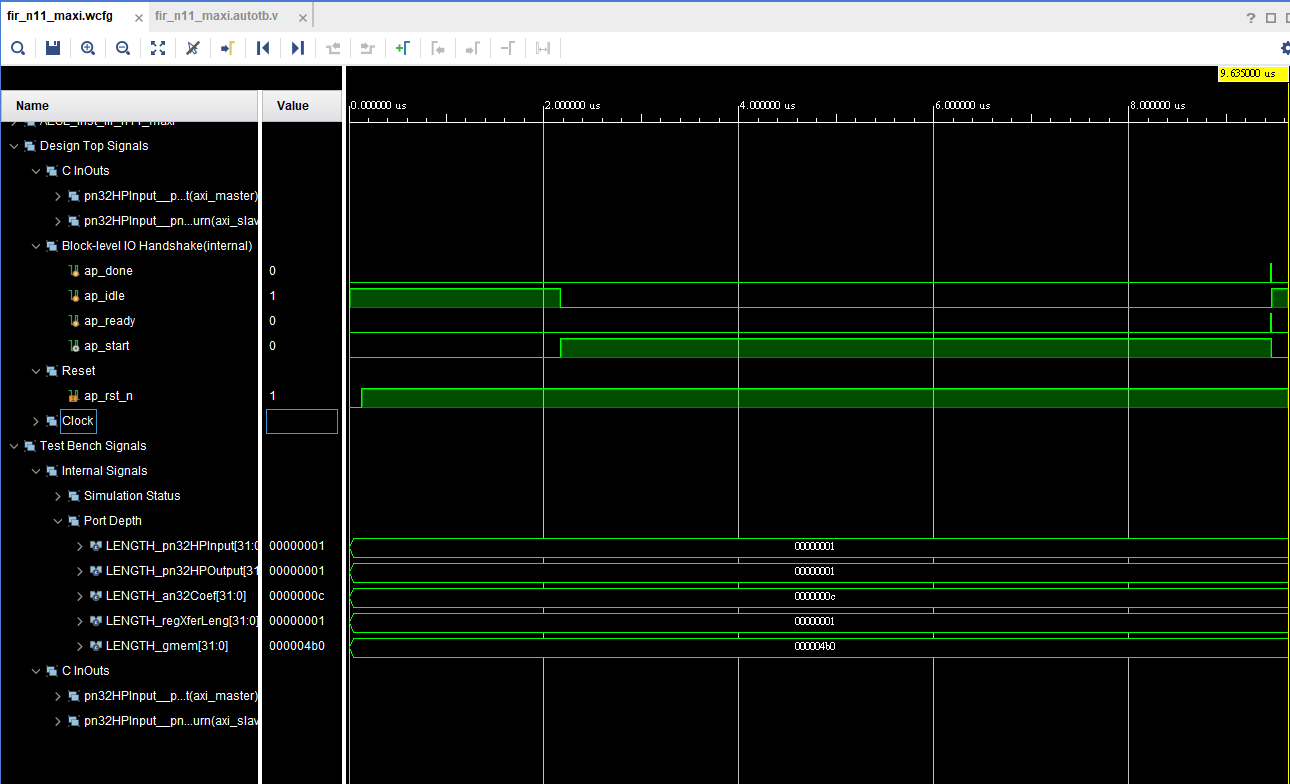


* **Interface**

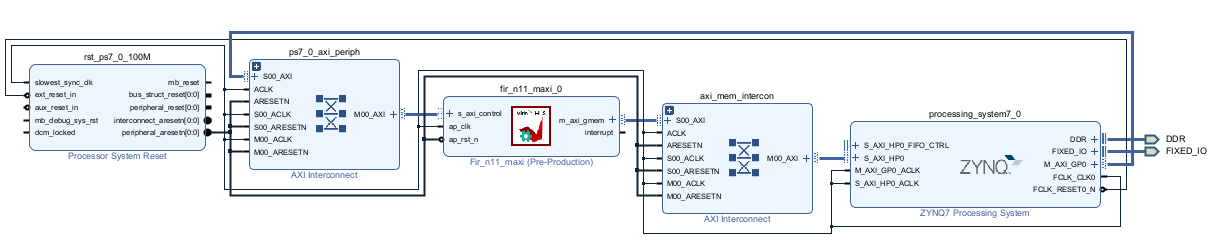


* Co-simulation transcript/Waveform

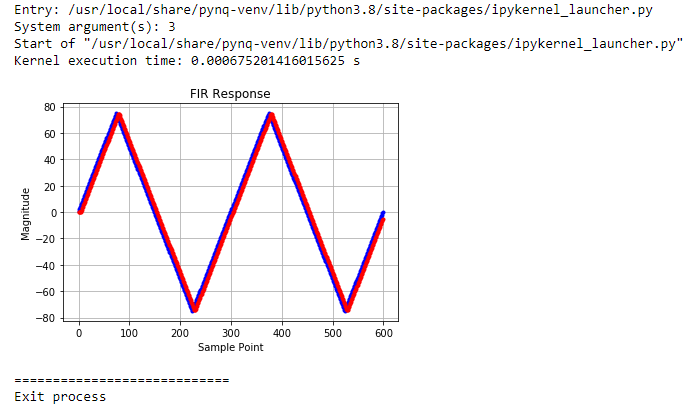




* Vivado block desgin

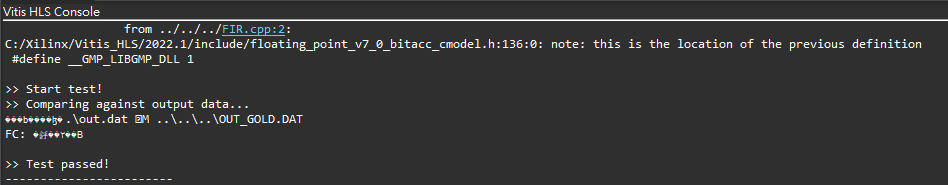


* **Jupyter Notebook execution results**



# FIRN11Stream/

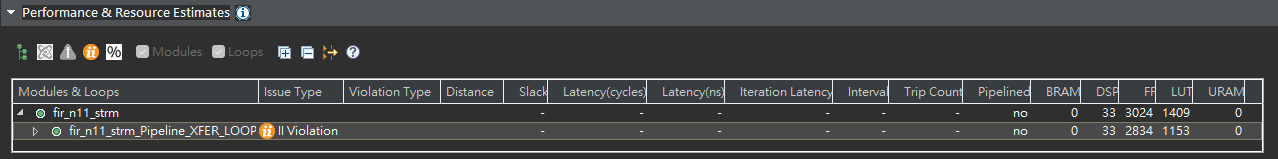
* **C Simulation Result**

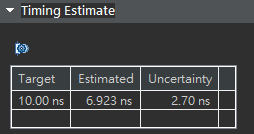


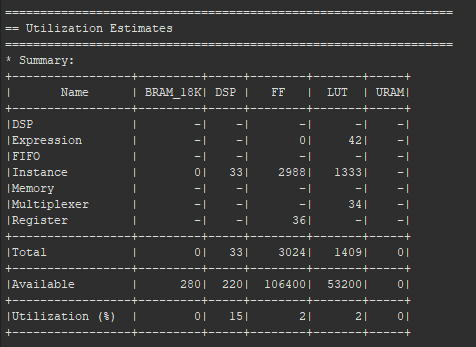
* **Performance**、**Utilization**

FF: 3024

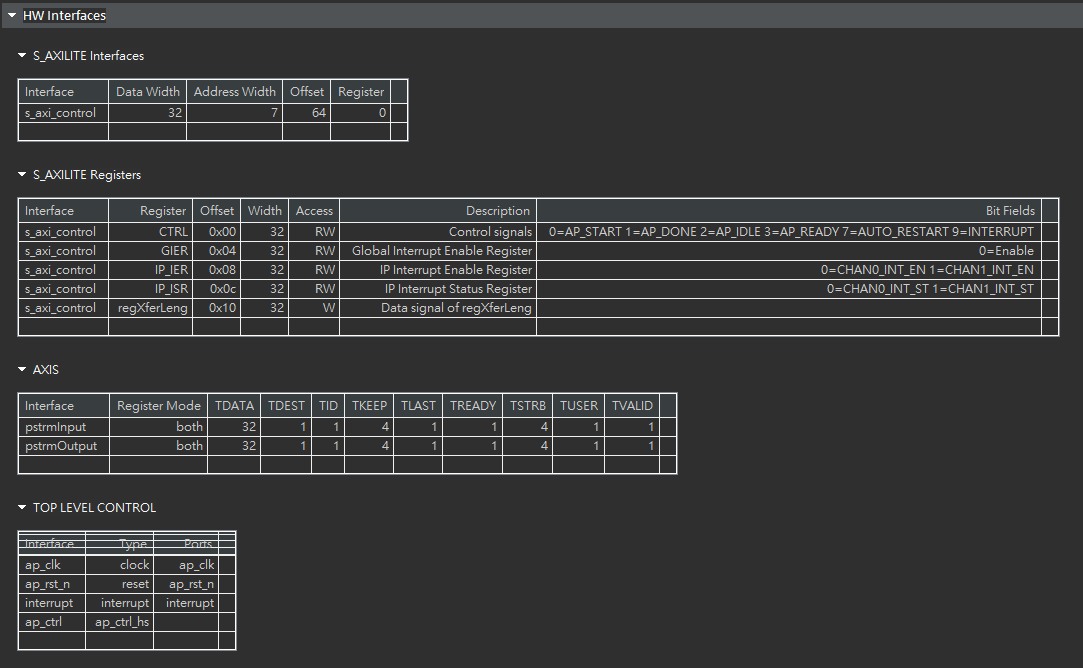
LUT: 1409



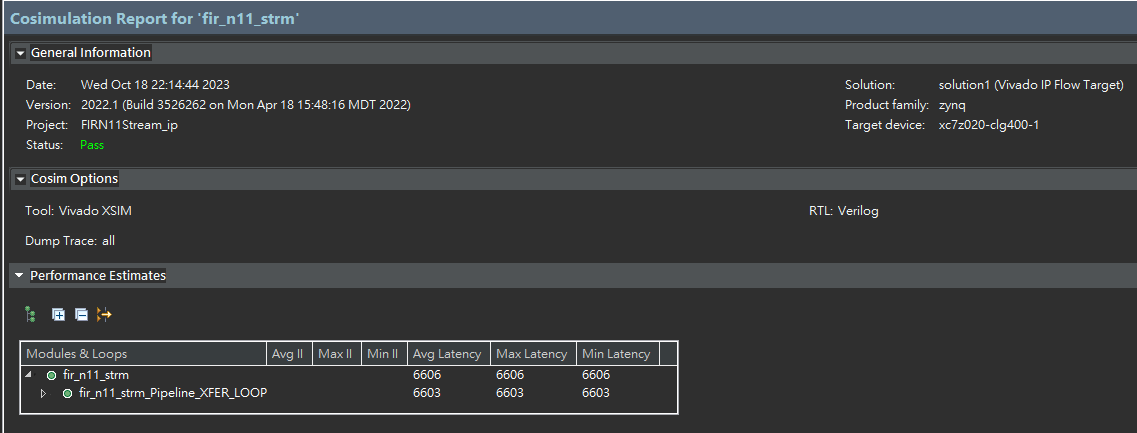


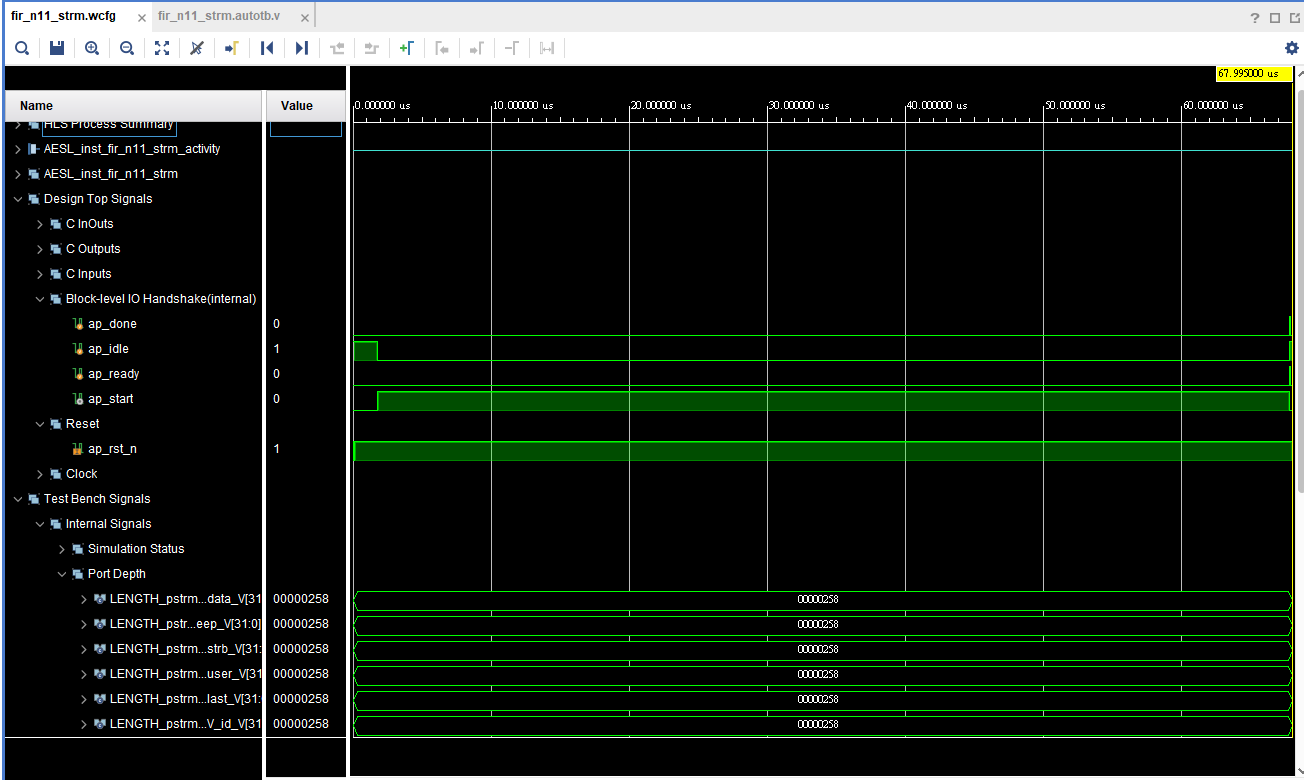


* **Interface**



* Co-simulation transcript/Waveform

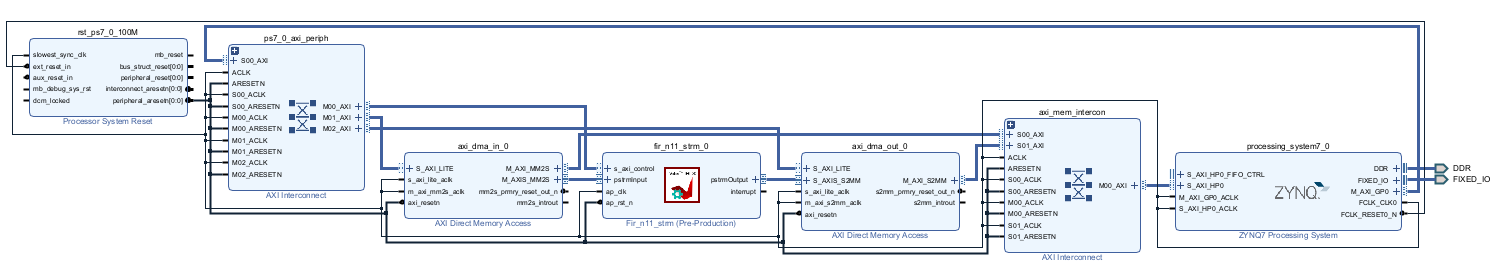


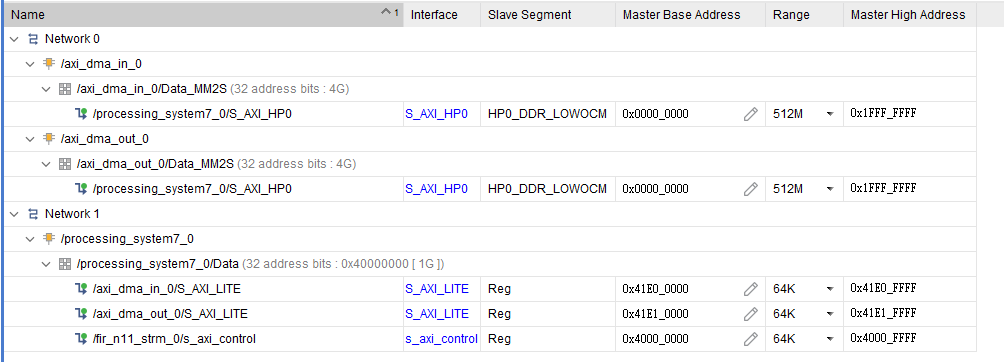


* Vivado block desgin

**FIR\_N11\_STRM**的**pstrminput**接到**axi\_dma\_in\_0**的**M\_AXIS\_MM2S**

**FIR\_N11\_STRM**的**pstrmoutput**接到**axi\_dma\_out\_0**的**S\_AXIS\_S2MM**





* **Jupyter Notebook execution results**

