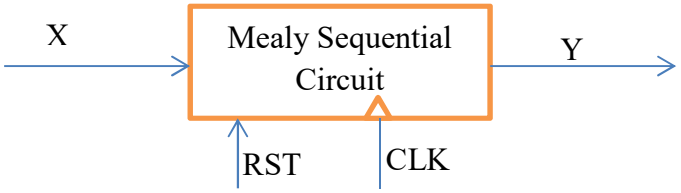
Lab #3: Mealy Sequential Circuit

1. Requirement

Design a Mealy Sequential Circuit which investigates an input sequence X and which will produce an output of Z = 1 for any input sequence ending in 1010, provided that the sequence 001 has occurred at least once. See table below for a sample set of input sequence. A reset signal RST will reset the circuit (reset the circuit to the initial state).

Input X	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	1	1
Output Y	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0



2. Pre-lab

- State graph
- State table

3. Lab

a. Design the circuit
b. Simulate using Xilinx ISE simulator

4. Deliverables

- VHDL program
- VHDL test cases
- Waveform