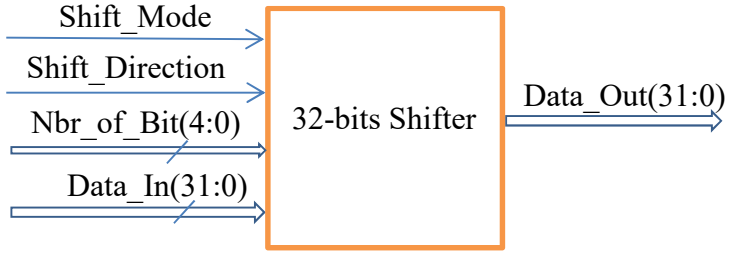
Lab #8: Design of a 32-bit Shifter

1. Requirement

Design a Shifter unit that will perform both an **arithmetic shift** and a **logical shift** of a 32-bit binary number depending on the shift mode. The shift should be identified as right or left for a certain number of given bits. Then design a test bench to verify the correctness of the design. Include enough test cases to cover all possibilities. The block diagram of this component is as below:



Shift_Mode: shift mode (arithmetic or logical shift)

Nbr_of_Bit: number of bits will be shifted

Shift_Direction: Shift left or right

The interface can be as below:

```
entity ShifterUnit_32Bits_Design is
      port(
            Shift_Mode:      in std_logic;
            Shift_Direction: in std_logic;
            Nbr_of_Bit:      in std_logic_vector(4 downto 0);
            Data_In:         in std_logic_vector(31 downto 0);
            Data_Out:        out std_logic_vector(31 downto 0)
      );
end ShifterUnit_32Bits_Design;
```

2. Pre-lab

- Study the basic operations of a logical shifter and arithmetic shifter
- Why are they important?
- What are they used for?

3. Lab

- Write the VHDL code for this unit
- Simulate using Xilinx ISE simulator

4. Deliverables

- VHDL program
- VHDL test bench with enough test cases
- Waveform with comments