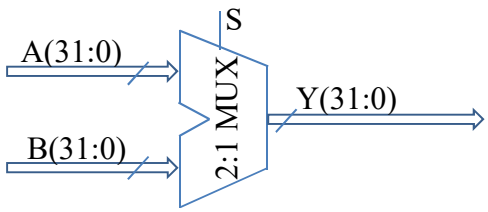
Lab #: Mux Design and Extension Unit Design

I. MUX Design

1. Requirement

Design a 32-bit 2-to-1 multiplexer using behavioral or data flow implementation style (your choice). Data inputs and output must be 32-bit vectors. Source selection is 1-bit. If source selection is 0, then source A will be selected as output, otherwise source B. The block diagram of this component is as below:



The interface can be as below:

```
entity MUX_32Bits_Design is
      port(
            S:  in std_logic;
            A:  in std_logic_vector(31 downto 0);
            B:  in std_logic_vector(31 downto 0);
            Y:  out std_logic_vector(31 downto 0)
      );
end MUX_32Bits_Design;
```

2. Pre-lab

- Study and analyze the working of a MUX (How it works and its purposes)

3. Lab

- Write the VHDL code for this MUX design
- Simulate using Xilinx ISE simulator

4. Deliverables

- VHDL program
- VHDL test bench with enough test cases
- Waveform with comments

II. Extension Unit Design

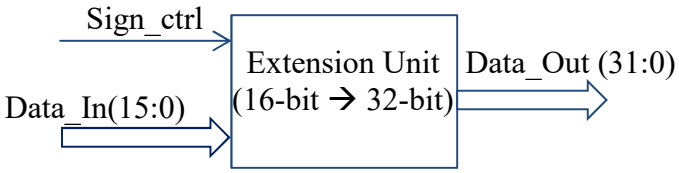
1. Requirement

Design an extension unit which can perform zero-extension or sign-extension from 16-bit binary number to 32-bit. If sign control signal is 0, then your design will perform zero-extension. If signal control signal is 1, then sign-extension will be performed.

Example of zero-extension: *X"0ABD" → X"00000ABD"*
X"7ABD" → X"00007ABD"
X"9DE2" → X"00009DE2"
X"8F2D" → X"00008F2D"

Example of sign-extension: *X"0ABD" → X"00000ABD"* *(positive number since MSb = '0')*
X"7ABD" → X"00007ABD" *(positive number since MSb = '0')*
X"9DE2" → X"FFFF9DE2" *(negative number since MSb = '1')*
X"8F2D" → X"FFFF8F2D" *(negative number since MSb = '1')*

The block diagram of this component is as below:



The interface can be declared as below:

```
entity ExtensionUnit_32Bits is
      port(
            Sign_Ctrl: in std_logic;
            Data_In:   in std_logic_vector(15 downto 0);
            Data_Out: out std_logic_vector(31 downto 0)
      );
end ExtensionUnit_32Bits;
```

2. Pre-lab

- Study and analyze the working of a sign extension unit in computer architecture (use lecture note (chapter 2, chapter 4) in class for your reference)

3. Lab

- Write the VHDL code for this component
- Simulate using Xilinx ISE simulator

4. Deliverables

- VHDL program
- VHDL test bench with enough test cases
- Waveform with comments