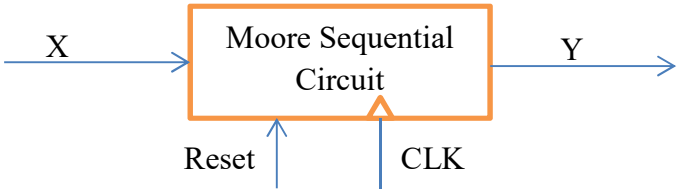
Lab #2: Moore Sequential Circuit

1. Requirement

A Moore sequential circuit has one input and one output. When the input sequence '011' occurs, the output becomes '1' and remains '1' until the sequence '011' occurs again in which the output returns to '0'. The output then remains '0' until a '011' occurs the third time etc….

Input X	0	1	0	1	1	0	1	0	1	1	0	1	0	0	1	1	1
Output Y	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1



2. Pre-lab

- State graph
- State table

3. Lab

a. Design the circuit
b. Simulate using Xilinx ISE simulator

4. Deliverables

- VHDL program
- VHDL test cases
- Waveform