Utilizing Neurons for Digital Logic Circuits: A Molecular Communications Analysis

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Abstract

With the advancement of synthetic biology, several new tools have been conceptualized over the years as alternative treatments for current medical procedures. Most of those applications are applied to various chronic diseases. This work investigates how synthetically engineered neurons can operate as digital logic gates that can be used towards bio-computing for the brain. We quantify the accuracy of logic gates under high firing rates amid a network of neurons and by how much it can smooth out uncontrolled neuronal firings. To test the efficacy of our method, simulations composed of computational models of neurons connected in a structure that represents a logic gate are performed. The simulations demonstrated the accuracy of performing the correct logic operation, and how specific properties such as the firing rate can play an important role in the accuracy. As part of the analysis, the Mean squared error is used to quantify the quality of our proposed model and predicting the accurate operation of a gate based on different sampling frequencies. As an application, the logic gates were used to trap epileptic seizures in a neuronal network, where the results demonstrated the effectiveness of reducing the firing rate. Our proposed system has the potential for computing numerous neurological conditions of the brain.

Index Terms

Logic gates, synthetic biology, nanocommunications, nanonetworks, Boolean algebra.

I. INTRODUCTION

It has been over a decade since *Molecular Communications* was introduced as a new communication paradigm aiming to conceptualize and build communication systems inspired by natural biological processes [1]–[4]. One of them is known as *neuro-spike communication* [5], where information is transferred between two neurons through electro-chemical process which triggers an electrical impulse called *action potentials*, i.e. spikes. This information can not only be encoded [6]–[11] but also modulated [12]–[14] mimicking a traditional communication system and potentially presenting itself as a tool for cognitive enhancement and treatment of neurodegenerative diseases [15], [16].

Synthetic Biology has enabled us to engineer cells that can modify or inherit new functions [17]–[19]. While the majority of focus of synthetic biology has been for prokaryotic cells, there is potential to engineer mammalian cells such as neurons and astrocytes that can be synthetically engineered to enable control of their dynamic behaviour and functionality, aiming at correction of abnormalities at a cellular level. With the advance of synthetic biology and nano-scale networks [20], many components ranging from logic gates [21]–[24] to integrated circuits such as oscillators [25] have also emerged. To date, there has not been an application of synthetic logic gates for neurological diseases.

Information processing in the brain involves the propagation of action potentials through countless numbers of specific neuronal networks. This enables the brain to process various types of information that can range from controlling the functions of organs within an organism to coding and storing long-term memory, as examples. A synchronous uncontrolled firing of spikes in large regions of the brain can occur spontaneously can can be related to neurological diseases, and one example is epilepsy [26]. Based on this, an example application of synthetic logic gates is to use them as digital filters and when positioned in between neurons as part of the network, they can play an important role in smoothing out uncontrolled neuronal firing and consequently reducing the effects of seizures. To the best of our knowledge, there are no works on neuronal logic gates that uses such models and investigate their effects in scenarios affected by neurological disorders.

In this paper, we build on top of our previous work [21] and analyze the effects of inserting neuronal logic gates in a network of neurons. The main contributions of this paper are as follows:

- **Neuronal logic gates are built, controlled and simulated within large neuronal networks using computational models of neurons** [27]. We use three models of neuron cells to create a single synthetic logic gate capable of performing logic operations at a cellular level.
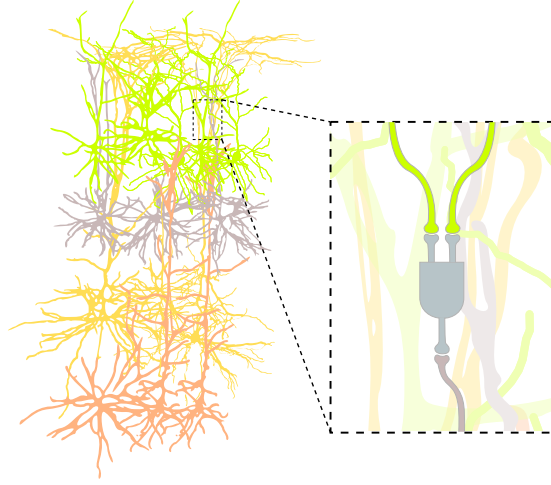
Fig. 1. Neuronal logic gate inside a cortical column.

- **Analysis of performance for the gates simulated in isolation and inside a network of neurons.** We analyze the dynamic behaviour of neuronal communications that could affect the operation of the gate and consequently the network, quantified in terms of accuracy.
- **Proposal of a queuing model for the input and gating of action potentials as units of information.** The model is capable of predicting the accuracy of the synthetic gates, and this is validated using mean squared error (MSE) as a function of the inter-spike interval (ISI) at different sampling frequencies.

The remainder of this paper is organized as follows, in Section II, a review of the current literature is provided. The construction of neuronal logic gates, their diverse types and the queue-theoretical analysis are discussed in Section IV. Section V contains all details regarding the simulation, network connectivity and its parameters and the results are presented. Finally, in Section VII the conclusions for this work are presented.

II. RELATED WORK

In the 1940s, McCulloch and Pitts envisioned that the brain would be composed of units with logic gating capabilities [28]. During that time this did not have much impact in neuroscience simply because neuronal cells are much more dynamic than simple digital logic gates, but their proposal did positively impact advancements in artificial neural network and machine learning theories [23]. The vision of creating logic operating engineered systems to interact between natural cells and engineered cells (i.e. bio-nanomachines) has the potential to create better alternatives for the treatment of diseases at the cellular level [29].

In light of numerous applications that can have an impact on biological systems [30], researchers have been investigating how logic gates can not only help treat neurodegenerative diseases but also enhance biological computations performed by the brain. One example is the work of Vogels and Abbott [24], where they investigated the signal propagation in networks of integrate-and-fire models of neurons and found that by either strengthening or weakening specific synapses, different types of logic gates may arise within the network. This "fine-tunning" approach to synaptic connections may pave the way to more sophisticated systems capable of, for example, weakening connections between neurons involved in a seizure or even strengthening connections responsible for memory storage.

Goldental and colleagues [23], on the other hand, decided to build on top of the fact that the way neurons work and communicate with each other exhibit far richer dynamics and so they proposed the concept of dynamic logic gates that work as a function of their historical activities, interconnection profiles, as well as the frequency of stimulation at the input terminals.

Song *et al* [31] took a different approach, where they considered a "third-party" for the analysis and proposed that the interaction of astrocytes in a tripartite synapse may be able to control the logic gate performance of neurons. Although they are also working with non-neuronal cells, the neurons used are all of the same morphological and electrical types.

III. NEURON COMMUNICATION BACKGROUND

Neuronal network communications allow the propagation of spikes through a population of neurons transferring information inside the brain. Bio-computing approaches based on the communication of neurons will rely on these propagation behaviour and its relation to the neuron properties as well as the characterization of neuronal communications. Therefore, before presenting the model of logic gates using neurons (Section IV), the morpho-electrical characteristics, the columnar and laminar organization properties of neurons as well as the compartmentalized Hodgkin-Huxley model for neuronal communications will be introduced.

A. Neuron Properties

Neuronal cells can be classified in terms of their morphology, electrophysiology, projections, position in the brain and the proteins and genes they express. The models of neurons used in this work, collected from [27], are classified only based on their morphological and electrical properties (morpho-electrical characteristics) as well as which cortical layer they are from (columnar and laminar organization). The classification method used in this work is detailed below.

1) Morpho-electrical Characteristics: Well-established features in the soma of the cell and its dendritic and axonal arbours are sufficient for the classification of different morphological cells. In terms of size, cortical neurons can be categorized as small neurons $(8 - 16 \, \mu m)$ along with neurons from the hippocampus, olfactory bulb and dorsal horn. Axonal features play a major role in distinguishing inhibitory types while excitatory types can be better identified by their dendritic features. On the other hand, the shape of the soma of cortical cells can help further categorize them into three major types [27], [32], [33]:

1) *Pyramidal cells* which are predominantly found in layers III and V and have a distinctive pyramidal shape. Its size (height $\times$ width) varies between $12 - 100 \, \mu m \times 10 - 60 \, \mu m$,
2) *Granule cells* can be found mostly in layers II and IV. The ones in IV receive inputs from the thalamus and pass information forward to cells in all other layers except to layer I. Its size range (height $\times$ width) is $15 - 30 \, \mu m \times 10 - 15 \, \mu m$.
3) *Fusiform cells* mainly populates in layer VI and have a flattened spindled-shaped form. They send information from the cortex back to the thalamus and some of its dendrites elongate up to layer I. The size of the soma for this type of cell varies between $15 - 30 \, \mu m \times 10 - 15 \, \mu m$ [32].

Different morphological types (m-types) of cells can have diverse firing patterns. These patterns are generated in response to the injection of step currents in cortical neurons. From the 11 different electrical types (e-types) identified by Markram et al [27], all m-types used in this work are burst Non-accommodating (bNAC) e-types.

2) Columnar and Laminar Organization of the Cortex: The cerebral cortex is composed of neurons arranged into six horizontally and dispersed layers. These layers have different characteristics such as thickness, size, cell type and cell density showing a "laminar" organization and subdividing the cortex into disparate regions and areas. These layers are known as (1) Molecular layer, (2) External granular layer, (3) Pyramidal layer, (4) Inner granular layer, (5) Ganglionic layer and (6) Multiform layer.

Despite the horizontal layering, cortical regions display vertical connections that are of prime importance and take two forms: mini-columns (also called, micro-columns) with approximately $30 - 50 \, \mu$m in diameter and when activated by peripheral stimuli, it generates the macro-columns, with a diameter of approximately $0.4 - 0.5$ mm [34].

B. Neuronal Communications

1) Neuron-to-neuron Communication: Communication between neurons is performed through electro-chemical synapses. Action potentials travel down the axon of the pre-synaptic cell and by the time it reaches the axon terminal, it stimulates the release of synaptic vesicles inside the synaptic cleft. These vesicles contain neurotransmitters that bind to neuro-receptors in the dendrites of the post-synaptic cell, on the other end of the synaptic cleft, either depolarizing the membrane. The depolarization starts in a potential state of approximately -65 mV and moves up to the point it reaches a threshold which is high enough to trigger the initiation of an action potential (excitatory) or polarizing the membrane even more, which in turn blocks the postsynaptic cell of firing any spikes (inhibitory) [21], [35]. In larger networks, the balance between inhibitory and excitatory connections helps in encoding information through the neuronal network [36].

After the membrane potential reaches its maximum peak of depolarization, it starts to repolarize itself towards its resting potential right after a spike is fired. The potential gets hyperpolarized for a very short period which is known as *refractoriness* and can be subdivided into *absolute* and *relative*. During the absolute refractory period (ARP), the cell is unable to fire again regardless of how strong the stimuli are and it takes about $1 - 2$ ms followed by the relative refractory period (RRP) during which a cell can fire again if the applied stimulus is stronger than it was when applied at its resting state [35].

To model such a complex system, we present a simplification of the model that is used in the NEURON simulator [37], [38] based on the compartmentalized Hodgkin-Huxley model. In this model, the cell is broken down into J equal length parts, and the spike propagation is modelled in one compartment travelling to all others (Fig. 2).

We can describe a single compartment model with the following proposed by Pospischil *et al* [39]

$$C_m \frac{\mathrm{d}V}{\mathrm{d}t} = -g_{leak}(V - E_{leak}) - I_{Na} - I_{K_d} - I_M - I_T - I_L, \tag{1}$$

where V is the membrane potential, C_m is the specific capacitance of the membrane, g_{leak} is the resting (leak) membrane conductance, E_{leak} is its reversal potential. I_{Na} and I_{K_d} are the sodium and potassium currents responsible for action potentials respectively, I_M is a slow voltage-dependent potassium current responsible for spike frequency adaptation, I_L is a high-threshold calcium current and I_T is a low-threshold calcium current. These voltage-dependent currents are variants of the same generic equation which is described as
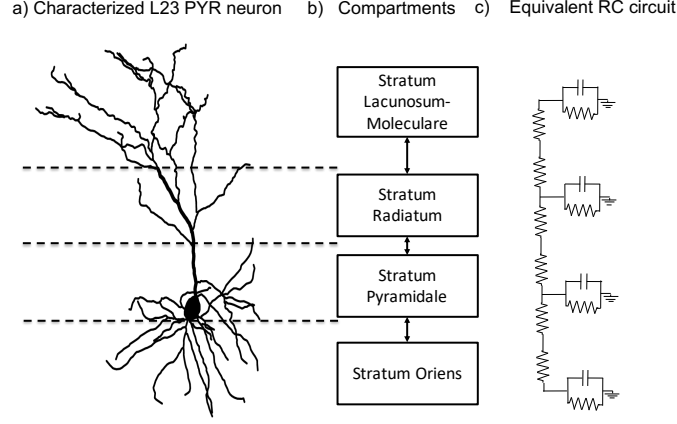
$$I_x = g_x m^M h^N (V - E_x), \tag{2}$$

Fig. 2. Cell comparmentalization; a) A morphological structure of a layer 2/3 pyramidal neuron, b) Compartment model of a Layer 2 pyramidal neuron including 4 compartments: stratum oriens, stratum pyramidale, stratum radiatum and stratum lacunosum-moleculare, c) The equivalent RC circuit module.

where the current I_x is expressed as the product of the maximal conductance, g_x, activation (m) and inactivation (h) variables, respectively, and the difference between membrane potential V and the reversal potential E_j. The gating of the channel is derived from the following first-order kinetic scheme

$$\text{C} \underset{\text{fi(V)}}{\overset{\text{ff(V)}}{\rightleftharpoons}} \text{O}, \tag{3}$$

where O and C are the open and closed states of the gate, and $\alpha(V)$ and $\beta(V)$ are the transfer rates for each respective direction. The variables m and h represent the fraction of independent gates in the open state, following the conventional approach introduced by [40] and stated as

$$\frac{\mathrm{d}m}{\mathrm{d}t} = \alpha_m(V)(1 - m) - \beta_m(V)m, \tag{4}$$

$$\frac{\mathrm{d}h}{\mathrm{d}t} = \alpha_h(V)(1 - h) - \beta_h(V)h. \tag{5}$$

To consider conductance-based inputs to the neuron in (1), it is necessary to the effects from the propagation and reception of neurotransmitters from another neuron in the synaptic cleft. We present a simple model for the sake of brevity, in which the neurotransmitter-activated ion channels (I_{syn}) is represented as an explicitly time-dependent conductance (g_{syn}), and it is defined as

$$I_{\text{syn}} = g_{\text{syn}} \left(V - E_{\text{syn}} \right), \tag{6}$$

where the parameter E_{syn} as well as g_{syn} are used to describe the many different synapses types. Typically, $E_{\text{syn}} = -75\text{mV}$ describes inhibitory synapses whereas $E_{\text{syn}} \approx 0$ describes excitatory ones. Based on this, g_{syn} can be defined as through a superposition of exponentials

$$g_{\text{syn}} = \sum_f \bar{g}_{\text{syn}} \, \mathrm{e}^{-(t-t^{(f)})/\tau} \, H(t - t^{(f)}), \tag{7}$$

where τ is a time constant, $t^{(f)}$ is the arrival time of a presynaptic action potential and $H(\cdot)$ is the Heaviside step function. The $t^{(f)}$ has a non-null value only when the membrane potential of the presynaptic compartment V_{pre} crosses a threshold th_{pre}, indicating a spike has occurred. This threshold-crossing mechanism for spike propagation is known as *event-based synapse* and it can be defined as

$$t^{(f)} = \begin{cases} t^{(f)}, & \text{if } V_{pre} \geq th_{pre} \\ \emptyset, & \text{otherwise.} \end{cases} \tag{8}$$

This can be thought of each synaptic event as a number of neurotransmitters released and bound to the postsynaptic terminal [41].

Integrating (1) for compartments that synapses may occur requires a simple addition of (6) on the left-hand side, as depicted below

$$C_m \frac{\mathrm{d}V}{\mathrm{d}t} = -g_{leak}(V - E_{leak}) - I_{Na} - I_{K_d} - I_M - I_T - I_L - I_{\text{syn}}(t). \tag{9}$$

In Subsection III-A, we presented the differences of morpho-electrical characteristics of neurons and their columnar and laminar organization that create a variety of neuronal networks with different types of cells. To incorporate these properties into the model presented in this section we need to use three different approaches. Their morphological properties will dictate the number of compartments of a cell type, which probably indicates that pyramidal, granule and fusiform cells will have different V propagation patterns based on their different number of compartments. For example, in Fig. 2, we divided a layer 2 pyramidal neuron into 4 compartments (stratum oriens, stratum pyramidale, stratum radiatum and stratum lacunosum-moleculare). By using the NEURON simulator, we can capture morphological properties with precision through the validated models of Markram et al [27] in which compartments are already provided. In a similar manner, also using the models from [27], it is necessary to change the following parameters in order to shape the electrical characteristics and obtain a type-specific spiking activity, other than the types already available: m, h, $\alpha(V)$, $\beta(V)$, g_x, g_{syn}, and initial values of E_{leak} and E_{syn}. Lastly, based on the cell type, we define a network of excitatory neurons that consider the connection probabilities between them as defined in the *Neocortical Microcircuit Collaboration Portal*[1]. We use a simple directed graph to capture this network connectivity pattern, as shown in Fig. 3.
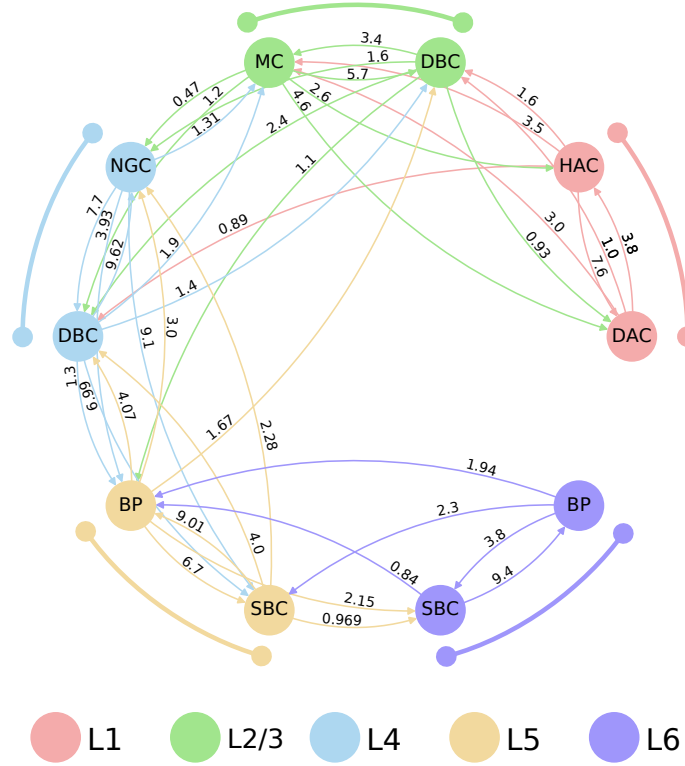

Fig. 3. Graphical visualization of network connectivity and each connection probability (in percentage) between pairs of neurons.

2) Role of the Threshold in Event-based Synapses: As aforementioned in Section III-B1, for a spike to be fired, the membrane potential of the cell compartment to reach a threshold during its depolarization state, the threshold for spike initiation varies with stimuli, cell type and the history of cell's activity. It is not yet clear what characteristics can cause this variability which may affect the performance of the gate. According to Platkiewicz and Brette [42], even though the concept of spike threshold may be different for *in vivo*, *in vitro* and computational experiments, the threshold in brain cells depends on several parameters such as stimulus, type of cells, synaptic conductances and properties of ionic channels.

From a synaptic point of view, with each action potential arrival at the presynaptic terminal at time $t^{(f)}$, a specific number of neurotransmitters may be released into the synaptic cleft and has a probability of binding to the neuroreceptors at the postsynaptic cell. This release process is proportional to the shape and energy of the incoming action potential. An event-based synapse mimics this chemical process and sends an event with a synaptic weight to the postsynaptic cell that may trigger an action potential and consequently propagate information through the network.

[1]https://bbp.epfl.ch/nmc-portal/welcome

To the best of our knowledge, there are no works that utilizes realistic models of neurons, and especially the neuron models proposed by Markram *et al* [27], where the gates are constructed from heterogeneous neuronal arrangements and controlled by their respective threshold for event-based synapses.

IV. NEURONAL DIGITAL LOGIC GATES AND CIRCUITS

In this section we describe the construction of neuronal logic gates and how queue theory can be applied to neuronal circuits to predict and assess how the stimuli in the pre-synaptic terminal is being processed by the post-synatpic cell.

A. Single Logic Gates

Eight neuronal logic gates were built, including five different OR gates and three different AND gates. The truth table for both of these types of gates is depicted in Table I. For an AND gate, both inputs must be non-null in order to have a non-null output. On the other hand, an OR gate can send out non-null output not only when both inputs are active but also when either one of them are active while the other is not.

TABLE I
TRUTH TABLE FOR BOTH GATE TYPES.

	Truth Table		
I_1	I_2	O_{AND}	O_{OR}
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

All cell types used to build the gates are listed in Table II. For each gate, three different types of cells were arranged in a way that two of them should operate as the inputs of the gate and the third one as the output (Fig. 4(b)). The idea is to keep the inner connections of the gate, i.e. the connection between the inputs cells with the output cell, fixed at their default parameters and respective connection probabilities according to the type of cells being connected.

TABLE II
TYPES OF CELLS USED TO BUILD THE GATES.

	Cell Types	
L1	DAC	Descending Axon Cell
	HAC	Horizontal Axon Cell
	SAC	Small Axon Cell
L2/3	MC	Martinotti Cell
	NBC	Nest Basket Cell
	BTC	Bitufted Cell
	DBC	Double Bouquet Cell
	LBC	Large Basket Cell
L4	DBC	Double Bouquet Cell
	SBC	Small Basket Cell
	MC	Martinotti Cell
L5	BP	Bipolar Cell
	SBC	Small Basket Cell
L6	MC	Martinotti Cell

Combinations of cells (as illustrated in Fig. 4(a)) were created largely based on their respective connection probabilities. Since the synaptic weight was kept at a fixed starting value, the higher the probability of two cells establishing a synapse, the higher the influence of the pre-synaptic cell on the post-synaptic cell. In this case, OR gates should have stronger inner connections when compared to AND gates so we can achieve the desired behaviour, as presented in Table I.

In this work, a simple *On-Off Keying (OOK)* modulation is implemented where a spike is considered as a bit '1' and its absence a bit '0' in each time slot (usually 5 ms long) for the inputs into the synthetic gates. The example spikes that propagate along each neuron of a gate is illustrated in Fig. 5. When reproducing a $[1, 1]$ input with both L1-HAC and L1-DAC cells (Fig. 5 left side), the spikes should arrive at L23-MC with minimum amount of time shift between the spikes to avoid misprocessing of the inputs by the output cell.

B. Queuing Theory in Neuronal Circuits

Queueing theory is applied in our analysis with the objective of evaluting the response time and accuracy of the proposed neuronal logic gates. When looking into the times of arrival of spikes, in other words, considering only the electrical behaviour of an electro-chemical synapse, even though there are two inputs, we assume that there is only one queue at the server in
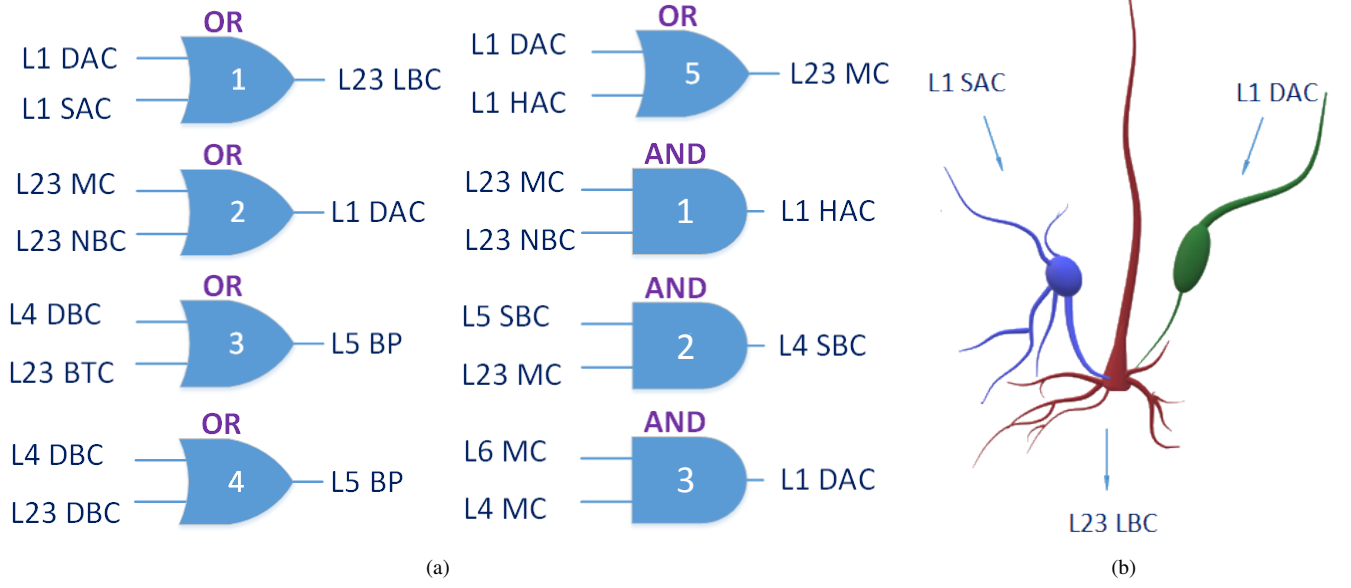
Fig. 4. Neuronal logic gates; (a) set of neuronal logic gates built using the models of neurons shown in Table II in a traditional representation and (b) potential real connection of neurons as a gate.
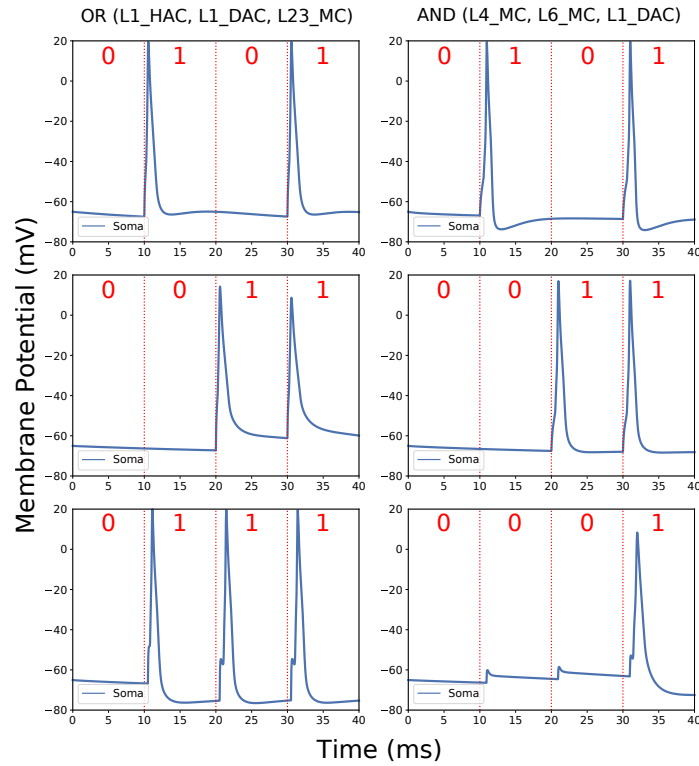

Fig. 5. Basic simulation with inputs $[0,0]$, $[0,1]$, $[1,0]$ and $[1,1]$ for both OR and AND gates with a 10-ms time slot. Inputs 1 and 2 are the first and second rows respectively, the last row is the output.

which the inputs arrive at a unified rate. At any given moment, only one impulse is carried by the cell and any impulse coming at a rate higher than the service rate may be lost, otherwise, the cell may be able to carry the stimulus and fire again if the input is strong enough to trigger an action potential. The server utilization over a certain period of time, however, depends on the rate of the impulse arrival to the presynaptic terminal.

1) Queueing Analysis: Consider three neuronal cells arranged as a gate, as illustrated in Fig. 4(b), in which two of them are inputs 1 and 2, respectively, and the third cell is the output. We assume that inputs 1 and 2 have *poissonic* rates of λ_1 and λ_2 spikes per second, respectively, and the output cell "processes" those inputs with a rate of μ spikes per second.

Let's also consider that each input has an individual inter-spike interval, ΔI_1 and ΔI_2, and an inter-neuronal spike interval between both inputs, ΔI_N. It is safe to assume that from the perspective of the output cell, the inputs have a merged rate, λ, defined as [43]

$$\lambda = \lambda_1 + \lambda_2, \tag{10}$$

which means that there is only one input with rate λ and, analogously, ΔI_N as a unified inter-spike interval. In other words, inputs arrive at time $t^{(f)} + k \cdot \Delta I_N$, as depicted in (8), where k is a zero-indexed order of arrival.

The system now looks like a single-queue and single-server (Fig. 6). However, if $\mu < \lambda$, there will be no waiting time and, any spike that is not processed at a first come first serve basis, will be lost.
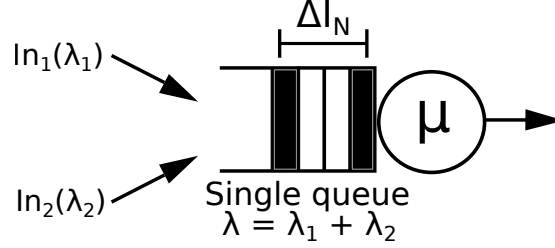

Fig. 6. Illustration of merged rates of pre-synpatic spikes into a single queue to be processed by a single server as described in Section IV-B1. ΔI_N may have different values for OR and AND gates.

In the case of an OR gate, the output cell should fire when either of the inputs or even both of them fire, hence

$$\Delta I_{1,2} \geq 2 \cdot \Delta I_N, \tag{11}$$

on the other hand, a cell working as an AND gate should fire only when both inputs fire together. So

$$\Delta I_{1,2} \leq Rp + \Delta I_N. \tag{12}$$

where Rp is the refractory period of the output cell. There are different rules for the value of ΔI_N when either input fires (OR gate) or both inputs fire (both gates), thus

$$\begin{cases} \Delta I_N \geq Rp, & \text{either input fires,} \\ 0 \leq \Delta I_N \leq t_s, & \text{both inputs fire,} \end{cases} \tag{13}$$

where t_s is some threshold in milliseconds allowing the cell to process neighbouring spikes as $[1,1]$ input.

If an input arrives with time $t^{(f)}$ (7), then the probability of another input arriving **before** $t^{(f)} + t_s$ is

$$P(1|[t^{(f)}, t^{(f)} + t_s]) = 1 - e^{-\lambda \Delta I_N}, \tag{14}$$

where for an AND gate, the smaller the t_s, the better to evoke a spike in the output. In the case of an OR gate, we are also interested in another input arriving **after** $t^{(f)} + t_s$, which will transform into

$$P(1|[t^{(f)}, t^{(f)} + t_s]) = e^{-\lambda \Delta I_N}. \tag{15}$$

Using both (14) and (15), it is possible to predict the output and then calculate the accuracy in relation to the expected output. This accuracy should be compared to the approach for calculating the difference between the actual output of the gate and the expected output. The model is further validated in Subsection VI-A, where we employ the Mean Squared Error (MSE) analysis.

V. SIMULATION MODEL

In this section, the simulation model for a single neuronal logic gate as well as the application case-study scenario for the suppression of epilepsy, are presented.

TABLE III
PARAMETERS FOR SIMULATION.

Simulation Parameters	
Synaptic weight	0.04 μS
Simulation time	1 s
Time slot	5 ms
NetStim.noise	1
ExpSyn.tau	2
NetCon.threshold (AND)	-64 mV
NetCon.threshold (OR)	5 mV
NetCon.delay	0
Threshold (spike detection)	0 mV
Rp	5 ms
t_s	0 ms

A. Single Gate

The single neuronal logic gates were simulated in two ways. First, they were individually analyzed and simulated in isolation, where their respective accuracy values were evaluated and those results were fitted to the model described in Section IV-B1. In isolated form, their configuration is illustrated in Fig. 4(b).

For all simulations, intrinsic parameters of the cell were kept at their default values (such as the length and diameter of each compartment of the cell), and all other parameters of the simulator required to reproduce the desired behaviour are shown in Table III.

The values of Rp and t_s are only used when simulating the queue model and they are not part of the simulation of the network.

1) Accuracy: All gates were tested in terms of accuracy with variations in a few parameters to test their performance. These parameters include their firing rate, λ and synaptic threshold, th. As mentioned earlier in Subsection IV-A, we are using an OOK modulation to discretize the spiking activity into binary code. Action potentials can shift and get slightly delayed during propagation, and this is due to axonal characteristics. This emphasizes the importance of having a time slot with a fair length of time so there is a fair distinction between different input combinations. The accuracy will measure how correct is the bit train from the output cell with regards to the ideal output that would be generated by an error-free logic gate. In the simulations, random spike trains following a *Poisson* process were stimulated. For each simulation, since the input is random, the number of spikes fired between both inputs with the same rate is approximately the same.

The accuracy is calculated according to the following equation [44]:

$$A(E[Y]; Y) = \frac{P_{1,1} + P_{0,0}}{P_{1,1} + P_{1,0} + P_{0,1} + P_{0,0}} \tag{16}$$

where $P_{Y,E[Y]}$ is the probability of Y given $E[Y]$ in which Y is the actual output and $E[Y]$ is the expected one and $Y \,\&\, E[Y] \in \{0,1\}$.

2) Mean Squared Error (MSE): To validate the model proposed in Section IV-B1, we estimated how far away our predictions were from the values of accuracy by using *Mean Squared Error*. MSE is a way to measure the quality of an estimator, and in our case, we want to determine the effectiveness of our model with respect to the real accuracy of the gate operation.

Consider that A is the actual accuracy obtained from the real output and that $\overline{A}$ is the predicted accuracy estimated by our model, then the MSE for each point can be calculated as

$$MSE = \frac{1}{a} \sum_{i=1}^{a} (A_i - \overline{A}_i)^2, \tag{17}$$

where a is the number of accuracy values.

B. Neuronal Activity Behavior During Epileptic Seizures

Neuronal synchronization is the basis for fundamental brain processes. In neurological diseases, such as epilepsy, neuronal synchronicity as well as the balance between excitation and inhibition in populations of cortical neurons can be modified [45], [46].

In this work, a study on brain seizures is conducted by simulating the activity of neurons grouped in a cortical column and by reproducing the stages of spikes before, during, after, and recovery periods of epileptic seizures with a dynamic firing rate. The frequencies for stimulation varies according to results published by Alvarado-Rojas *et al* [45]. In a simulation with time $T = 1000$ ms, the firing rate γ (spikes/s) of the network under epilepsy for the periods of before, during, after, and resting period is based on the following values
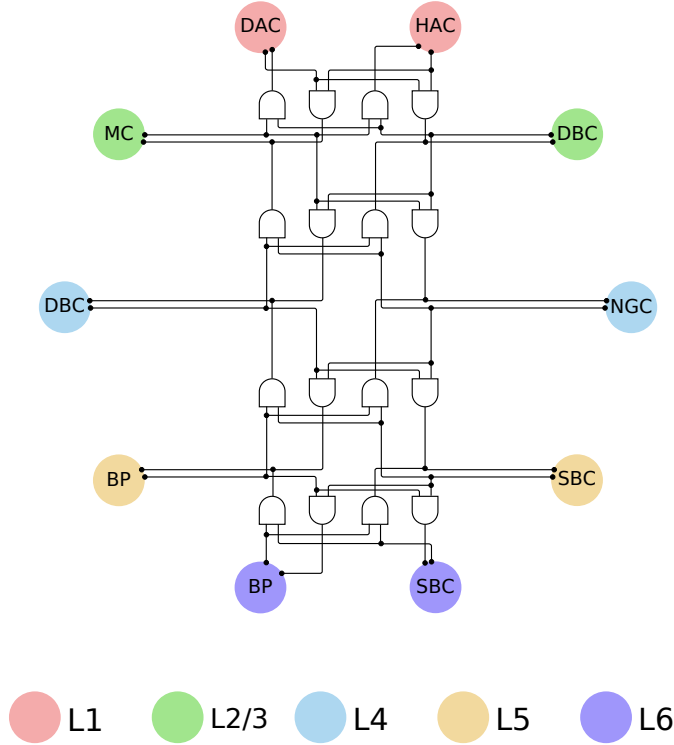
Fig. 7. Schematic of the connection of 16 neuronal logic gates in between the 10 cells that forms the network. The placement of a logic gate in the network require the breakage of the natural connections between the cells.

$$\gamma = \begin{cases} 30, & \text{if } T \leq 300, \\ 70, & \text{if } 300 < T \leq 650, \\ 180, & \text{if } 650 < T \leq 750, \\ 10, & \text{if } T > 750, \end{cases} \quad (18)$$

where the evoked activity of the network also follows a *Poisson* process. This procedure can also be described with the pseudo-code presented in Algorithm 1.

**Algorithm 1** Development of Epileptic Seizure Model

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1: **Inputs:**
   $\gamma = \{30, 70, 180, 10\}$
   $T = \{0, 300, 650, 750, 1000\}$
2: **Initialize:**
   $\mathcal{C} = \{c_1, ..., c_n\}$
3: **for** $c_n \in \mathcal{C}$ **do**
4:   **for** i : $0 \rightarrow$ length(γ) **do**
5:     stimulate c_n at $(\gamma_i, [T_i, T_{i+1}])$
6:   **end for**
7: **end for**

Neuronal AND logic gates were inserted inside a network with 10 neurons (two neurons per cortical layer) that simulated different stages of an epileptic seizure. The positioning of the gates inside the network is depicted in Fig. 7.

VI. RESULTS AND DISCUSSIONS

In this section, we present a discussion over the results for the logic gate analysis and its epilepsy case study.
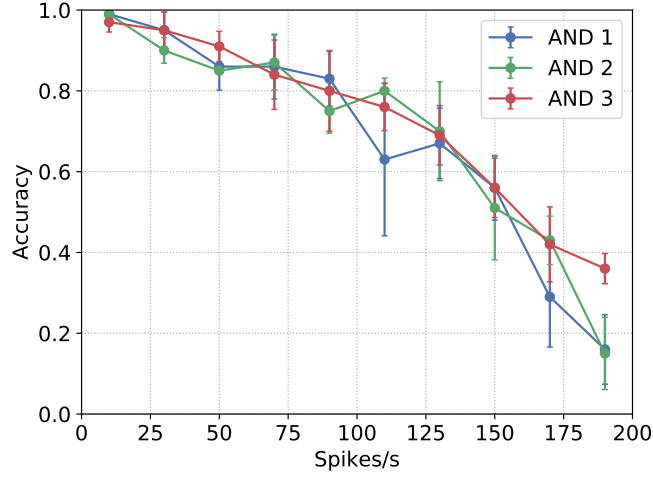
(a)
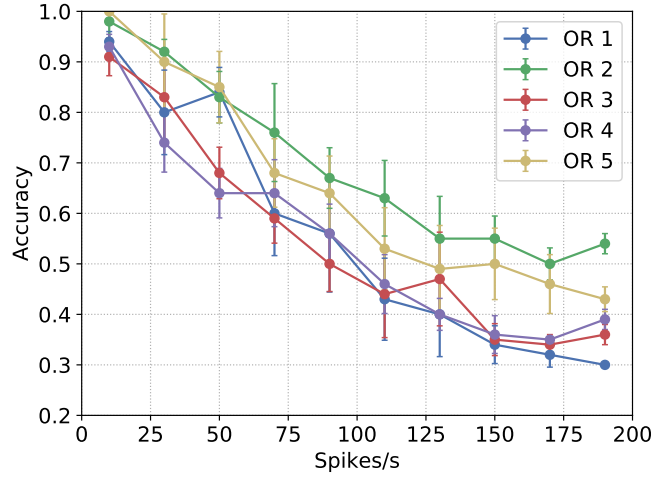
(b)

Fig. 8. Mean and standard deviation of the accuracy for the (a) three AND gates and (b) five OR gates. Five simulations were performed for each rate and the firing of the spikes follows a *Poisson* process.

A. *Logic Gate Performance*

For the single gate performance accuracy, we use the configurations that are presented in Fig. 4(a). In the simulations with isolated gates, two different analysis were performed. First, the spiking rate was increased and the accuracy of the gates was computed, and the simulations used the parameters shown in Table III. In both Figs. 8(a) and 8(b), the accuracy decrease as the firing rate increases, but they are decreasing at different rates due to their different behaviours as shown in Table I and Fig. 5. Even though the different versions of both types of gates have very similar values of accuracy, in Fig. 8(a) all of the AND gate configurations have very similar behaviour, this may be due to the fact that, as depicted in Table I, there is only one way for the gate to fire which decreases the chances of misprocessing the inputs. Meanwhile, since OR gates have more ways of firing an output (Table I), the different arrangements may be affecting the processing of the inputs by the output considering that the gates have a bit less similar perfomance between each other when compared to the performance of AND gates. Fig. 8(b) shows that OR 2 slightly stands out in performance with better accuracy compared to the other OR gates. To obtain the mean and standard deviation, the simulation ran five times.

Second, two gates were picked out, one of each type (OR2 because it showed a better accuracy in Fig. 8(b) and, AND1 was actually picked at random since all AND gates have a similar performance), and the accuracy was computed based on both the accuracy and the threshold at the pre-synaptic compartment. In Fig. 9, it is noticeable that the accuracy has a relationship with the threshold, th_{pre} in (8), and spiking rate of the neurons, $\lambda_{1,2}$ in (10). Generally speaking, lower spiking rates with higher thresholds negatively affects the accuracy of both types of gates. The results presented is based on the mean from three simulation runs.
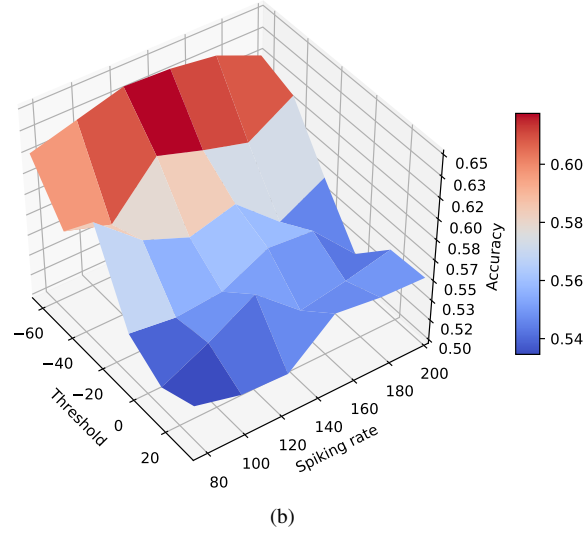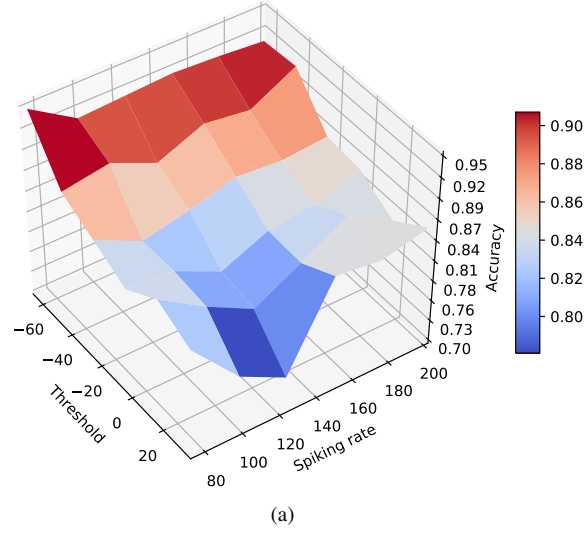
(a)

(b)

Fig. 9. Spiking rate λ, threshold th and mean accuracy Acc for gates (a) AND1 and (b) OR2.

TABLE IV
ACCURACY MEAN AND STANDARD DEVIATION VALUES FOR DIFFERENT DELAYS BETWEEN INPUTS.

Effect of Delay on Accuracy								
Types	AND 1	AND 2	AND 3	OR 1	OR 2	OR 3	OR 4	OR 5
Mean	0.9660	0.9530	0.9954	0.7595	0.8595	0.7630	0.7615	0.7720
Std Dev	0.00577	0.00604	0.00603	0.02871	0.02752	0.03059	0.03405	0.03039

The effect of shifting the synchronization of the spikes by up to 4 ms was also analyzed. The results, depicted in Table IV, did not show any specific trend when the shift was increased. For the AND gates, the accuracy remained above 95%, which represent a difference of at least 9% in relation to OR gates where the highest performance is approximately 86%. The highest standard deviation for an AND gate is still over 50 times smaller than the highest value for an OR gate, as aforementioned, this may be due to their different gating behaviours.

The prediction model was analyzed in relation to ΔI_N and its performance is presented for two gates *AND1* (Fig. 10(a)) and *OR2* (Fig. 10(b)). These accuracy values were calculated with a five-millisecond time slot for the discretization analysis of the output cells. The other performances were omitted to avoid redundancy but MSE values are presented in Fig. 11 for all of the eight built gates. The results presented in Fig. 10 shows that for the AND gates, the model results in slighlty higher accuracy compared to the OR gate. This difference between types of gates reveals itself for the other six gates, four of the OR type and two of the AND type.

In Fig. 11, the sampling frequency was changed to evaluate how the shift among bits from both inputs affect the results of
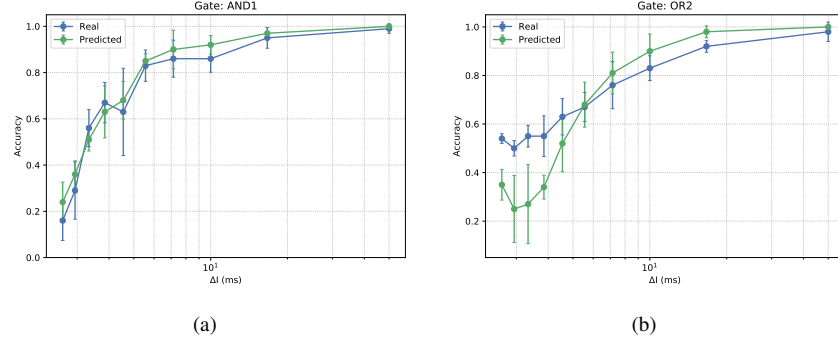
Fig. 10. Real and predicted mean and standard deviation of the accuracy for an (a) AND gate type 1 and (b) OR gate type 2 in relation to the ISI. Predicted results obtained from the implementation of the model proposed in Section IV-B1.
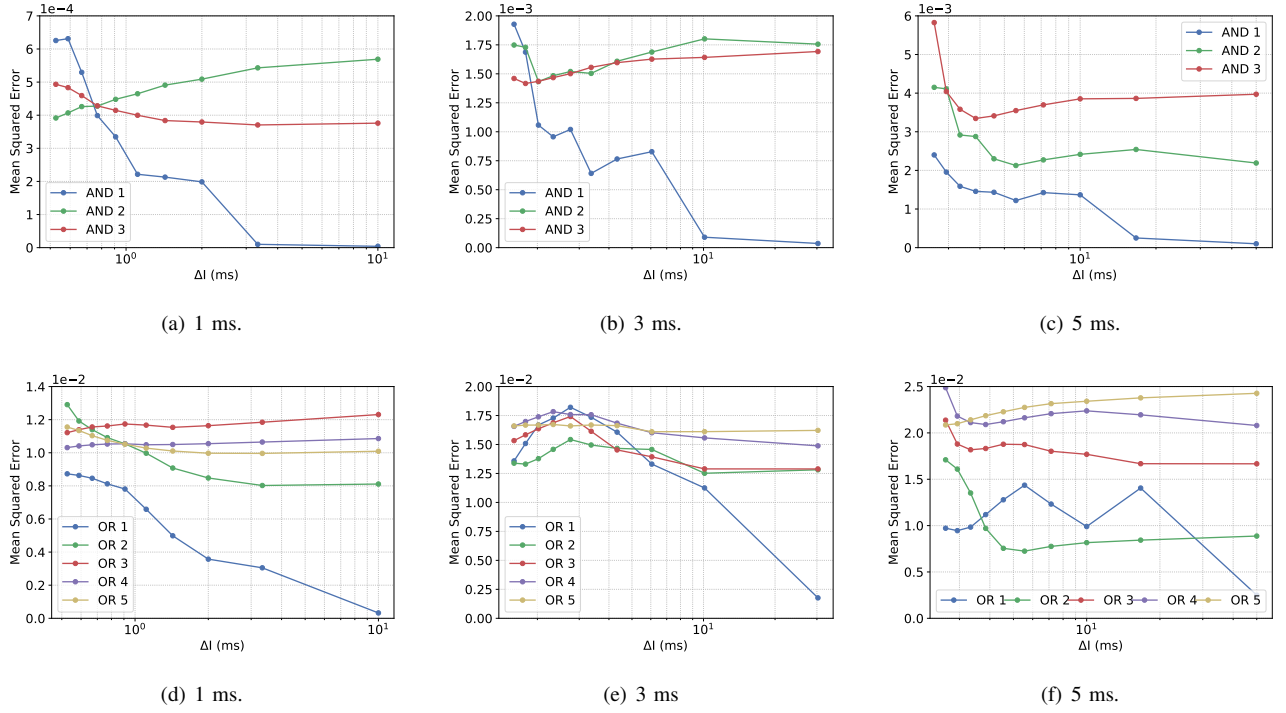

Fig. 11. Mean Squared Error between the predicted accuracy by the model described in Section IV-B1 and accuracy calculated with real output. Spike trains were sampled at different time slots. Figures 11(a), 11(b) and 11(c) show the MSE for all AND gates and Figures 11(d), 11(e) and 11(f) show the MSE for all OR gates.

our model in comparison with the real firing of the gates.

Figs. 11(a)-11(c) shows the MSE for AND gates with ΔI_N equal to 1, 3, and 5 ms respectively. On the other hand, Figs. 11(d)-11(f) show results for the same analysis but OR gates. In both scenarios, the best MSE was for a time slot with a length of 1 ms, even though an action potential takes a longer period than the firing as well as duration to pass the absolute refractory period. For all gate models, the MSE is quite low showing the robustness of developing gates from the various types of neurons.

B. Epilepsy Case Study

When simulating a network of cells susceptible to epileptic seizures, the analysis was performed in both cases (with and without logic gates within the network). Only one type of AND gate was used in random positions within the network (as illustrated in Fig. 7) that is composed of L23-MC, L23-NBC and L1-HAC cells. The placement of the AND gates was chosen at random and we start placing the gates inside the network at regions with high connections to other cells.

Figure 12(c) shows how placing higher number of gates inside the network may help filter out high frequencies of firing by decreasing the average firing rate of the network. This effect is visually shown in Figures 12(a) and 12(b), where during

(a) Zero gates in the network.

(b) 16 gates in the network.
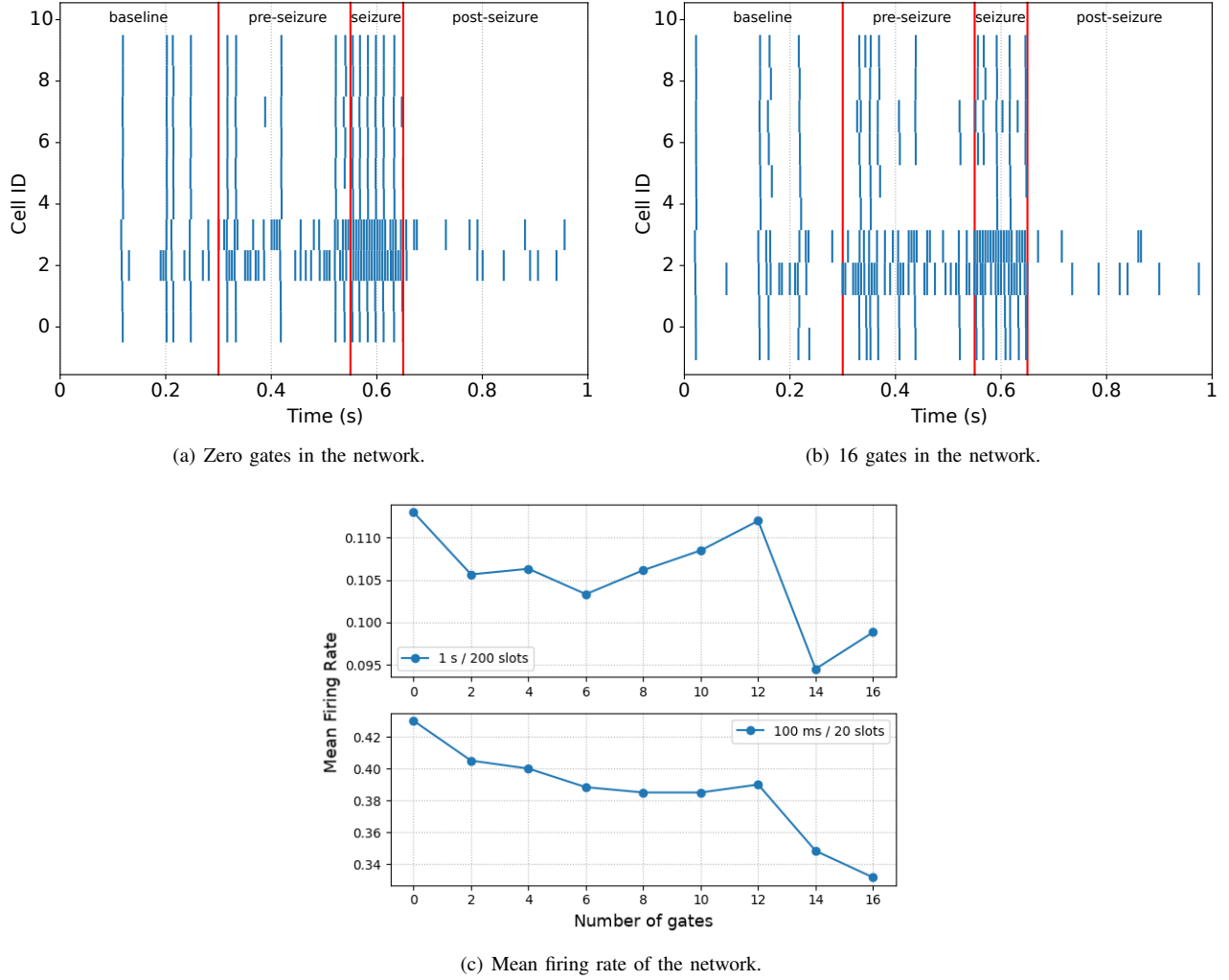
(c) Mean firing rate of the network.

Fig. 12. Simulation of epileptic seizures in a network with 10 neurons (2 neurons per cortical layer), stimulation performed in cells at layer 2/3. (a) Raster plot of the network with no gates inserted and natural connections only as illustrated in Fig. 3; (b) Raster plot of the network with 16 neuronal logic gates, natural connections are broken where gates are placed. Placement depicted in Fig. 7; (c) Mean firing rate in the network as the more and more gates are placed within it; top graph shows the firing rate of the whole network for all stages as shown in Figures 12(a) and 12(b); bottom graph shows the firing rate for the whole network but only for the seizure stage.

the seizure, the entire network resulted in lower levels of activity with 16 gates in comparison with the network that did not contain any gates.

VII. CONCLUSION

Even though around 50 million people worldwide have epilepsy, it is estimated that 10% of the world population will have a seizure during their lifetime without even being an epileptic person. In this paper, the performance of neuronal logic gates was presented as isolated units and their positive effect by smoothing out the synchronous activity of several brain cells that occur during seizures. This approach requires that the cells involved in the gating process should be synthetically engineered and strategically positioned depending on the network connectivity with the objective of improving results.

Also in this work, it was proposed a model based on queue theory concepts that can predict how accurate a specific gating unit can be based on the input and threshold of the output cell. The model showed, in the worst scenario, for OR gates, an MSE of 0.025 while for AND gates this value is of 0.006. The results also show that the sampling frequency of the spike train plays a role in the accuracy of the gates and the quality of the model. Although this paper only concentrated in the treatment of seizures in the brain, logic gates can also be applied for the encoding of information and have the potential to use synthetic biology to create medical nano-machines to improve the quality of life of people with neurodegenerative diseases and the enhancement of information processing inside the brain.

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