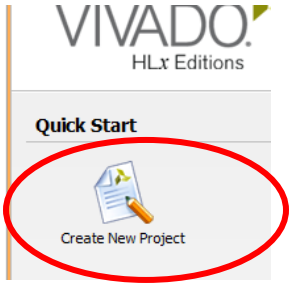
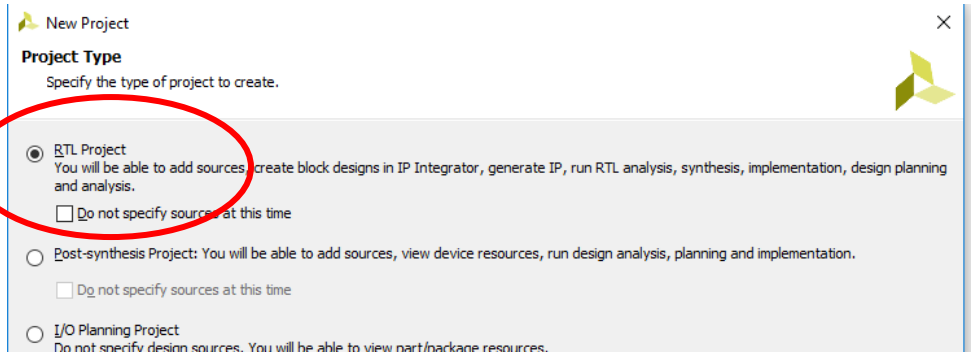
FPGA Synthesis Tutorial
Xilinx Vivado 2016.2

Make sure you have the following files on a memory stick or on a folder in the system:
- next4fpga.v (this is the top level module)
- clk_divider.v
- decade.v
- seven_seg.v
- n4DDRfpga.xdc (this is the Xilinx design constraint (.xdc) file)

1) turn on power to FPGA board (slide switch near security cable; red light indicates power applied)
2) Go to the directory **Xilinx Design Tools**/ or START Menu on Windows
3) click on directory **vivado 2016.2**
4) click on vivado 2016.2 (it's the one with the green three-piece logo)
5) click "create new project"



6) click "next"
7) fill in the name of directory (which will be created) on your memory stick or your windows account. Click "select"
8) check the "create project subdirectory" box
9) click "next"
10) select "RTL project"

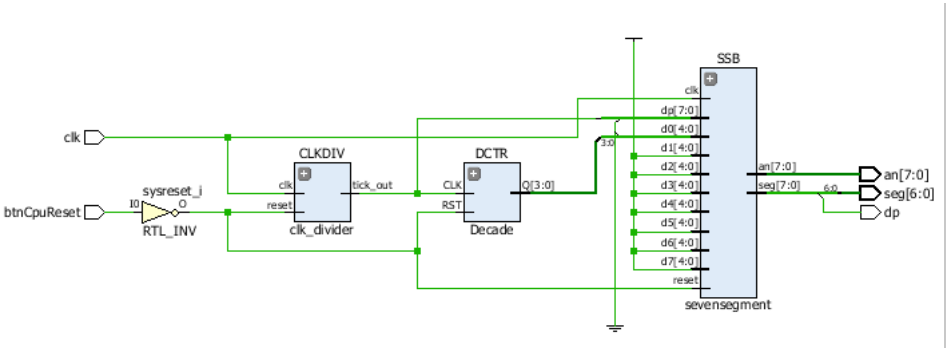


11) click "next"
12) click "+" and then "Add Files". Enter the name of all of the files needed for the design (the 4 .v files listed above) NOTE: If you hold down the shift key you can select them all at once.

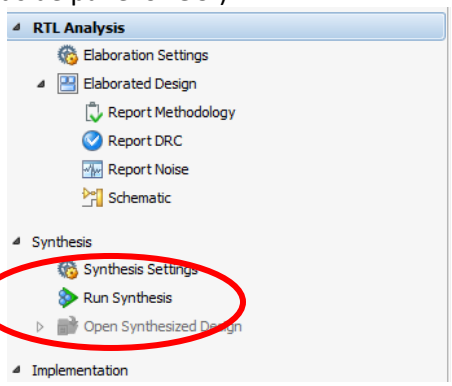
Then click “ok”. (This does not include the constraints file .xdc)

13) after all *.v files have been entered, click “next”
14) there are no Existing IP to add so click “next”
15) you do have a constraint file (the *.xdc file above). Add it by clicking “+” and then “Add Files”. Choose “n4DDRfpga.xdc”. Then click “ok” and “next”.
16) choose a device from the dropdown menu. (The device on the board is a **xc7A100tcsg324-1**)
17) click “next” (a project summary is displayed. verify it is correct)
18) click “finish”
19) (optional) If you choose on the left side “RTL analysis”, “Open Elaborated Design” and “schematic” then a schematic of your design will be displayed. This step **not** required for synthesis.

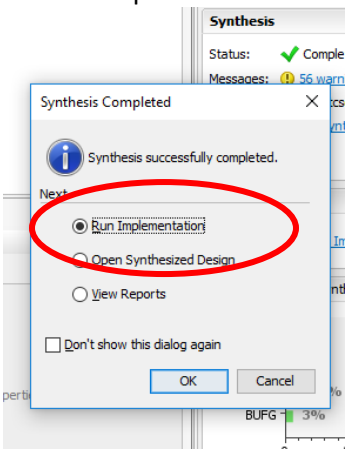
The design should look something like:



20) click on “run synthesis” (on left side panel of GUI)

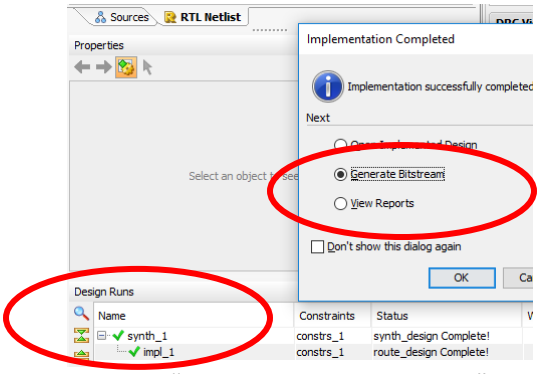


21) When the popup box appears, choose “run implementation” then click “ok”

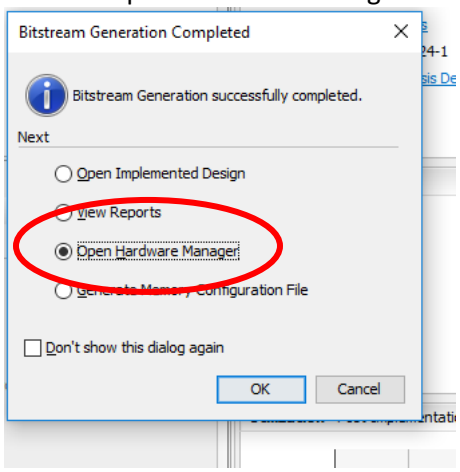


22) When the popup box appears, choose “generate bitstream” then click “ok”

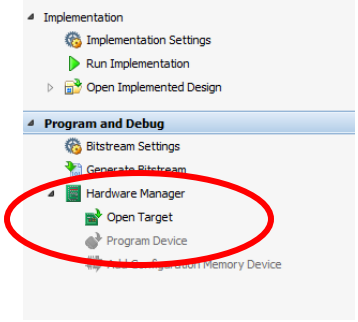
Note: If your implementation and synthesis ran without errors, you will find green tick marks in the design runs tab in the below section of the screen:



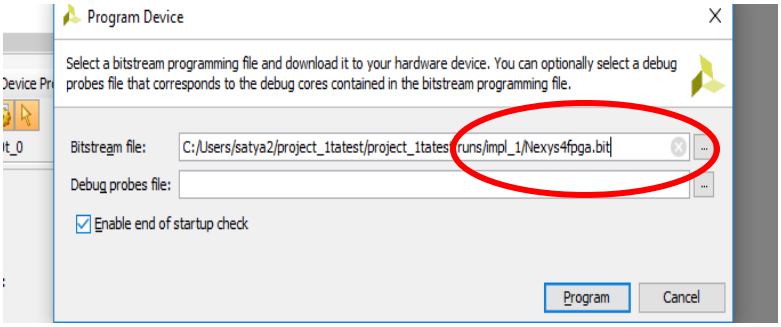
23) When the popup box appears, choose “open hardware manager”



24) On the left side of the GUI click on “open target” and choose “auto connect”



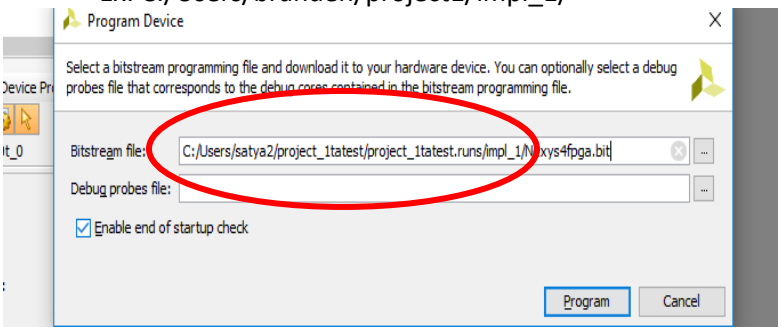
25) click “program device” which is enabled now on the left panel (click on device displayed)
26) click “program” This will pop up a window with your .bit file. Click on “Program”



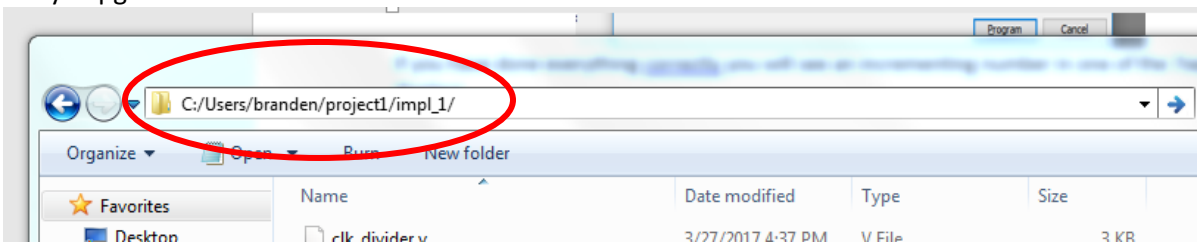
If you have done everything correctly you will see an incrementing number in one of the 7segment displays.

Saving the BITSTREAM file for DEMO

1) While doing the Step 26, the below screenshot shows the pop up window with the Nexys4fpga.bit file. Copy the file path of this ".bit" file
   Ex: C:/Users/branden/project1/impl_1/



2) Open windows explorer, paste the path in the field shown and press enter. Now, locate the Nexys4fpga.bit file in the folder.



3) Save this .bit file to your pen drive and bring it for Demo. You do not need to re-simulate the design for the demo.

Note: Save this bit stream file for future assignments as well.

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