ECE 351 HW 3

1) (5 points) Write a Verilog program that implements the Moore FSM shown below.
2) (5 points) Write a testbench that tests your FSM module for the input sequence $r = 0\ 0\ 1\ 0\ 1\ 1\ 1\ 1\ 0$
3) (2 point bonus) This is an optional problem. Simulate your FSM using the testbench from question 2. Turn in a hard copy of the timing diagram.