ECE 351 Syllabus for Spring 2019 Qtr

Instructor: Dr. Garrison Greenwood
email: greenwd@pdx.edu
Office: FAB 20-12
Office hours: W 1500–1700

Prerequisites: ECE 172 (or equivalent)

Course Objectives:

Students must demonstrate the ability to

- describe complex digital designs in the Verilog HDL.
- design testbenches needed to test digital designs
- describe those language syntax that promotes efficient synthesized designs
- apply design automation tools to synthesize designs in FPGAs
- describe good coding practices for efficient FPGA synthesis
- describe how embedded systems are implemented in FPGAs
- be familiar with timing closure and how it is accomplished

Textbook: https://www.oreilly.com/library/view/verilog-hdl-a/0130449113/

1. The course will be supplemented with material, which will be posted on D2L. Supplemental material is testable.
2. Your grade will be based on the two one-hour tests (25 points each), homework (20 points) and a final exam (30 points).
3. The grade scale is

A	$\rightarrow$	≥ 90 pts
B	$\rightarrow$	80–89 pts
C	$\rightarrow$	70–79 pts
D	$\rightarrow$	60–69 pts
F	$\rightarrow$	< 60 pts

4. This class uses a Verilog simulator (Questa-sim) and a synthesizer design suite (Vivado) , which are installed on the PC network in the circuits lab in FAB. D2L contains a complete tutorial on their use.
5. This class uses a FPGA board which has a Xilinx FPGA chip on it. The boards are in the circuits lab in FAB. A tutorial on their use will be posted on D2L

6. General Notes:

- No curve is used in determining grades.
- Any form of cheating will not be tolerated. *If you cheat on an exam, you get a score of zero on that exam.* Character does matter.
- As a courtesy to me and your fellow students, turn off all cell phones before you enter the classroom.
- Homework is assigned each week and is due the following Thursday. All assignments will be posted on D2L.
- Homework is due at the end of the class period. Late homework is not accepted. You can turn in your homework early at the ECE office *but you must get it timestamped*. No timestamp and I consider it late.
- Do not email me your homework; it must be submitted in hardcopy form. Homework submitted directly to the TA will not be graded.
- Some homework assignments will require you to simulate and/or synthesize the design in an FPGA and demonstrate it to the class TA. These demos must be individual efforts (no team demos allowed.) For those assignments requiring demos you must successfully complete the demo or you will not get any points for that homework assignment.
- Late homework is not accepted.
- There are no extra-credit assignments of any kind.
- I introduce Verilog syntax in a specific order. Do not work ahead. If you use a syntax in the homework or lab report or quiz that I have not introduced in class, I will deduct points—*even if the syntax you used was correct.*
- Accommodations are collaborative efforts between students, faculty, and the Disability Resource Center. Students with accommodations approved through the DRC are responsible for contacting the faculty member in charge of the course prior to or during the first week of the term to discuss accommodations. Students who believe they are eligible for accommodations but who have not yet obtained approval through the DRC should contact the DRC immediately. If you are already registered with DRC, I need to see you ASAP to discuss your accommodations.
- Exams/tests taken by students registered with DRC should be taken at the same time as the regular class.
- The two one-hour tests are scheduled for 25 April and 23 May (both on Thursdays). The final exam is on Monday, 10 June from 1015–1205.
- Be sure to check D2L frequently as new material is added from time to time. I will also use D2L for course announcements.