Running Synthesis with Tcl

The Tcl command to run synthesis is `synth_design`. Typically, this command is run with multiple options, for example:

```
synth_design -part xc7k30tfbg484-2 -top my_top
```

In this example, `synth_design` is run with the `-part` option and the `-top` option.

In the Tcl Console, you can set synthesis options and run synthesis using Tcl command options. To retrieve a list of options, type `synth_design -help` in the Tcl Console. The following snippet is an example of the `-help` output: `synth_design -help`.

```
Description:
Synthesize a design using Vivado Synthesis and open that design
Syntax:
synth_design  [-name <arg>] [-part <arg>] [-constrset <arg>] [-top <arg>]
              [-include_dirs <args>] [-generic <args>] [-verilog_define
<args>]
              [-seu_max_util <arg>] [-flatten_hierarchy <arg>]
              [-gated_clock_conversion <arg>] [-directive <arg>] [-rtl]
              [-bufg <arg>] [-no_lc] [-fanout_limit <arg>]
             [-shreg_min_size <arg>] [-mode <arg>] [-fsm_extraction <arg>]
              [-keep_equivalent_registers] [-resource_sharing <arg>]
              [-control_set_opt_threshold <arg>] [-max_bram <arg>]
              [-max_dsp <arg>] [-cascade_dsp] [-quiet] [-verbose]
Returns:
design object
Usage:
  Name                           Description
  -----------------------------------------
  [-name]                        Design name
  [-part]                        Target part
  [-constrset]                   Constraint fileset to use
  [-top]                         Specify the top module name
  [-include_dirs]                Specify verilog search directories
  [-generic]                     Specify generic parameters.
                                 Syntax: -generic
                                 <name>=<value> -generic <name>=<value> ...
  [-verilog_define]              Specify verilog defines. Syntax:
                                -verilog_define <macro_name>[=<macro_text>]
                                -verilog_define <macro_name>[=<macro_text>]
  [-flatten_hierarchy]           Flatten hierarchy during LUT mapping.
                                 Values:
                                 full, none, rebuilt
                                 Default: rebuilt
  [-gated_clock_conversion]      Convert clock gating logic to flop enable.
                                 Values: off, on, auto
                                 Default: off
  [-directive]                   Synthesis directive. Values:
                                 default,
```

```
                                AreaOptimized_high,
                                AreaMutlThresholdDSP
                                AlternateRoutability
                                FewerCarryChains
                                RunTimeOptimized
                                Default: default
[-rtl]                          Elaborate and open an rtl design
[-bufg]                         Max number of global clock buffers used by
                                synthesis
                                Default: 12
[-no_lc]                        Disable LUT combining.
                                Do not allow combining
                                LUT pairs into single dual output LUTs.
[-fanout_limit]                 Fanout limit. This switch does not impact
                                control signals (such as set,reset, clock
                                enable) use MAX_FANOUT to replicate these
                                signals if needed.
                                Default: 10000
[-shreg_min_size]               Minimum length for chain of registers to be
                                mapped onto SRL
                                Default: 3
[-mode]                         The design mode. Values: default,
                                out_of_context
                                Default: default
[-fsm_extraction]               FSM Extraction Encoding. Values: off,
                                one_hot, sequential, johnson, gray, auto
                                Default: auto
[-keep_equivalent_registers]    Prevents registers sourced by the same logic
                                from being merged.
                                (Note that the merging can
                                otherwise be prevented using the synthesis
                                KEEP attribute)
[-resource_sharing]             Sharing arithmetic operators. Value: auto,
                                on, off
                                Default: auto
[-control_set_opt_threshold]    Threshold for synchronous control set
                                optimization to lower number
                                of control sets.
                                Valid values are 'auto', integer 0 to 16.
                                The higher the number, the more control set
                                optimization will be performed and fewer
                                control sets will result.
                                To disable control
                                set optimization completely, set to 0.
                                Default: auto
[-max_bram]                     Maximum number of block RAM allowed in
                                design. (Note -1 means that the tool will
                                choose the max number allowed for the
                                part in question
                                Default: -1
[-max_dsp]                      Maximum number of block DSP allowed in
                                design. (Note -1 means that the tool will
                                choose the max number allowed for the part
                                Default: -1
```

```
[-cascade_dsp]                  Controls how adders in sum DSP block outputs
                                are implemented.
                                The values are: auto, tree, and force.
[-quiet]                        Ignore command errors
[-verbose]                      Suspend message limits during execution
```

For the `-generic` option, special handling needs to happen with VHDL boolean and `std_logic` vector type because those type do not exist in other formats. Instead of `TRUE`, `FAlse`, or 0010, for example, Verilog standards should be given.

For boolean, the value for `FALSE` is as follows:

```
-generic my_gen=1'b0
```

For `std_logic` vector the value for 0010 is:

```
-generic my_gen=4'b0010
```

IMPORTANT: *Overriding string generics or parameters is not supported.*

IMPORTANT: *If you are using the* `-mode out_of_context` *option on the top-level, do not use the* `PACKAGE_PIN` *property unless there is an I/O buffer instantiated in the RTL. The out_of_context option tells the tool to not infer any I/O buffers including tristate buffers. Without the buffer, you will get errors in placer.*

A verbose version of the help is available in the *Vivado Design Suite: Tcl Command Reference Guide* (UG835) [Ref 3]. To determine any Tcl equivalent to a Vivado IDE action, run the command in the Vivado IDE and review the content in the TCL Console or the log file.

Multithreading in RTL Synthesis

On multiprocessor systems, RTL synthesis leverages multiple CPU cores by default (up to 4) to speed up compile times.

The maximum number of simultaneous threads varies, depending on the number of processors available on the system, the OS, and the stage of the flow (see this link in the Implementation User Guide - UG904). The Tcl parameter `general.maxThreads`, which is common to all threads in Vivado, gives control to the user to specify the number of threads to use when running RTL synthesis. For example:

```
Vivado% set_param general.maxThreads <new limit>
```

Where the `<new limit>` must be an integer from 1 to 8 inclusive. For RTL synthesis, 4 is the maximum number of threads that can be set effectively.