ECE 351 Test #1 Study Guide

Your test is scheduled for Thursday, 25 Apr. It is a one-hour open book/ open note, multiple choice test.

The test will cover the following topics:

- Verilog HDL syntax/semantics. In particular you should be able to answer questions about Verilog programs that appear on the exam
- Simulator/synthesizer concepts (i.e., concepts covered in the ASIC application note)
- Basic structures of Verilog modules
- Verilog levels of abstraction (nothing on behavioral)
- module templates and instantiation

NOTES:

- You must bring a SCANTRON 882E to class to record your answers. These can be purchased at the PSU bookstore.
- You may have any electronic device capable of reading PDFs
- There will be a short lecture prior to the test.