**Questa Sim Tutorial**

**This tutorial shows you how to simulate a Verilog HDL design. The simulated module is “adder.v” and the testbench is “test\_adder.v”.**

**Both of the above files should be stored on your own flash drive.**

1. From your desktop, open Questa Sim (you will find it under “All Programs Questa Sim-64 10.3b

Quest Sim”).

**2. Create a “New Project”**

a. On the menu‐bar, **select File** **New** **Project**.

b. **Type** project name.

c. **Choose location** (directory) where you want to save it by clicking “Browse” button.

(**Important:** Verilog files should be stored on your flash drive.)

d. **Click “OK”**.

3. Add existing files:

a. From the **“Add items to the Project”** window, **select** the **“Add Existing File”** option(icon)

and add source files by clicking **“Browse”** button.

b. **Select** source files and **click “Open”** and **“OK”**. (You will repeat this twice: once to add test\_addr.v and again to add adder.v)

c. **Close** “Add items to the Project” window.

4. Compilation step:

a. On the menu‐bar, **select Compile** **Compile All**

Or click the “Compile All” icon ( ) on the Main window toolbar.

b. If a red appears next to your source file, your Verilog/SystemVerilog file has an error

that needs to be fixed.

If a green check appears, the compilation step passed.

5. Simulation step:

a. On the menu‐bar, **select Simulate** **Start Simulation**

Or click the “Simulate” icon ( ) on the Main window toolbar.

b. From the **“Start Simulation”** window, **click “(+)”** icon next to the “work” library.

c. Load the test module into the simulator by **selecting test\_addr**.

d. **Disable** optimization option by **removing check mark next to “Enable optimization”**.

e. **Click “OK”**.

6. Run step:

a. In the **“Objects”** window, **select all of the items (signals) listed** using the standard

**“Shift‐click”**. Once they are all selected, **“right‐click”** and **select Add** **To Wave** 

**Selected Signals**.

This should open up the **“Wave”** tab with all of the signals you selected from “Object”

window.

b. On the menu‐bar, **select Simulate** **Run** **Run –All** (or **Run 100**).

Or click either the “Run 100” icon ( ) or “Run –All” icon ( ) on the Main window

toolbar.

Also you can enter command **“run –all”** or **“run 100”** in the **“Transcript”** window.

c. When **“Finish Vsim”** window pops up, **click “No”**. (If you click “Yes”, it will close the

ModelSim GUI.)

7. To view the waveform move the cursor into the black timing diagram. Press “I” to zoom in; press “O” to zoom out.

8. To print out the waveform:

a. **Click “Wave” tab** and adjust waveforms by clicking **“Zoom”** buttons ( ).

b. Go to the menu‐bar, **select File** **Print**.

c. Choose printer name and click “OK”.

8. Exit from ModelSim GUI:

a. On the menu‐bar, **select File** **Quit** and **click “Yes”**.