BASE REGISTER	Region Name	Start Address	End Address	Description
	Control Module	0x44E10000	0x44E11FFF	Control Module Registers

	Offset	Control Module Register	Value	Description
Pin Config	0x95C	conf_spi0_cs0	0x2 (010b)	Write to enable (SCL) for MODE2 w/o pullup
	0x958	conf_spi0_d1	0x2 (010b)	Write to enable (**SDA**) for MODE2 w/o pullup

BASE REGISTER	Region Name	Start Address	End Address	Description
	CM_PER	0x44E00000	0x44E003FF	Clock Module Peripheral Registers

	Offset	Clock Module Peripheral Register	Value	Description
Power On	0x48	CM_PER_I2C1_CLKCTRL	0x2	Write to enable I2C1 Clock.

BASE REGISTER	Region Name	Start Address	End Address	Description
	I2C1	0x4802A000	0x4802BFFF	I2C1 Registers

	Offset	I2C1 Register	Value	Description
Module Configuration	0xB0	I2C_PSC (Clock Prescalar Register)	0x03	Write for **ICLK** of 12 MHz
	0xB4	I2C_SCLL (SCL Low Time Register)	0x35	Write for **tLOW** to get 100kbps (5us-Low)
	0xB8	I2C_SCLH (SCL High Time Register)	0x37	Write for **tHIGH** to get 100kbps (5us-High)
	0xA8	I2C_OA (Own Address Register)	0x001	Write to configure Own Address
	0xA4	I2C_CON (Configuration Register)	0x8000	Write to take out of reset, enable I2C1 module.
Initialization	0xA4	I2C_CON (Configuration Register)	0xE00	Read-Modify-Write to configure mode. Mode = Master, Transmitter
	0x2C	I2C_IRQENABLE_SET (Interrupt Enable Set Register)	0x0000	Enable polling, No Interrupts (Part 1). Interrupts Enabled (Part 2), Write value for interrupts = 0x0018
	0x94	I2C_BUF (Buffer Configuration Register)	0x0000	Transmit and Receive Threshold before **RRDY** and **XRDY** are active. **TXTRSH** = 0 + 1, **RXTRSH** = 0 + 1.
Pre-Transmission	0xAC	I2C_SA (Slave Address Register)	0x78	Write Slave address value: 1: Newhaven Display = 0x78 2: Sitronix Controller = 0x3C up to 0x3F
	0x98	I2C_CNT (Data Count Register)	0x78	n = Depends on Transmission. Starting Transmission is 0x7
Initiate Transmission	0x24	I2C_IRQSTATUS_RAW (I2C Status Raw Register)	0x00001000	Read **BB**: 1: **BB** is set to 1 after Start Condition. 2: **BB** is set to 0 after Stop Condition.
	0xA4	I2C_CON (Configuration Register)	0x3	Read-Modify-Write to queue Start/Stop Condition. 1: Stop condition will generate when **DCOUNT** passes 0. **STT** = 1, **STP** = 1, Conditions = Start-Stop (**DCOUNT**=n), Bus Activities = S-A-D..(n)..D-P.
Receive Data	0x24	I2C_IRQSTATUS_RAW (I2C Status Raw Register)	0x00000008	Read Mask for reading **RRDY** (polling or interrupt) to see if data is ready to read from **I2C_DATA** Register.
	0x9C	I2C_DATA (Data Access Register)	Read Received Data Byte	If **RRDY** is "1" data is ready for read. **RXTRSH** has been met.
	0x28	I2C_IRQSTATUS (Status Register)	0x00000008	If "1", Read-Modify-Write to Clear **RRDY**
Transmit Data	0x24	I2C_IRQSTATUS_RAW (I2C Status Raw Register)	0x00000010	Read Mask for reading **XRDY** (polling or interrupt) to see if data can be written to **I2C_DATA** Register.
	0x9C	I2C_DATA (Data Access Register)	Write Data Byte to be Transmitted	If **XRDY** is "1" data is ready for write. T**XTRSH** has been met, or anytime there is a read request from external master (for each acknowledge received from the master), if **TXTRSH** = 1.
	0x28	I2C_IRQSTATUS (Status Register)	0x0010	If "1", Read-Modify-Write to clear **XRDY**