



## Single-Chip IEEE 802.11 b/g/n MAC/Baseband/Radio with Bluetooth 4.1 and an FM Receiver

### GENERAL DESCRIPTION

The Broadcom® BCM43438 is a highly integrated single-chip solution and offers the lowest RBOM in the industry for smartphones, wearables, and a wide range of other portable devices. The chip includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/radio, Bluetooth 4.1 support, and an FM receiver. In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

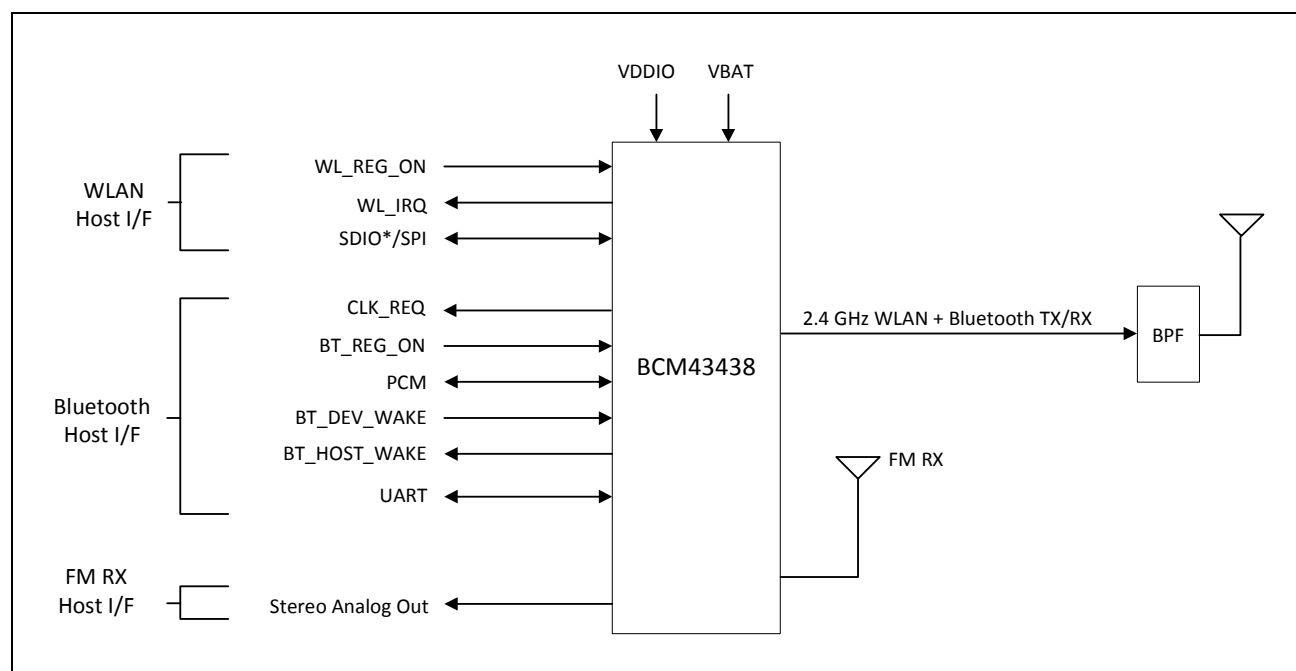
The WLAN host interface supports gSPI and SDIO v2.0 modes, providing a raw data transfer rate up to 200 Mbps when operating in 4-bit mode at a 50 MHz bus frequency. An independent, high-speed UART is provided for the Bluetooth/FM host interface.

### GENERAL DESCRIPTION

Using advanced design techniques and process technology to reduce active and idle power, the BCM43438 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

The BCM43438 implements the world's most advanced Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely collaborative WLAN and Bluetooth coexistence.

**Figure 1: BCM43438 System Block Diagram**



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**FEATURES****IEEE 802.11x Key Features**

- Single-band 2.4 GHz IEEE 802.11b/g/n
- Single-stream IEEE 802.11n.
- Support for TurboQAM® (MCS-8 86 Mbps and MCS-9 96 Mbps) HT20, 20 MHz channel bandwidth.
- Integrated iTR switch supports a single 2.4 GHz antenna shared between WLAN and Bluetooth.
- Supports explicit IEEE 802.11n transmit beamforming.
- Supports standard SDIO v2.0 and gSPI host interfaces.
- Integrated ARM® Cortex-M3™ processor and on-chip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features. On-chip memory includes 512 KB SRAM and 640 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as to future devices.

**Bluetooth and FM Key Features**

- Complies with Bluetooth Core Specification Version 4.1 with provisions for supporting future specifications.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference.
- Interface support—Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data.

**FEATURES****Bluetooth and FM Key Features (Continued)**

- The FM receiver unit supports HCI for communication.
- Low power consumption improves battery life of handheld devices.
- FM receiver: 65 MHz to 108 MHz FM bands; supports the European Radio Data Systems (RDS) and the North American Radio Broadcast Data System (RBDS) standards
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.

**General Features**

- Supports a battery voltage range from 3.0V to 4.8V with an internal switching regulator.
- Programmable dynamic power management.
- 4 Kbit One-Time Programmable (OTP) memory for storing board parameters.
- Can be routed on low-cost 1–x–1 PCB stack-ups.
- 63-ball WLPGA package (4.87 mm × 2.87 mm, 0.4 mm pitch)
- Security:
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES in WLAN hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

## Revision History

<b>Revision</b>	<b>Date</b>	<b>Change Description</b>
43438-DS101-R	4/07/14	<b>Added:</b> <ul style="list-style-type: none"><li>• “External Coexistence Interface” on page 75.</li></ul> <b>Updated:</b> <ul style="list-style-type: none"><li>• “GPIO Interface” on page 75.</li><li>• Figure 33: “63-Ball WLBGA Ball Map (Top View),” on page 80</li><li>• Table 16: “WLBGA Signal Descriptions,” on page 84.</li><li>• Table 21: “Environmental Ratings,” on page 93.</li><li>• Table 23: “Recommended Operating Conditions and DC Characteristics,” on page 94.</li><li>• Table 25: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 97.</li><li>• Table 26: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 100.</li></ul>
43438-DS100-R	3/18/14	Initial release

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## About This Document

### Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM43438. It is intended for hardware design, application, and OEM engineers.

### Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to:

<http://www.broadcom.com/press/glossary.php>.

### Document Conventions

The following conventions may be used in this document:

Convention	Description
<b>Bold</b>	User input and actions: for example, type <b>exit</b> , click <b>OK</b> , press <b>Alt+C</b>
Monospace	Code: <code>#include &lt;iostream&gt;</code> HTML: <code>&lt;td rowspan = 3&gt;</code> Command line commands and parameters: <code>wl [-1] &lt;command&gt;</code>
<code>&lt; &gt;</code>	Placeholders for <i>required</i> elements: enter your <code>&lt;username&gt;</code> or <code>wl &lt;command&gt;</code>
<code>[]</code>	Indicates <i>optional</i> command-line parameters: <code>wl [-1]</code> Indicates bit and byte ranges (inclusive): <code>[0:3]</code> or <code>[7:0]</code>

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## Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (<https://support.broadcom.com>). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (<http://www.broadcom.com/support/>).

# Section 1: Overview

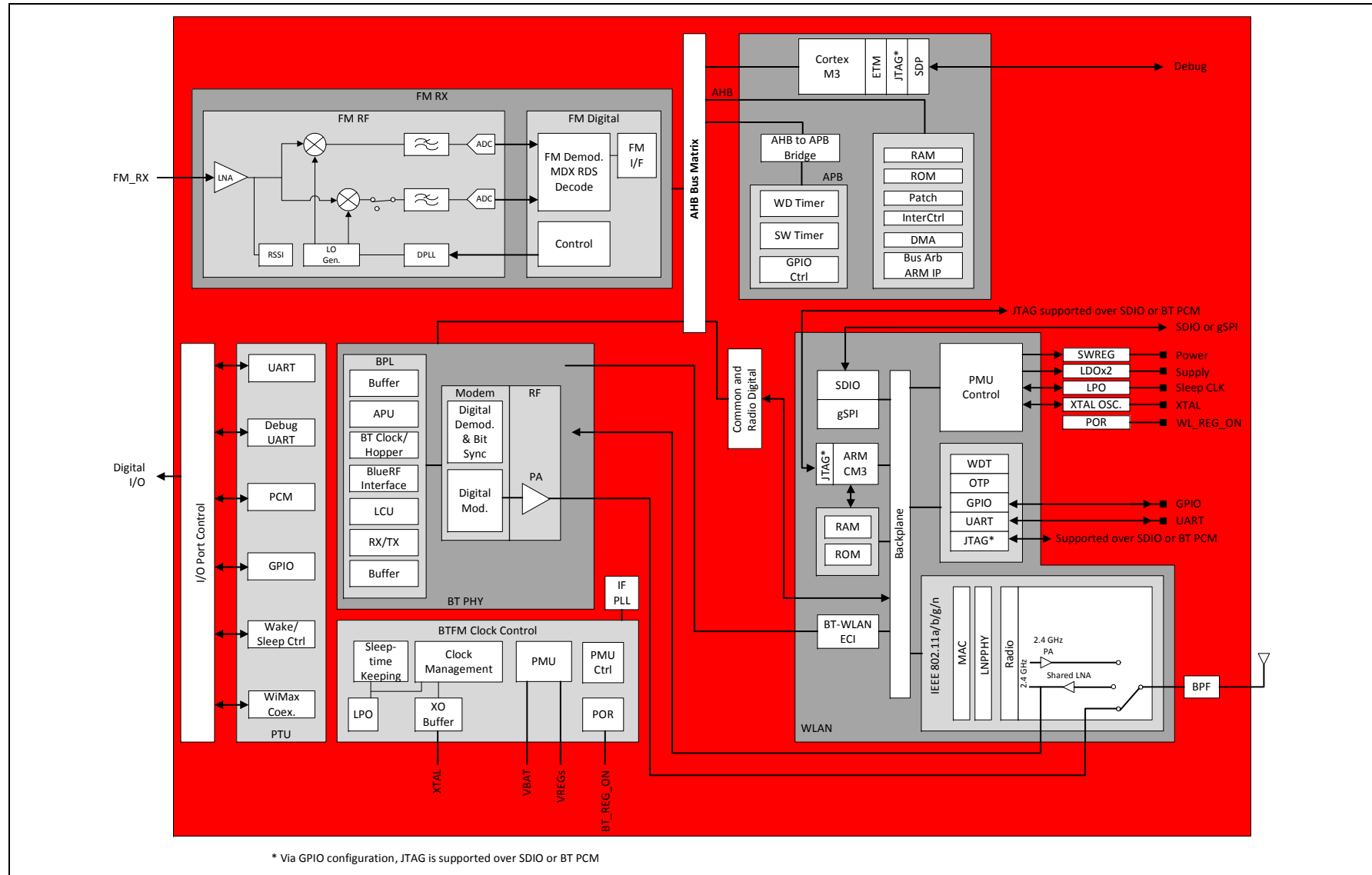
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## Overview

The Broadcom® BCM43438 provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The BCM43438 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

[Figure 2 on page 16](#) shows the interconnection of all the major physical blocks in the BCM43438 and their associated external interfaces, which are described in greater detail in subsequent sections.

Figure 2: BCM43438 Block Diagram



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## Features

The BCM43438 supports the following WLAN, Bluetooth, and FM features:

- IEEE 802.11b/g/n single-band radio with an internal power amplifier, LNA, and T/R switch
- Bluetooth v4.1 with integrated Class 1 PA
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Simultaneous BT/WLAN reception with a single antenna
- WLAN host interface options:
  - SDIO v2.0, including default and high-speed timing.
  - gSPI—up to a 50 MHz clock rate
- BT UART (up to 4 Mbps) host digital interface that can be used concurrently with the above WLAN host interfaces.
- ECI—enhanced coexistence support, which coordinates BT SCO transmissions around WLAN receptions.
- PCM for FM/BT audio, HCI for FM block control
- HCI high-speed UART (H4, H4+, H5) transport support
- Wideband speech support (16 bits, 16 kHz sampling PCM, through PCM interfaces)
- Bluetooth SmartAudio® technology improves voice and music quality to headsets.
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- FM advanced internal antenna support
- FM auto searching/tuning functions
- FM multiple audio routing options: PCM, eSCO, and A2DP
- FM mono-stereo blending and switching, and soft mute support
- FM audio pause detection support
- Multiple simultaneous A2DP audio streams
- FM over Bluetooth operation and on-chip stereo headset emulation

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## Standards Compliance

The BCM43438 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.1 (Bluetooth Low Energy)
- 65 MHz to 108 MHz FM bands (US, Europe, and Japan)
- IEEE 802.11n—Handheld Device Class (Section 11)
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The BCM43438 will support the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
- IEEE 802.11i MAC Enhancements
- IEEE 802.11r Fast Roaming Support
- IEEE 802.11k Radio Resource Measurement

The BCM43438 supports the following security features and proprietary protocols:

- Security:
  - WEP
  - WPA™ Personal
  - WPA2™ Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - WAPI
  - AES (Hardware Accelerator)
  - TKIP (host-computed)
  - CKIP (SW Support)
- Proprietary Protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3-wire requirements.

## Section 2: Power Supplies and Power Management

### Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the BCM43438. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, WLAN, and FM functions in embedded designs.

A single VBAT (3.0V to 4.8V DC maximum) and VDDIO supply (1.8V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM43438.

Two control signals, BT\_REG\_ON and WL\_REG\_ON, are used to power up the regulators and take the respective circuit blocks out of reset. The CBUCK CLDO and LNLDO power up when any of the reset signals are deasserted. All regulators are powered down only when both BT\_REG\_ON and WL\_REG\_ON are deasserted. The CLDO and LNLDO can be turned on and off based on the dynamic demands of the digital baseband.

The BCM43438 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, LPLDO1 provides the BCM43438 with all required voltage, further reducing leakage currents.



**Note:** VBAT should be connected to the LDO\_VDDBAT5V and SR\_VDDBAT5V pins of the device.



**Note:** VDDIO should be connected to the WCC\_VDDIO pin of the device.

## BCM43438 PMU Features

The PMU supports the following:

- VBAT to 1.35Vout (170 mA nominal, 370 mA maximum) Core-Buck (CLOCK) switching regulator
- VBAT to 3.3Vout (250 mA nominal, 450 mA maximum 800 mA peak maximum) LDO3P3
- 1.35V to 1.2Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35V to 1.2Vout (80 mA nominal, 200 mA maximum) CLDO with bypass mode for deep sleep
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode.

[Figure 3 on page 21](#) and [Figure 4 on page 22](#) show the typical power topology of the BCM43438.

WCC\_VDDIO also provides an internal supply to LPLDO1. LPLDO1 is active during PMU sleep mode when CBUCK is off.

Figure 3: Typical Power Topology (1 of 2)

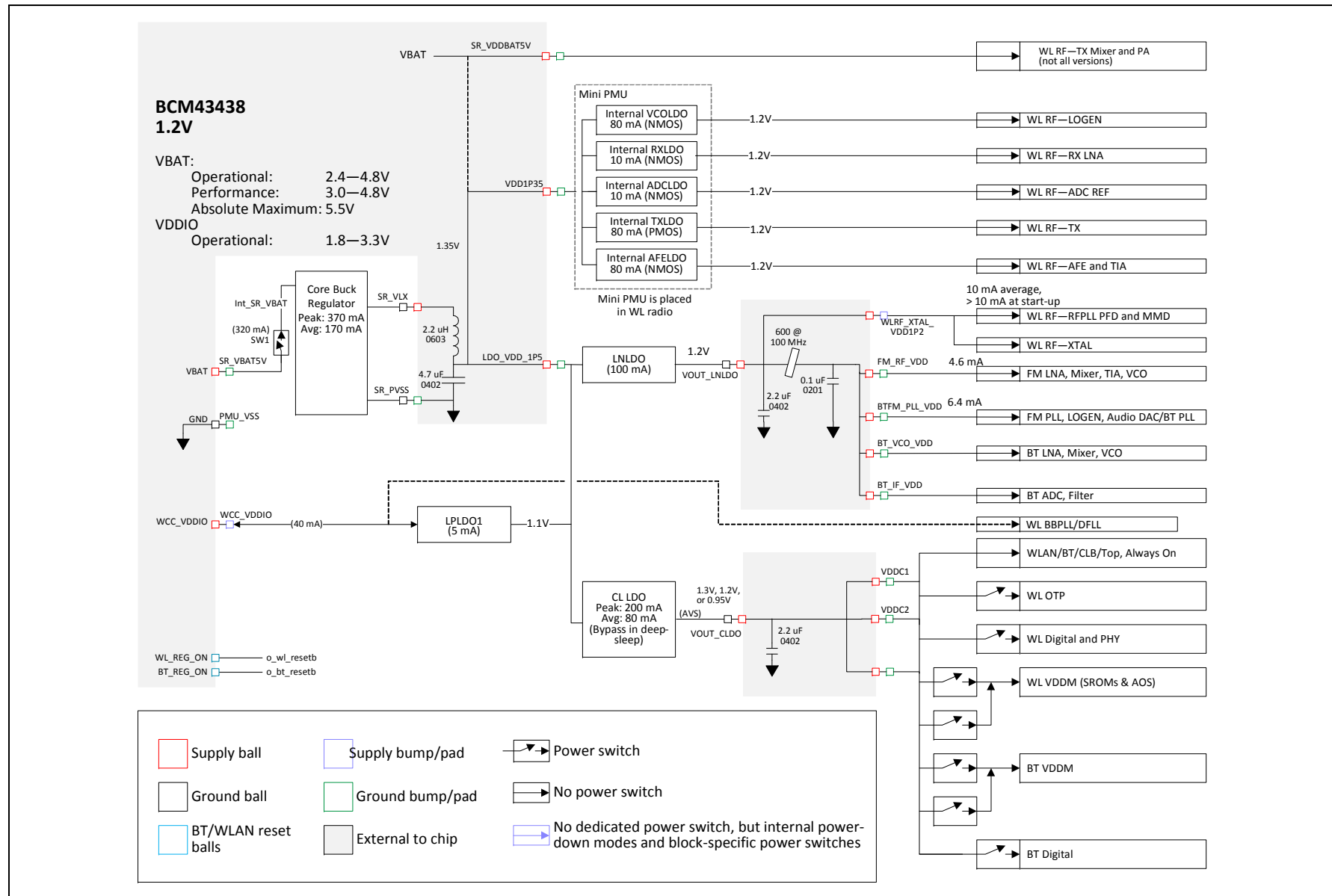
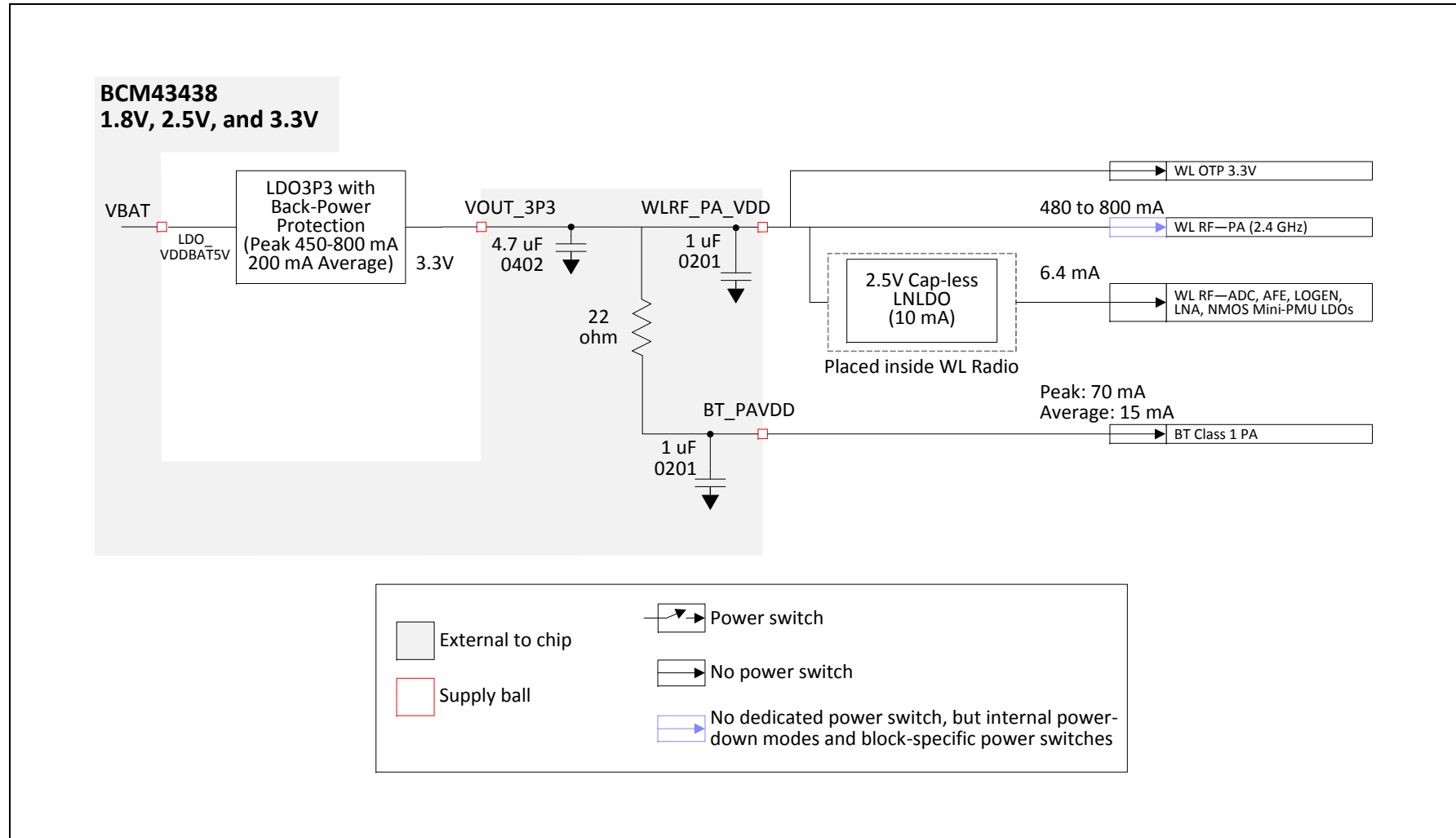


Figure 4: Typical Power Topology (2 of 2)



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## WLAN Power Management

The BCM43438 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43438 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the BCM43438 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43438 into various power management states appropriate to the operating environment and the activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at the 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM43438 WLAN power states are described as follows:

- **Active mode**—All WLAN blocks in the BCM43438 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Doze mode**—The radio, analog domains, and most of the linear regulators are powered down. The rest of the BCM43438 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- **Deep-sleep mode**—Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware reinitialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- **Power-down mode**—The BCM43438 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

---

## PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests can derive from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of the following four states:

- enabled
- disabled
- transition\_on
- transition\_off

The timer value is 0 when the resource is enabled or disabled and nonzero during state transition. The timer is loaded with the time\_on or time\_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition\_off to disabled or transition\_on to enabled. If the time\_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time\_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.



## Power-Off Shutdown

The BCM43438 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the BCM43438 is not needed in the system, VDDIO\_RF and VDDC are shut down while VDDIO remains powered. This allows the BCM43438 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the BCM43438, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the BCM43438 to be fully integrated in an embedded device and to take full advantage of the lowest power-savings modes.

When the BCM43438 is powered on from this state, it is the same as a normal power-up, and the device does not retain any information about its state from before it was powered down.

## Power-Up/Power-Down/Reset Circuits

The BCM43438 has two signals (see [Table 1](#)) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see [Section 22: “Power-Up Sequence and Timing,” on page 127](#).

**Table 1: Power-Up/Power-Down/Reset Control Signals**

<b>Signal</b>	<b>Description</b>
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal BCM43438 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM43438 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming.

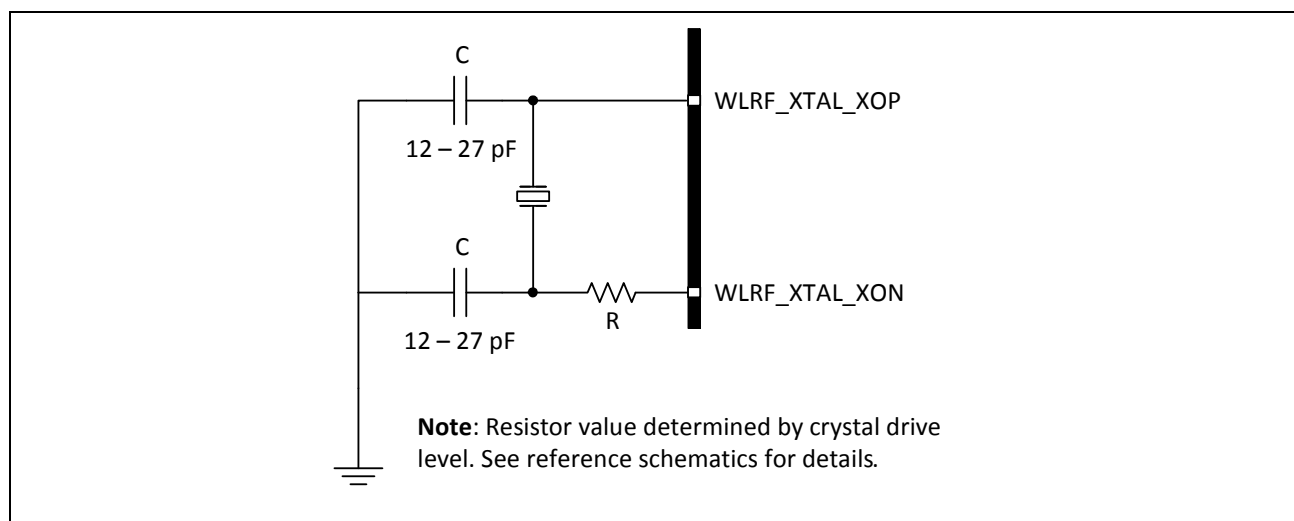
## Section 3: Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

### Crystal Interface and Clock Generation

The BCM43438 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in [Figure 5](#). Consult the reference schematics for the latest configuration.

**Figure 5: Recommended Oscillator Configuration**



The BCM43438 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing so that it can operate using numerous frequency references. The frequency reference can be an external source such as a TCXO or a crystal interfaced directly to the BCM43438.

The default frequency reference setting is a 37.4 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in [Table 2 on page 27](#).



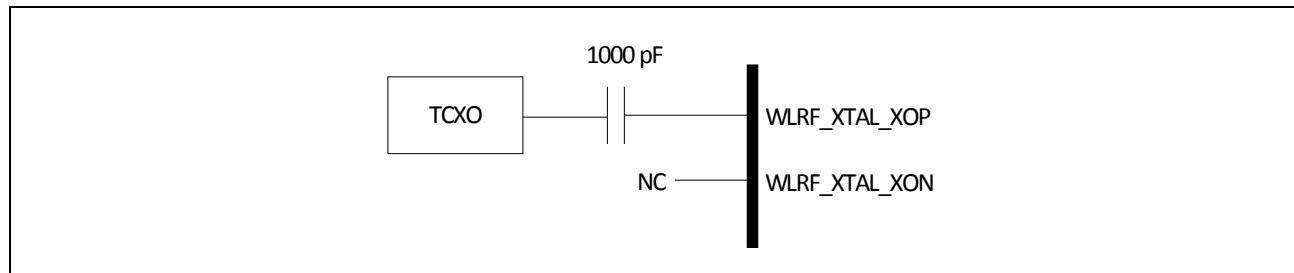
**Note:** Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

## TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the phase noise requirements listed in [Table 2 on page 27](#).

If the TCXO is dedicated to driving the BCM43438, it should be connected to the WLRF\_XTAL\_XOP pin through an external 1000 pF coupling capacitor as shown in [Figure 6](#).

**Figure 6: Recommended Circuit to Use with an External Dedicated TCXO**



**Table 2: Crystal Oscillator and External Clock Requirements and Performance**

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	–	–	37.4 <sup>a</sup>	–	–	–	–	MHz
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input Impedance (WLRF_XTAL_XOP)	Resistive				10k	100k	–	Ω
	Capacitive				–	–	7	pF
WLRF_XTAL_XOP input voltage	AC-coupled analog signal				400 <sup>b</sup>	–	1260	mV <sub>p-p</sub>
WLRF_XTAL_XOP input low level	DC-coupled digital signal				0	–	0.2	V
WLRF_XTAL_XOP input high level	DC-coupled digital signal				1.0	–	1.26	V
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	37.4 MHz clock				40	50	60	%
Phase Noise <sup>c, d, e</sup> (IEEE 802.11 b/g)	37.4 MHz clock at 10 kHz offset				–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset				–	–	–136	dBc/Hz
Phase Noise <sup>c, d, e</sup> (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset				–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset				–	–	–141	dBc/Hz

**Table 2: Crystal Oscillator and External Clock Requirements and Performance (Cont.)**

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Phase Noise <sup>c, d, e</sup> (256-QAM)	37.4 MHz clock at 10 kHz offset				–	–	–140	dBc/Hz
	37.4 MHz clock at 100 kHz offset				–	–	–147	dBc/Hz

- The frequency step size is approximately 80 Hz. The BCM43438 does not auto-detect the reference clock frequency; the frequency is specified in the software and/or NVRAM file.
- To use 256-QAM, a 800 mV minimum voltage is required.
- For a clock reference other than 37.4 MHz,  $20 \times \log_{10}(f/37.4)$  dB should be added to the limits, where f = the reference clock frequency in MHz.
- Phase noise is assumed flat above 100 kHz.
- The BCM43438 supports a 26 MHz reference clock sharing option. See the phase noise requirement in the table.

## External 32.768 kHz Low-Power Oscillator

The BCM43438 uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz  $\pm$  30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in [Table 3 on page 29](#).



**Note:** The BCM43438 will auto-detect the LPO clock. If it senses a clock on the EXT\_SLEEP\_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT\_SLEEP\_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT\_SLEEP\_CLK.

**Table 3: External 32.768 kHz Low-Power Oscillator Specifications**

<b>Symbol</b>	<b>Parameter</b>	<b>Condition/Notes</b>	<b>Specification</b>			<b>Units</b>
			<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	
Fr	Frequency	–	–	32768	–	Hz
$\Delta f/fr$	Frequency tolerance	At 25°C	–30	–	+30	ppm
		–20°C <Ta< +70°C	–150	–	+40	
		–30°C <Ta< +85°C	–220	–	+40	
Duty cycle	–	–	30	–	70	%
Vol	Output low voltage	–	0	–	0.2	V
Voh	Output high voltage	–	0.7 × VDDIO	–	VDDIO	V
Tr/Tf	Rise and fall time	–	–	–	100	ns
–	Signal type	Digital	–	–	–	–
–	Clock jitter	Integrated over 300 Hz to 15 kHz	–	–	30	ns
–	Input impedance	Resistive	10	–	–	MΩ
		Capacitive	–	–	2	pF
–	Input amplitude	Fail safe, 3.3V digital I/O	–	–	3.63	V

# Section 4: WLAN System Interfaces

## SDIO v2.0

The BCM43438 WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See [Table 17 on page 88](#) for details.

Three functions are supported:

- Function 0 standard SDIO function. The maximum block size is 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

## SDIO Pin Descriptions

Table 4: SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used	NC	Not used
DATA3	Data line 3	NC	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 7: Signal Connections to SDIO Host (SD 4-Bit Mode)

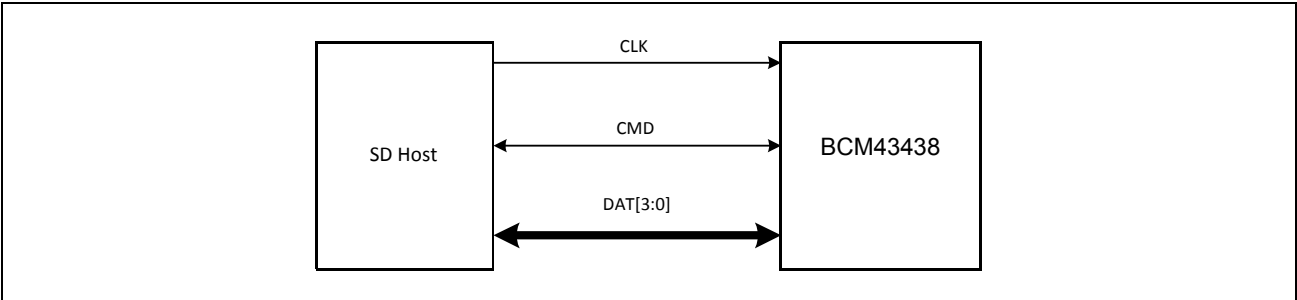
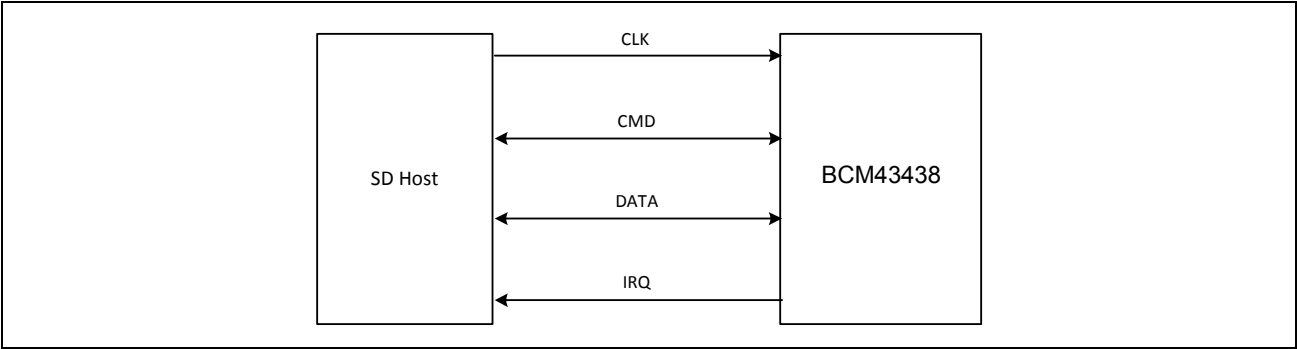


Figure 8: Signal Connections to SDIO Host (SD 1-Bit Mode)



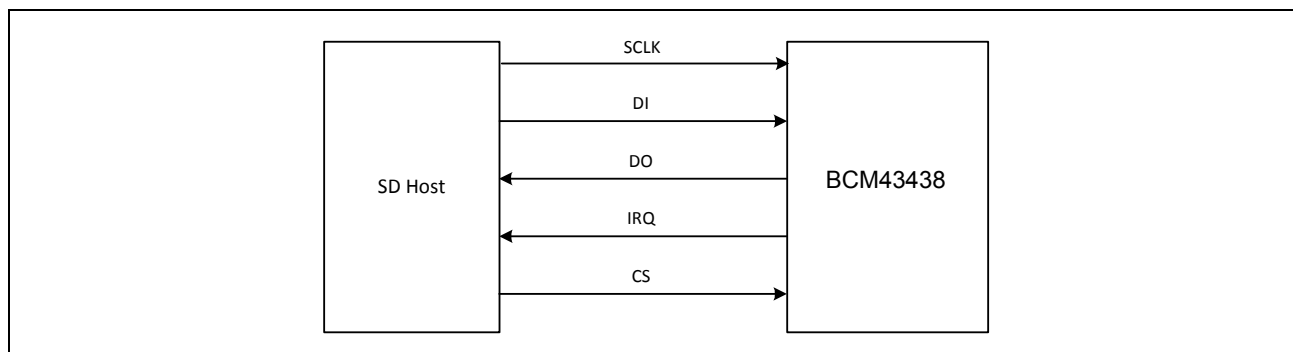
## Generic SPI Mode

In addition to the full SDIO mode, the BCM43438 includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Up to 50 MHz operation
- Fixed delays for responses and data from the device
- Alignment to host gSPI frames (16 or 32 bits)
- Up to 2 KB frame size per transfer
- Little-endian and big-endian configurations
- A configurable active edge for shifting
- Packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins. See [Table 17 on page 88](#) for details.

**Figure 9: Signal Connections to SDIO Host (gSPI Mode)**





# SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianness is supported in both modes. [Figure 10](#) and [Figure 11 on page 34](#) show the basic write and write/read commands.

Figure 10: gSPI Write Protocol

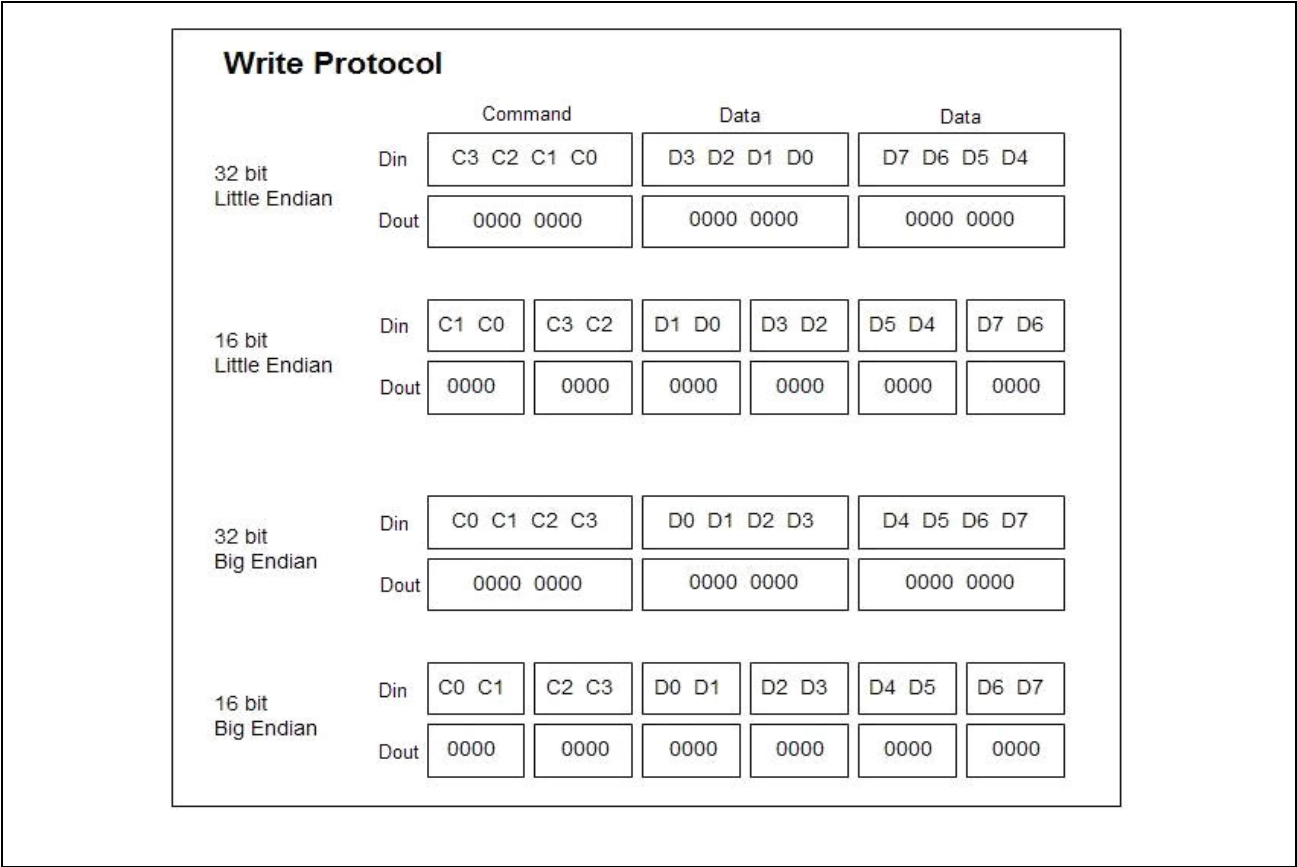
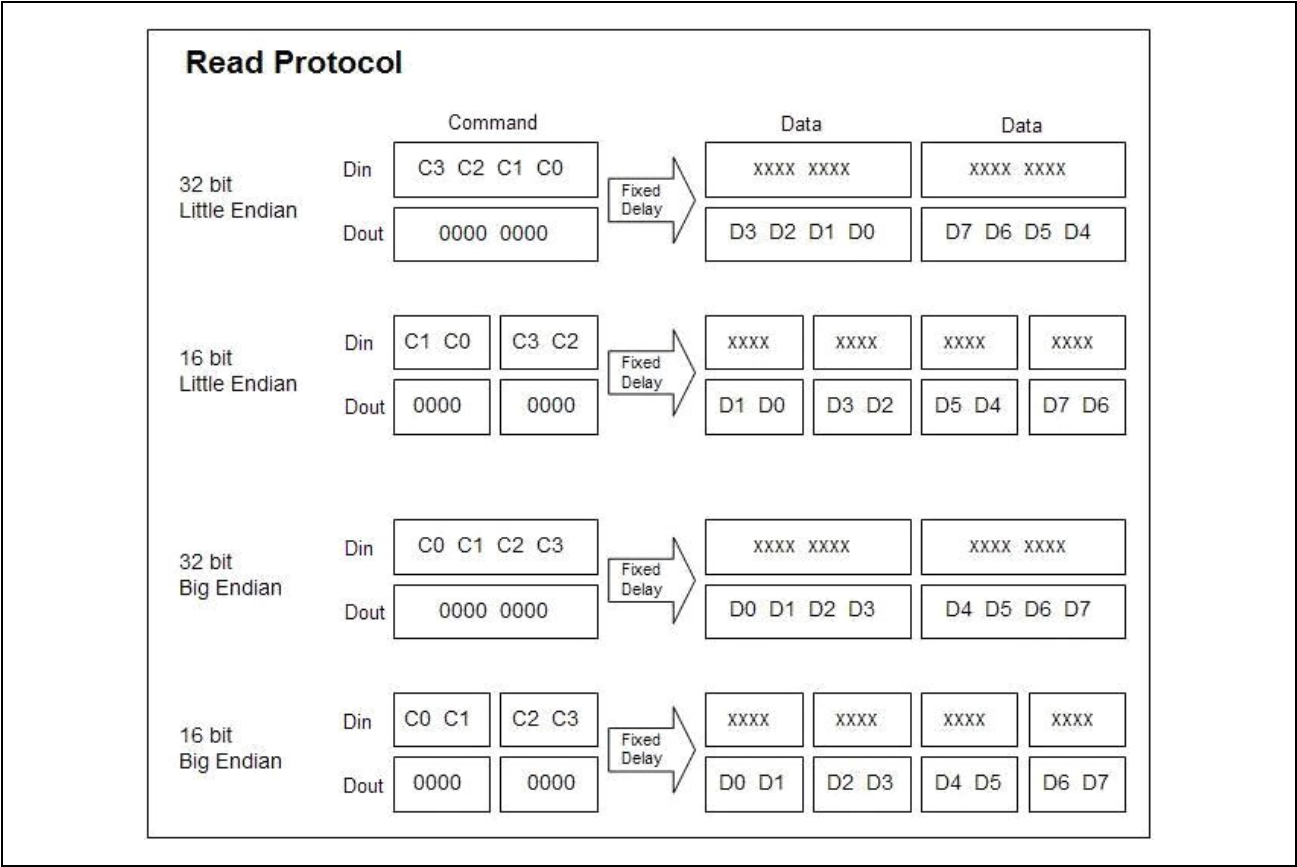


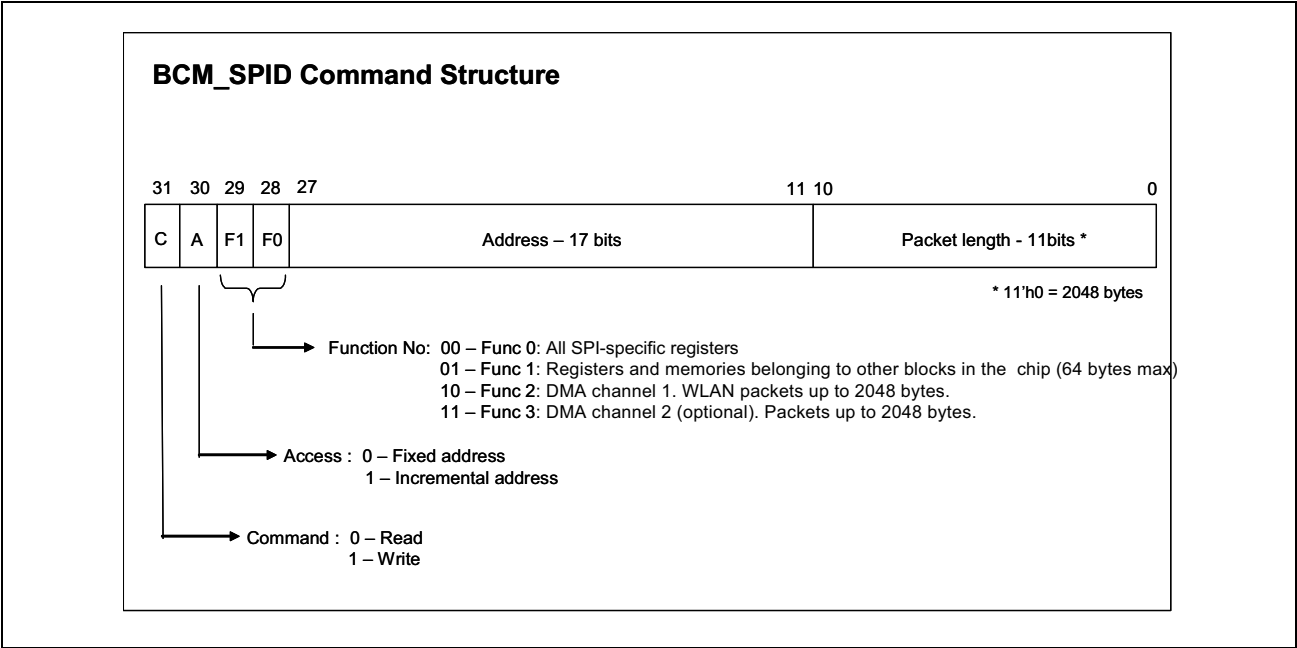
Figure 11: gSPI Read Protocol



Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are shown in [Figure 12](#).

Figure 12: gSPI Command Structure



Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising-clock edge of the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

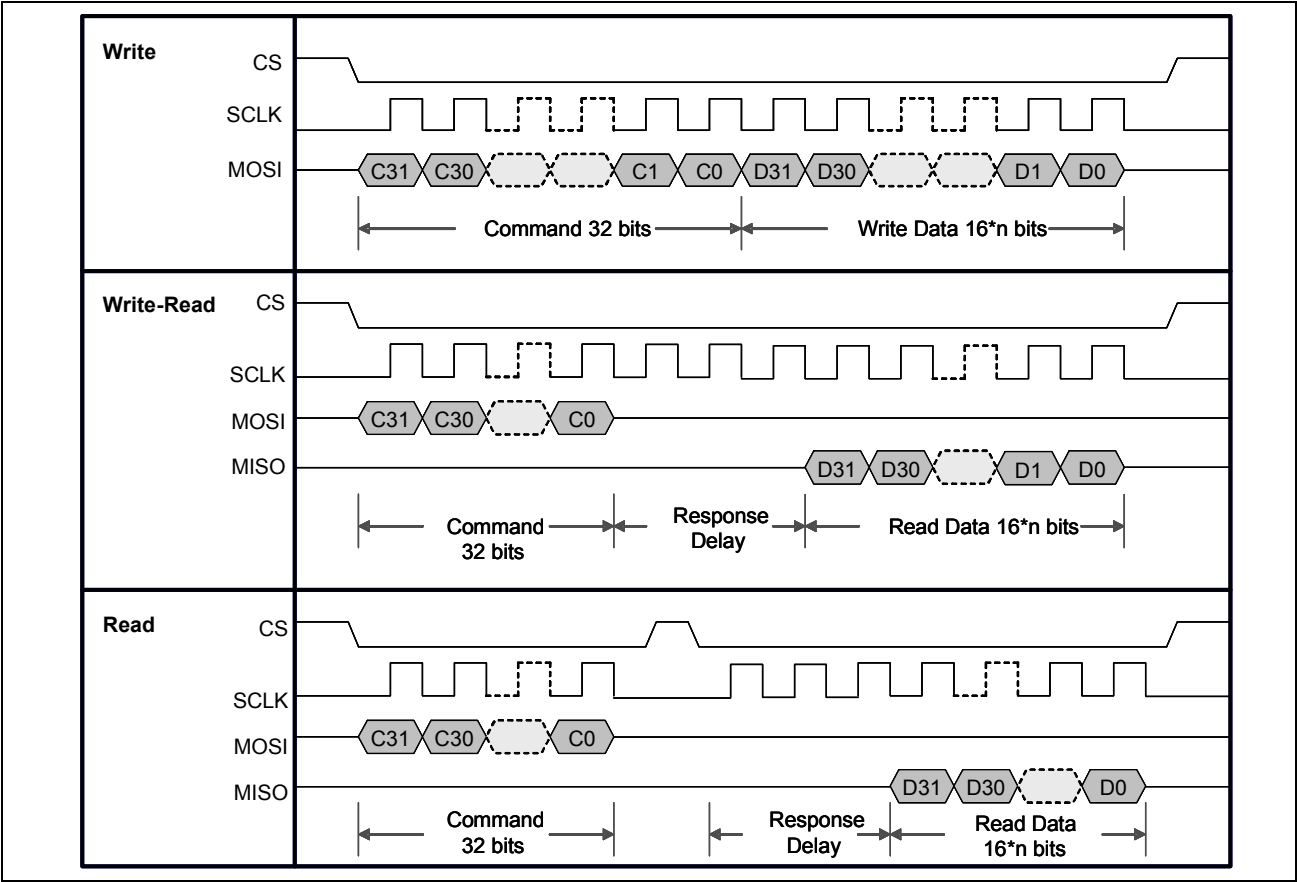
Read

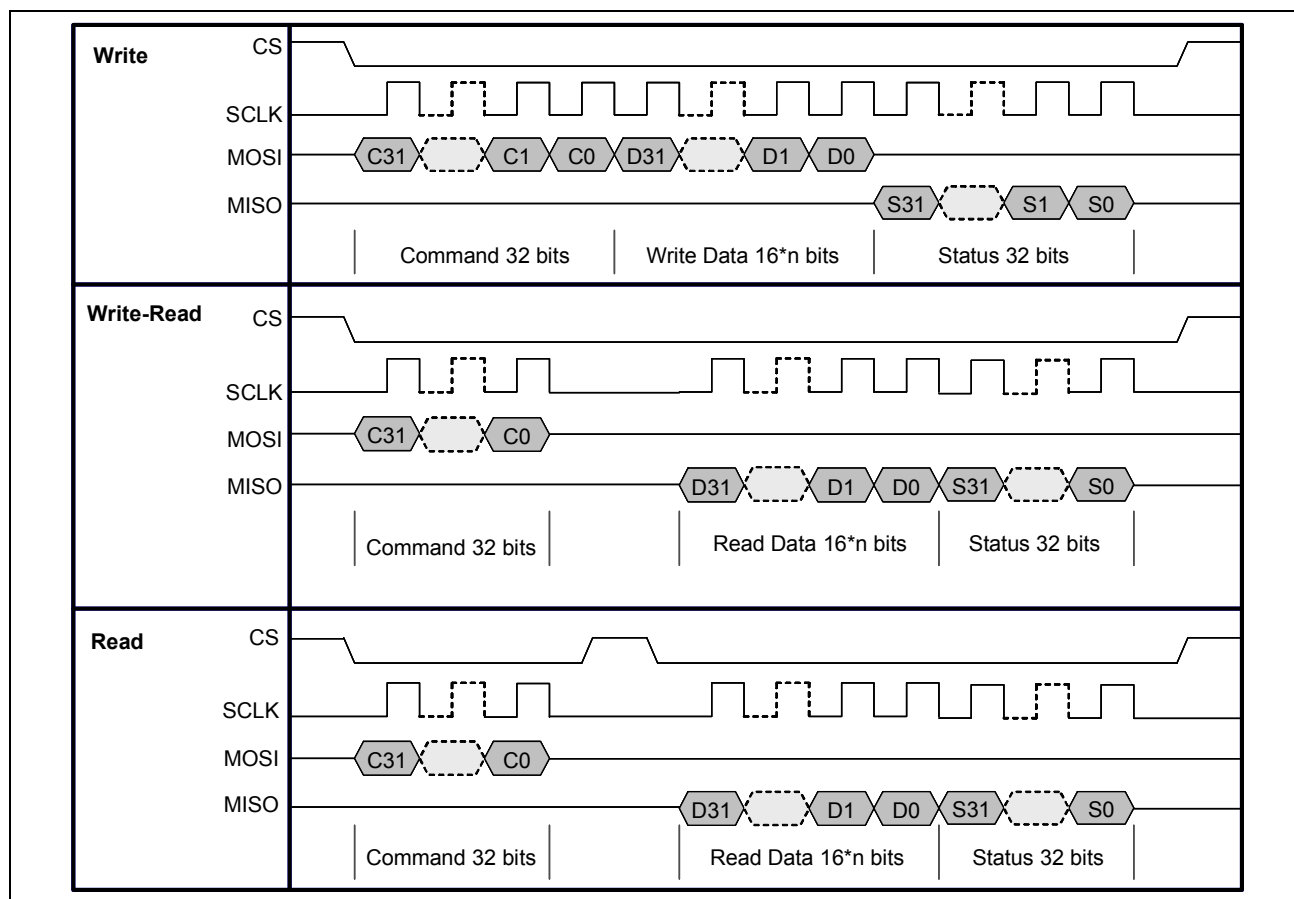
The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data, and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about packet errors, protocol errors, available packets in the RX queue, etc. The status information helps reduce the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 13 below and Figure 14 on page 37. See Table 5 on page 37 for information on status-field details.

Figure 13: gSPI Signal Timing Without Status



**Figure 14: gSPI Signal Timing with Status (Response Delay = 0)****Table 5: gSPI Status Field Details**

Bit	Name	Description
0	Data not available	The requested read data is not available.
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command.
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command.
3	F2 interrupt	F2 channel interrupt
5	F2 RX ready	F2 FIFO is ready to receive data (FIFO empty).
7	Reserved	—
8	F2 packet available	Packet is available/ready in F2 TX FIFO.
9:19	F2 packet length	Length of packet available in F2 FIFO

## gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM43438 is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of the interrupt and then take necessary actions.

## Boot-Up Sequence

After power-up, the gSPI host needs to wait 50 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 address 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wake-up WLAN bit (F0 reg 0x00 bit 7). Wake-up WLAN turns the PLL on; however, the PLL doesn't lock until the host programs the PLL registers to set the crystal frequency.

For the first time after power-up, the host needs to wait for the availability of the low-power clock inside the device. Once it is available, the host needs to write to a PMU register to set the crystal frequency. This will turn on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This indicates device awake/ready status. See [Table 6](#) for information on gSPI registers.

In [Table 6](#), the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

**Table 6: gSPI Registers**

Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16-bit word length 1: 32-bit word length
	Endianness	1	R/W/U	0	0: Little endian 1: Big endian
	High-speed mode	4	R/W/U	1	0: Normal mode. Sample on SPICLK rising edge, output on falling edge. 1: High-speed mode. Sample and output on rising edge of SPICLK (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low. 1: Interrupt active polarity is high (default).
	Wake-up	7	R/W	0	A write of 1 denotes a wake-up command from host to device. This will be followed by an F2 interrupt from the gSPI device to host, indicating device awake status.

**Table 6: gSPI Registers (Cont.)**

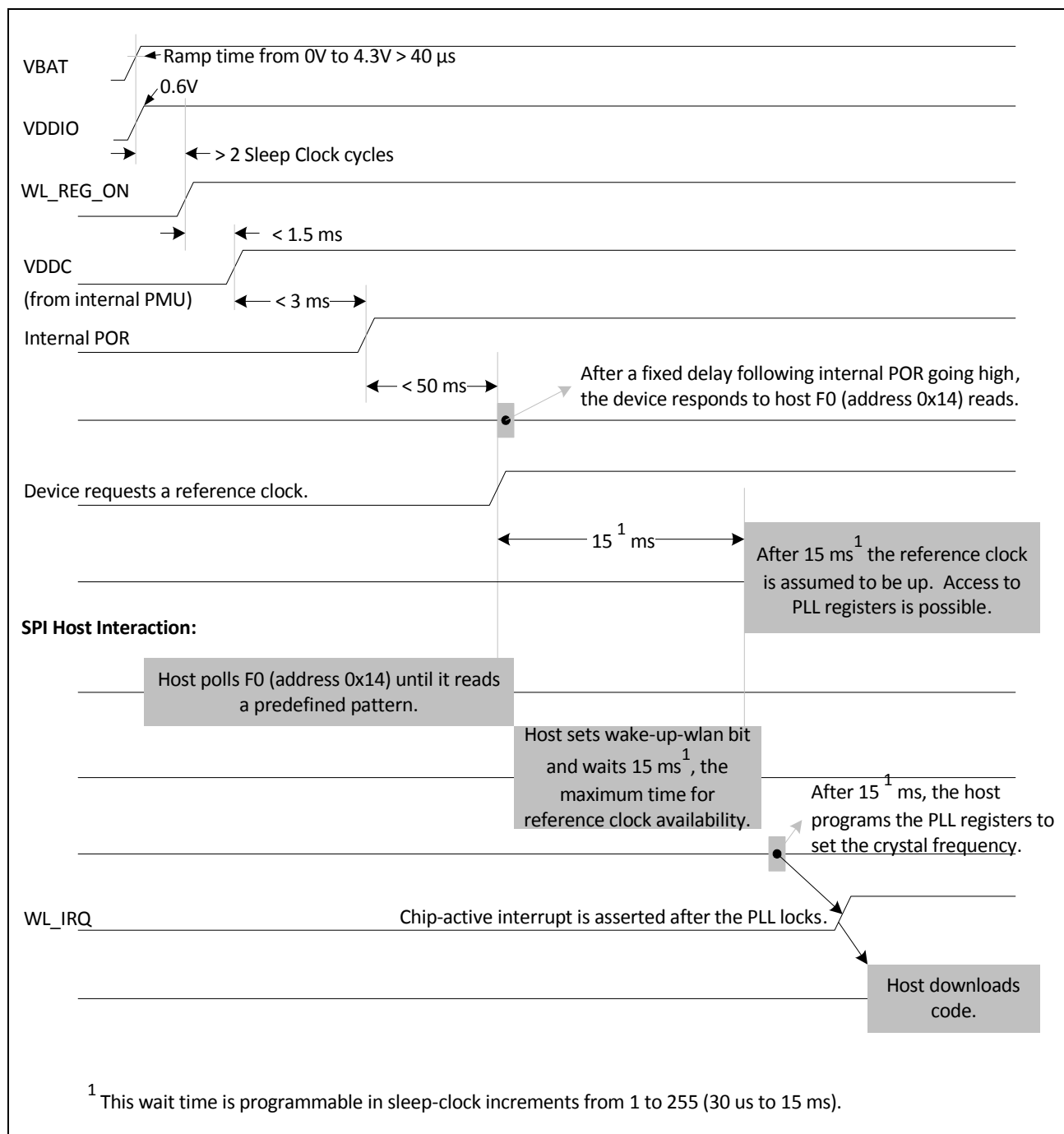
Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0: No status sent to host after a read/write. 1: Status sent to host after a read/write.
	Interrupt with status	1	R/W	0	0: Do not interrupt if status is sent. 1: Interrupt host even if status is sent.
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available. Cleared by writing a 1 to this location.
		1	R	0	F2/F3 FIFO underflow from the last read.
		2	R	0	F2/F3 FIFO overflow from the last write.
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow from the last write.
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006, x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular interrupt is enabled if a corresponding bit is set.
x0008 to x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C, x000D	F1 info. register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 maximum packet size
x000E, x000F	F2 info. register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 maximum packet size
x0014 to x0017	Test-Read only register	31:0	R	32'hFEEDB EAD	This register contains a predefined pattern, which the host can read to determine if the gSPI interface is working properly.
x0018 to x001B	Test-R/W register	31:0	R/W/U	32'h000000 00	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.
x001C to x001F	Response delay registers	7:0	R/W	0x1D = 4, other registers = 0	Individual response delays for F0, F1, F2, and F3. The value of the registers is the number of byte delays that are introduced before data is shifted out of the gSPI interface during host reads.

Figure 15 on page 40 shows the WLAN boot-up sequence from power-up to firmware download, including the initial device power-on reset (POR) evoked by the WL\_REG\_ON signal. After initial power-up, the WL\_REG\_ON signal can be held low to disable the BCM43438 or pulsed low to induce a subsequent reset.



**Note:** The BCM43438 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 3 ms after VDDC and VDDIO have both passed the 0.6V threshold.

Figure 15: WLAN Boot-Up Sequence





## Section 5: Wireless LAN MAC and PHY

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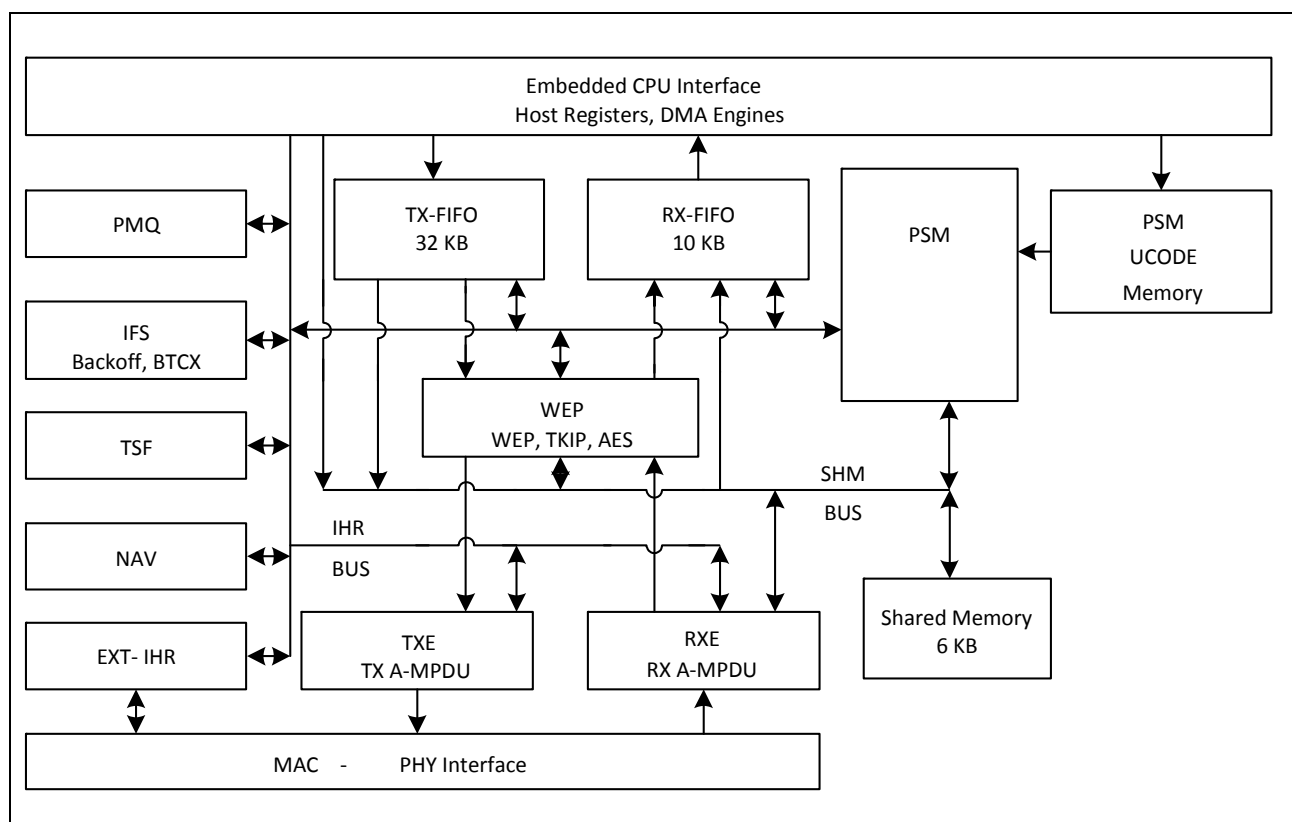
### MAC Features

The BCM43438 WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU).
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies.
- Interframe space timing support, including RIFS.
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges.
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification.
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware.
- Hardware off-load for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management.
- Support for coexistence with Bluetooth and other external radios.
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support.

### MAC Description

The BCM43438 WLAN MAC is designed to support high throughput operation with low-power consumption. It does so without compromising on Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes that have been implemented allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in [Figure 16 on page 42](#).

**Figure 16: WLAN MAC Architecture**

The following sections provide an overview of the important modules in the MAC.

## PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratch-pad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are collocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, an instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratch-pad memory, IHRs, or instruction literals, and the results are written into the shared memory, scratch-pad memory, or IHRs.

There are two basic branch instructions: conditional branches and ALU-based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs) or on the results of ALU operations.

## WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as the MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, and WPA2 AES-CCMP.

Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames. WAPI is also supported.

## TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

## RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RX FIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RX FIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

## IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple back-off engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The back-off engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the back-off counters. When the back-off counters reach 0, the TXE gets notified so that it may commence frame transmission. In the event of multiple back-off counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power-saving mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

## TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

## NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

## MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

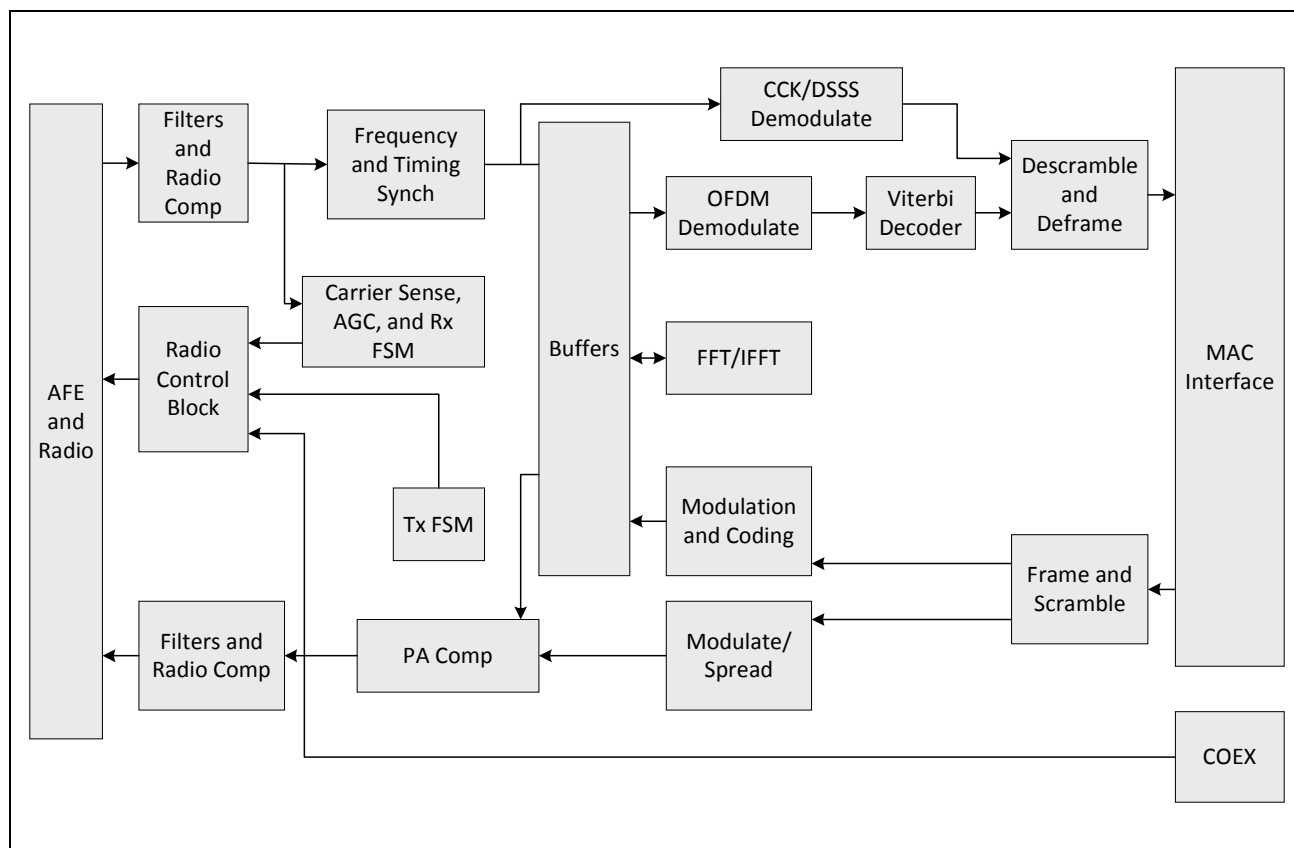
## PHY Description

The BCM43438 WLAN digital PHY is designed to comply with IEEE 802.11b/g/n single stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 96 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to meet specification requirements in the presence of interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/IEEE 802.11b hybrid networks with Bluetooth coexistence.

## PHY Features

- Supports the IEEE 802.11b/g/n single-stream standards.
- Supports explicit IEEE 802.11n transmit beamforming.
- Supports optional Greenfield mode in TX and RX.
- Supports IEEE 802.11h/d for worldwide operation.
- Algorithms achieving low power, enhanced sensitivity, range, and reliability.
- Algorithms to maximize throughput performance in the presence of Bluetooth signals.
- Automatic gain control scheme for blocking and nonblocking application scenarios for cellular applications.
- Closed-loop transmit power control.
- Designed to meet FCC and other regulatory requirements.

**Figure 17: WLAN PHY Block Diagram**

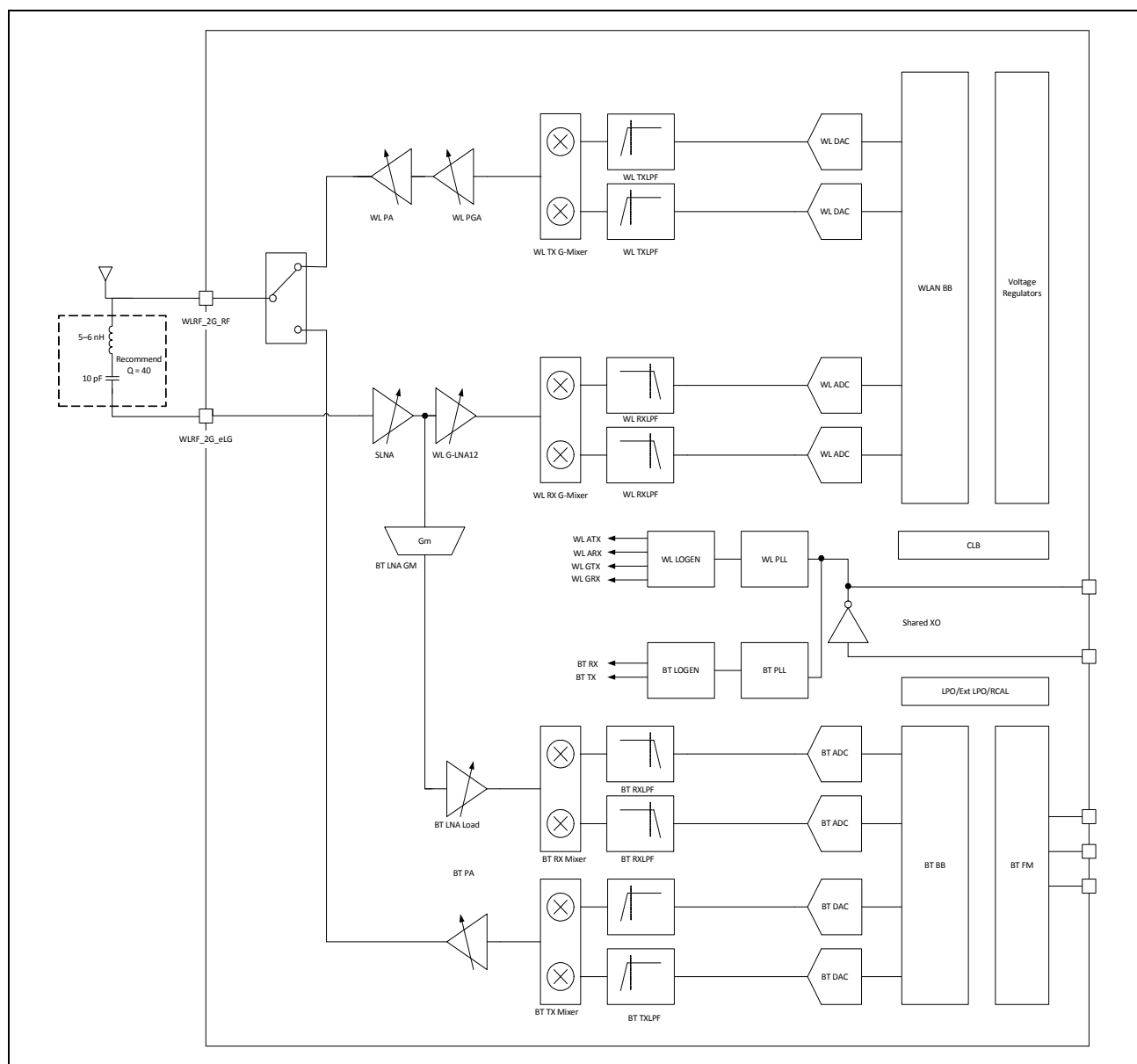
The PHY is capable of fully calibrating the RF front-end to extract the highest performance. On power-up, the PHY performs a full calibration suite to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift, thus maintaining high-performance over time. A closed-loop transmit control algorithm maintains the output power at its required level and can control TX power on a per-packet basis.

## Section 6: WLAN Radio Subsystem

The BCM43438 includes an integrated WLAN RF transceiver that has been optimized for use in 2.4 GHz Wireless LAN systems. It is designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions. Improvements to the radio design include shared TX/RX baseband filters and high immunity to supply noise.

Figure 18 shows the radio functional block diagram.

**Figure 18: Radio Functional Block Diagram**



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## Receive Path

The BCM43438 has a wide dynamic range, direct conversion receiver. It employs high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band.

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## Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. A linear on-chip power amplifier is included, which is capable of delivering high output powers while meeting IEEE 802.11b/g/n specifications without the need for an external PA. This PA can be powered directly from VBAT, thereby eliminating the need for a separate PALDO. Closed-loop output power control is integrated.

---

## Calibration

The BCM43438 features dynamic on-chip calibration, eliminating process variation across components. This enables the BCM43438 to be used in high-volume applications because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically during normal radio operation. Automatic calibration examples include baseband filter calibration for optimum transmit and receive performance and LOFT calibration for leakage reduction. In addition, I/Q calibration, R calibration, and VCO calibration are performed on-chip.



## Section 7: Bluetooth + FM Subsystem Overview

The Broadcom BCM43438 is a Bluetooth 4.1-compliant, baseband processor and 2.4 GHz transceiver with an integrated FM/RDS/RBDS receiver. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth plus FM radio solution.

The BCM43438 is the optimal solution for any Bluetooth voice and/or data application that also requires an FM radio receiver. The Bluetooth subsystem presents a standard Host Controller Interface (HCI) via a high speed UART and PCM interface for audio. The FM subsystem supports the HCI control interface as well as PCM and stereo analog interfaces. The BCM43438 incorporates all Bluetooth 4.1 features including secure simple pairing, sniff subrating, and encryption pause and resume.

The BCM43438 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with any of the standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS, WLAN, NFC, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

---

### Features

#### Major Bluetooth features of the BCM43438 include:

- Supports key features of upcoming Bluetooth standards
- Fully supports Bluetooth Core Specification version 4.1 plus enhanced data rate (EDR) features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.1 packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links

- Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Beacon fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT\_DEV\_WAKE and BT\_HOST\_WAKE signaling (see [“Host Controller Power Management” on page 55](#))
- Channel-quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

**Major FM Radio features include:**

- 65 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- FM subsystem control using the Bluetooth HCI interface
- FM subsystem operates from reference clock inputs.
- Improved audio interface capabilities with full-featured bidirectional PCM and stereo analog output.

**FM Receiver-Specific Features Include:**

- Excellent FM radio performance with 1  $\mu$ V sensitivity for 26 dB (S+N)/N
- Signal-dependent stereo/mono blending
- Signal dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RSSI and IF frequency status indicators
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump

---

## Bluetooth Radio

The BCM43438 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

## Transmit

The BCM43438 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path has signal filters, an I/Q upconverter, an output power amplifier, and RF filters. The transmitter path also incorporates  $\pi/4$ -DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth Class 1 or Class 2 operation.

## Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK,  $\pi/4$ -DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

## Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

## Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near-thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

## Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the BCM43438 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

## Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

## Receiver Signal Strength Indicator

The radio portion of the BCM43438 provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

## Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM43438 uses an internal RF and IF loop filter.

## Calibration

The BCM43438 radio transceiver features an automated calibration scheme that is self contained in the radio. No user interaction is required during normal operation or during manufacturing to optimize performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including filter gain and phase characteristics, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

## Section 8: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase the reliability and security of data before sending and receiving it over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewatering in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

### Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

- Dual-mode classic Bluetooth and classic Low Energy (BT and BLE) operation.
- Low energy physical layer
- Low energy link layer
- Enhancements to HCI for low energy
- Low energy direct test mode
- 128 AES-CCM secure connection for both BT and BLE



**Note:** The BCM43438 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

## Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer contains the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth link controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - BLE Adv
  - BLE Scan/Initiation

## Test Mode Support

The BCM43438 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM43438 also supports enhanced testing features to simplify RF debugging and qualification as well as type-approval testing. These features include:

- Fixed frequency carrier-wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to an I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - Eight-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

## Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by the BCM43438 are:

- [RF Power Management](#)
- [Host Controller Power Management](#)
- [BBC Power Management](#)
- [FM Power Management](#)

## RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

## Host Controller Power Management

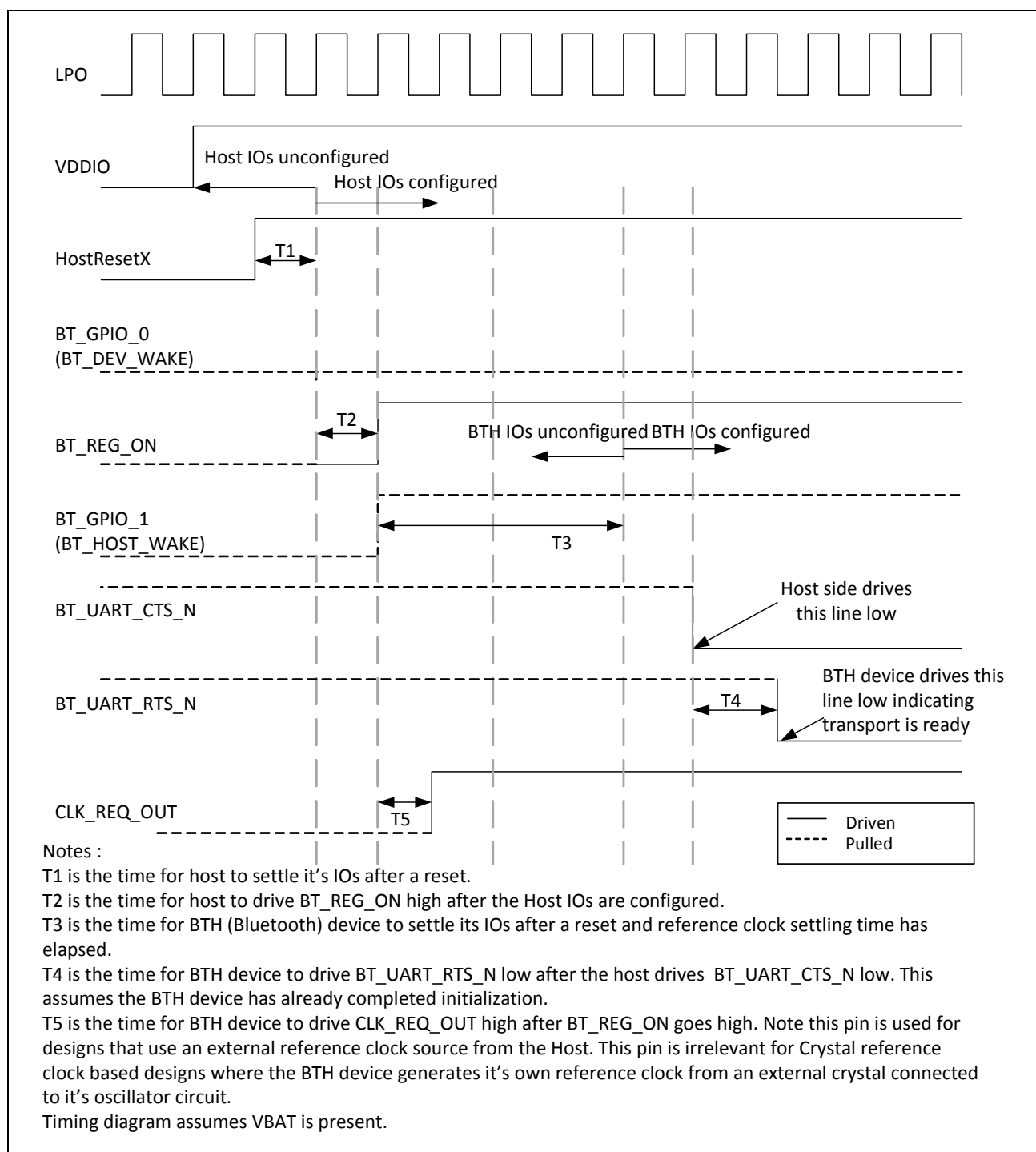
When running in UART mode, the BCM43438 can be configured so that dedicated signals are used for power management handshaking between the BCM43438 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

[Table 7](#) describes the power-control handshake signals used with the UART interface.

**Table 7: Power Control Pin Description**

<b>Signal</b>	<b>Type</b>	<b>Description</b>
BT_DEV_WAKE	I	Bluetooth device wake-up signal: Signal from the host to the BCM43438 indicating that the host requires attention. <ul style="list-style-type: none"> <li>• Asserted: The Bluetooth device must wake up or remain awake.</li> <li>• Deasserted: The Bluetooth device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	O	Host wake-up signal. Signal from the BCM43438 to the host indicating that the BCM43438 requires attention. <ul style="list-style-type: none"> <li>• Asserted: Host device must wake up or remain awake.</li> <li>• Deasserted: Host device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.
CLK_REQ	O	The BCM43438 asserts CLK_REQ when Bluetooth, NFC, or WLAN directs the host to turn on the reference clock. The CLK_REQ polarity is active-high. Add an external 100 k $\Omega$ pull-down resistor to ensure the signal is deasserted when the BCM43438 powers up or resets when VDDIO is present.

**Note:** Pad function Control Register is set to 0 for these pins.

**Figure 19: Startup Signaling Sequence**



## BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff and hold. While in these modes, the BCM43438 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the BCM43438 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the BCM43438 to effectively be off while keeping the I/O pins powered, so they do not draw extra current from any other I/O-connected devices.

During the low-power shut-down state, provided VDDIO remains applied to the BCM43438, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on digital signals in the system and enables the BCM43438 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two BCM43438 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF\_TCXO\_IN) and the 32.768 kHz input (LPO). When the BCM43438 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

## FM Power Management

The BCM43438 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems. The FM block does not have a low power state, it is either on or off.

## Wideband Speech

The BCM43438 provides support for wideband speech (WBS) technology. The BCM43438 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

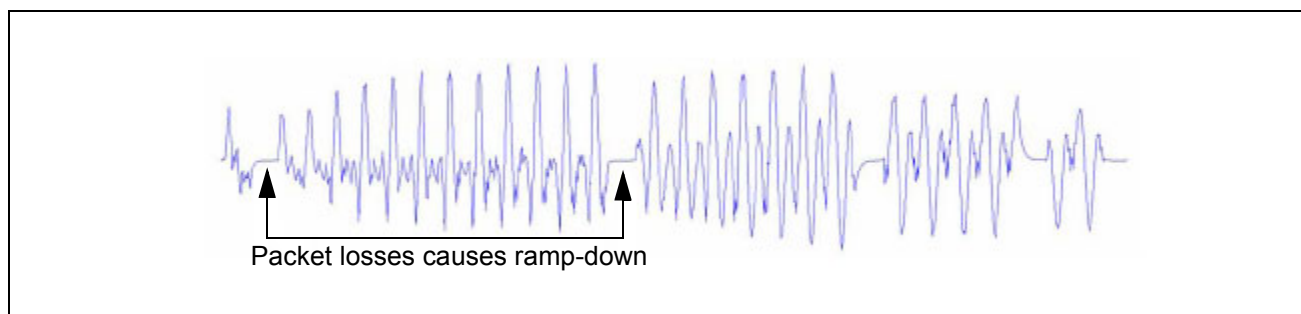
## Packet Loss Concealment

Packet Loss Concealment (PLC) improves the apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

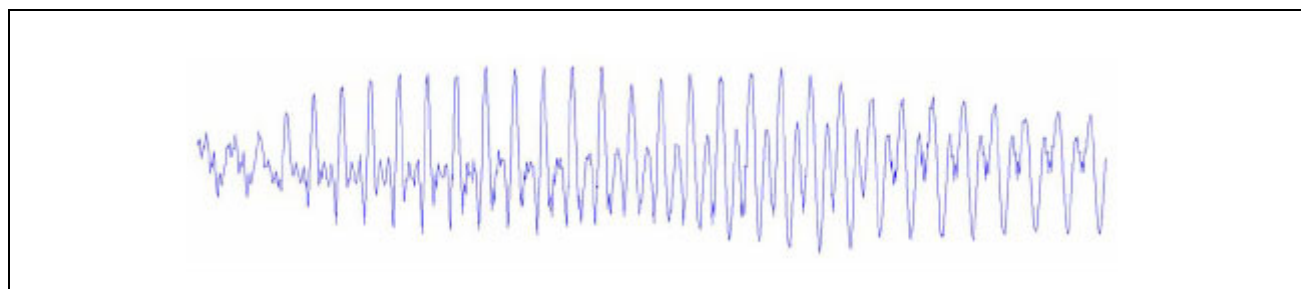
- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The BCM43438 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. [Figure 20](#) and [Figure 21](#) show audio waveforms with and without Packet Loss Concealment. Broadcom PLC/BEC algorithms also support wideband speech.

**Figure 20: CVSD Decoder Output Waveform Without PLC**



**Figure 21: CVSD Decoder Output Waveform After Applying PLC**



## Codec Encoding

The BCM43438 can support SBC and mSBC encoding and decoding for wideband speech.

## Multiple Simultaneous A2DP Audio Streams

The BCM43438 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

## FM Over Bluetooth

FM Over Bluetooth enables the BCM43438 to stream data from FM over Bluetooth without requiring the host to be awake. This can significantly extend battery life for usage cases where someone is listening to FM radio on a Bluetooth headset.

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## Adaptive Frequency Hopping

The BCM43438 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

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## Advanced Bluetooth/WLAN Coexistence

The BCM43438 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The BCM43438 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM43438 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM43438 also supports Transmit Power Control (TPC) on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core's channel information.

---

## Fast Connection (Interlaced Page and Inquiry Scans)

The BCM43438 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

## Section 9: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 576 KB of ROM for program storage and boot ROM, and 160 KB of RAM for data scratch-pad and patch RAM code. The internal ROM allows for flexibility during power-on reset (POR) to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or feature additions. These patches may be downloaded from the host to the BCM43438 through the UART transports.

---

### RAM, ROM, and Patch Memory

The BCM43438 Bluetooth core has 160 KB of internal RAM which is mapped between general purpose scratch-pad memory and patch memory, and 576 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory is used for bug fixes and feature additions to ROM memory code.

---

### Reset

The BCM43438 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT POR circuit is out of reset after BT\_REG\_ON goes high. If BT\_REG\_ON is low, then the POR circuit is held in reset.

# Section 10: Bluetooth Peripheral Transport Unit

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## PCM Interface

The BCM43438 supports two independent PCM interfaces. The PCM interface on the BCM43438 can connect to linear PCM codec devices in master or slave mode. In master mode, the BCM43438 generates the PCM\_CLK and PCM\_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43438. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

## Slot Mapping

The BCM43438 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rates is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

## Frame Synchronization

The BCM43438 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

## Data Formatting

The BCM43438 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM43438 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0's, 1's, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

## Wideband Speech Support

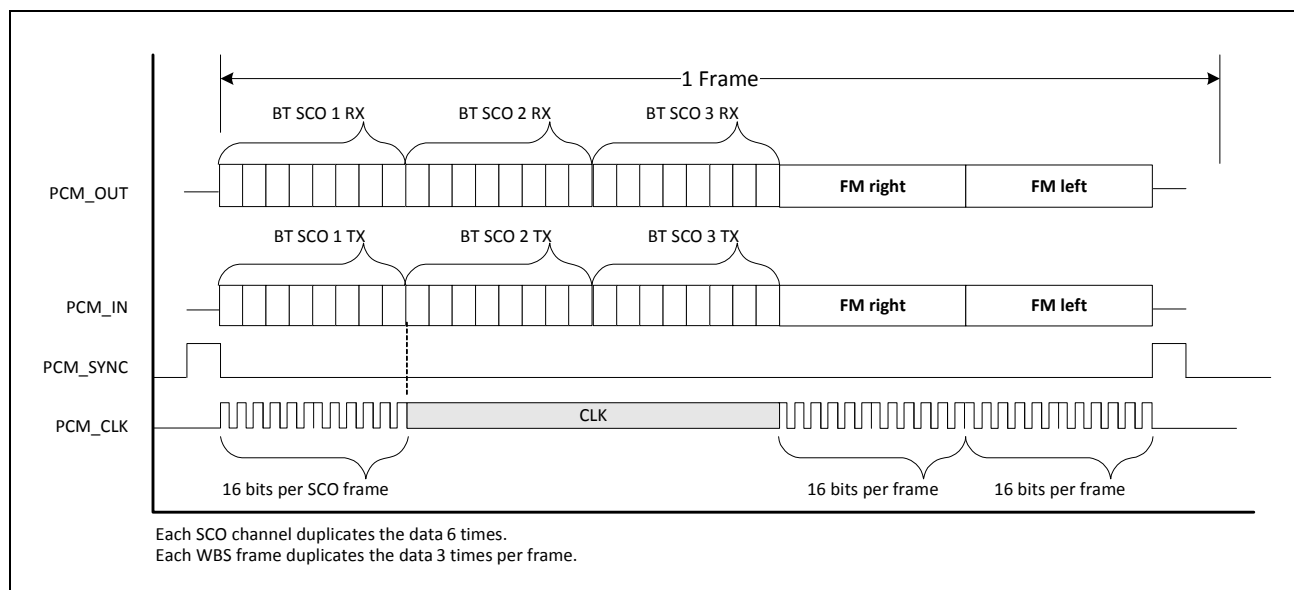
When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate. The BCM43438 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

## Multiplexed Bluetooth and FM over PCM

In this mode of operation, the BCM43438 multiplexes both FM and Bluetooth audio PCM channels over the same interface, reducing the number of required I/Os. This mode of operation is initiated through an HCI command from the host. The data stream format contains three channels: a Bluetooth channel followed by two FM channels (audio left and right). In this mode of operation, the bus data rate only supports 48 kHz operation per channel with 16 bits sent for each channel. To accomplish this, the Bluetooth data is repeated six times for 8 kHz data and three times for 16 kHz data. An initial sync pulse on the PCM\_SYNC line is used to indicate the beginning of the frame.

To support multiple Bluetooth audio streams within the Bluetooth channel, both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. [Figure 22](#) shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

**Figure 22: Functional Multiplex Data Diagram**



## PCM Interface Timing

### Short Frame Sync, Master Mode

Figure 23: PCM Timing Diagram (Short Frame Sync, Master Mode)

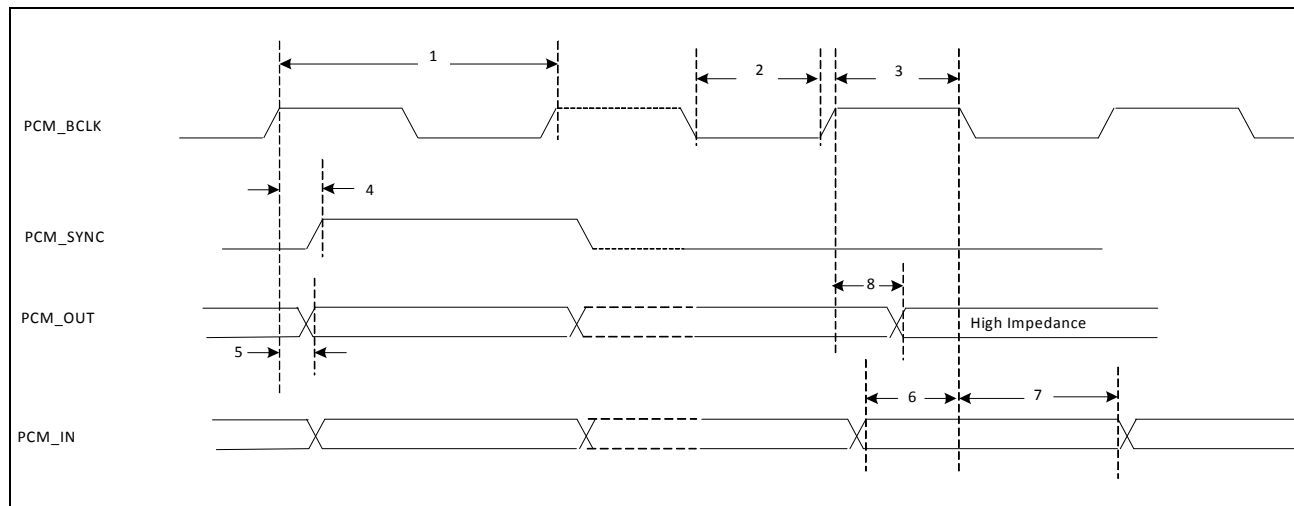


Table 8: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	PCM_SYNC delay	0	—	25	ns
5	PCM_OUT delay	0	—	25	ns
6	PCM_IN setup	8	—	—	ns
7	PCM_IN hold	8	—	—	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	—	25	ns

## Short Frame Sync, Slave Mode

Figure 24: PCM Timing Diagram (Short Frame Sync, Slave Mode)

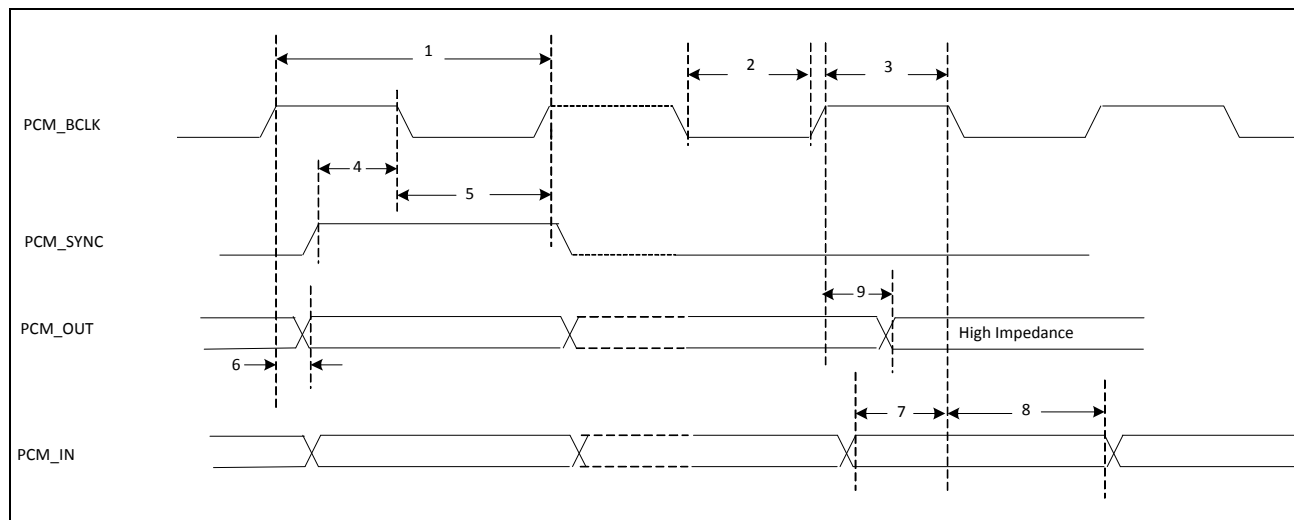


Table 9: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	PCM_SYNC setup	8	—	—	ns
5	PCM_SYNC hold	8	—	—	ns
6	PCM_OUT delay	0	—	25	ns
7	PCM_IN setup	8	—	—	ns
8	PCM_IN hold	8	—	—	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	—	25	ns



## Long Frame Sync, Master Mode

Figure 25: PCM Timing Diagram (Long Frame Sync, Master Mode)

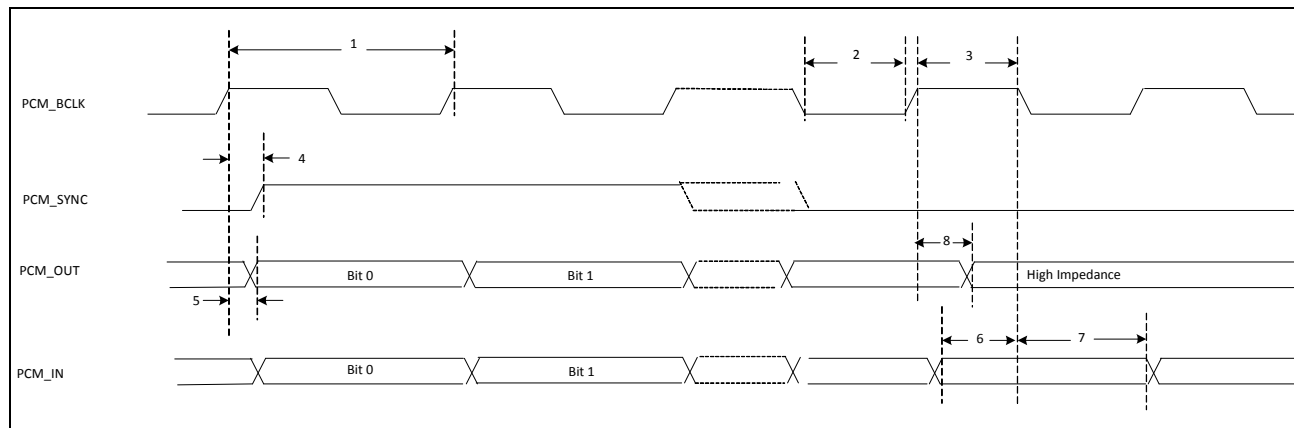
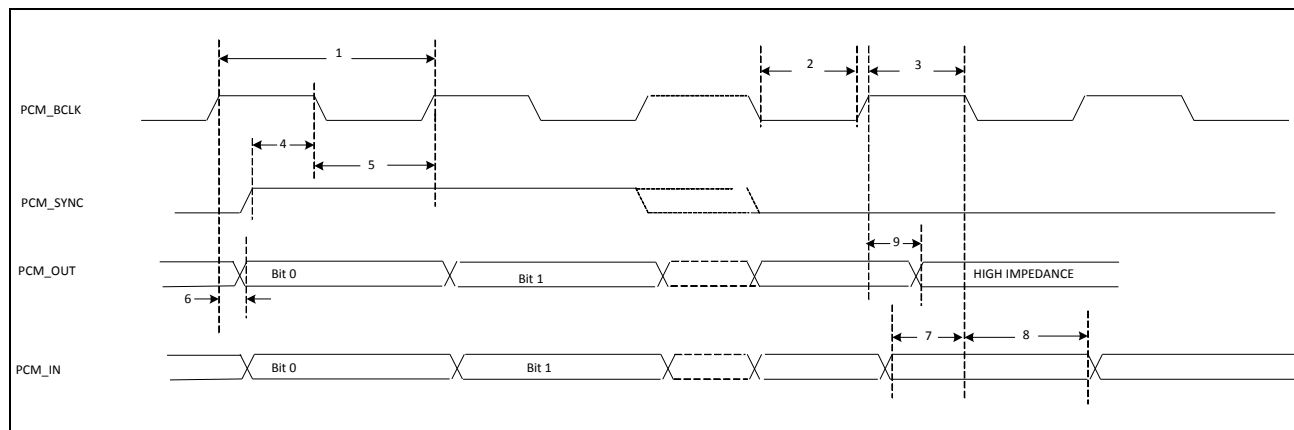


Table 10: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	PCM_SYNC delay	0	—	25	ns
5	PCM_OUT delay	0	—	25	ns
6	PCM_IN setup	8	—	—	ns
7	PCM_IN hold	8	—	—	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	—	25	ns

## Long Frame Sync, Slave Mode

**Figure 26: PCM Timing Diagram (Long Frame Sync, Slave Mode)**



**Table 11: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)**

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	PCM_SYNC setup	8	—	—	ns
5	PCM_SYNC hold	8	—	—	ns
6	PCM_OUT delay	0	—	25	ns
7	PCM_IN setup	8	—	—	ns
8	PCM_IN hold	8	—	—	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	—	25	ns

## UART Interface

The BCM43438 shares a single UART for Bluetooth and FM. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the Advanced High Performance Bus (AHB) interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport as described in the Bluetooth specification (*Three-wire UART Transport Layer*). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The BCM43438 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform a wake-on activity function. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM43438 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$  (see [Table 12](#)).

**Table 12: Example of Common Baud Rates**

<b>Desired Rate</b>	<b>Actual Rate</b>	<b>Error (%)</b>
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART timing is defined in [Figure 27](#) and [Figure 13](#).

Figure 27: UART Timing

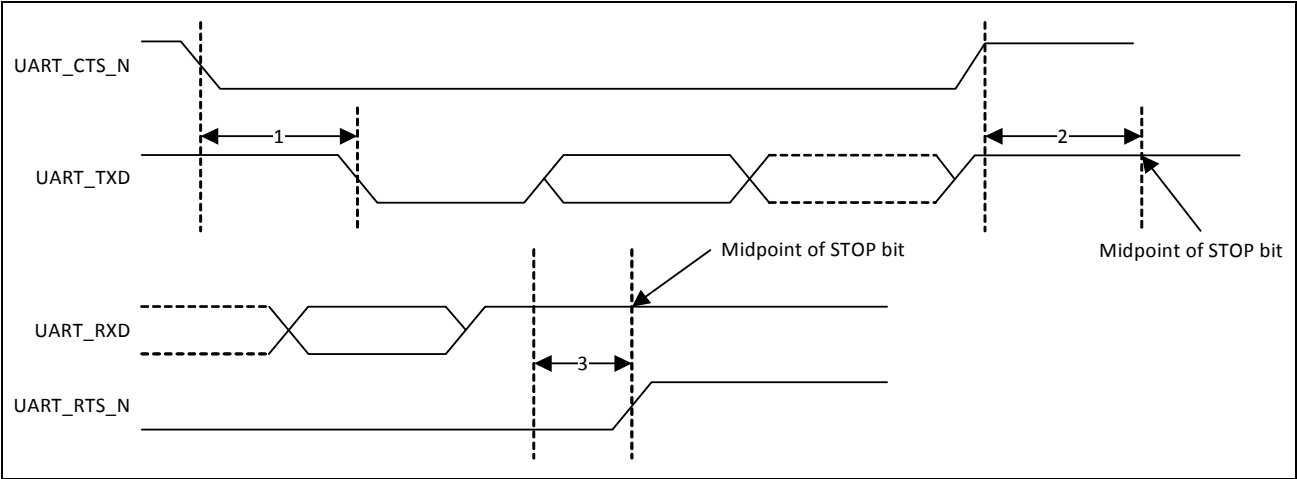


Table 13: UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

## Section 11: FM Receiver Subsystem

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### FM Radio

The BCM43438 includes a completely integrated FM radio receiver with RDS/RBDS covering all FM bands from 65 MHz to 108 MHz. The receiver is controlled through commands on the HCI. FM received audio is available as a stereo analog output or in digital form through PCM. The FM radio operates from the external clock reference.

---

### Digital FM Audio Interfaces

The FM audio can be transmitted via the PCM pins, and the sampling rate is programmable. The BCM43438 supports a three-wire PCM interface in either a master or slave configuration. The master or slave configuration is selected using vendor specific commands over the HCI interface. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks. In master mode, the clock rate is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

In slave mode, clock rates up to 3.072 MHz are supported.

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### Analog FM Audio Interfaces

The demodulated FM audio signal is available as line-level analog stereo output, generated by twin internal high SNR audio DACs.

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### FM Over Bluetooth

The BCM43438 can output received FM audio onto Bluetooth using one of following three links: eSCO, WBS, or A2DP. For all link types, after a link has been established, the host processor can enter sleep mode while the BCM43438 streams FM audio to the remote Bluetooth device, thus minimizing system current consumption.

---

### eSCO

In this use case, the stereo FM audio is downsampled to 8 kHz and a mono or stereo stream is sent through the Bluetooth eSCO link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

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## Wideband Speech Link

In this case, the stereo FM audio is downsampled to 16 kHz and a mono or stereo stream is sent through the Bluetooth wideband speech link to a remote Bluetooth device, typically a headset. Two Bluetooth voice connections must be used to transport stereo.

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## A2DP

In this case, the stereo FM audio is encoded by the on-chip SBC encoder and transported as an A2DP link to a remote Bluetooth device. Sampling rates of 48 kHz, 44.1 kHz, and 32 kHz joint stereo are supported. An A2DP lite stack is implemented in the BCM43438 to support this use case, which eliminates the need to route the SBC-encoded audio back to the host to create the A2DP packets.

---

## Autotune and Search Algorithms

The BCM43438 supports a number of FM search and tune functions, allowing the host to implement many convenient user functions by accessing the Broadcom FM stack.

- **Tune to Play**—Allows the FM receiver to be programmed to a specific frequency.
- **Search for SNR > Threshold**—Checks the power level of the available channel and the estimated SNR of the channel to help achieve precise control of the expected sound quality for the selected FM channel. Specifically, the host can adjust its SNR requirements to retrieve a signal with a specific sound quality, or adjust this to return the weakest channels.
- **Alternate Frequency Jump**—Allows the FM receiver to automatically jump to an alternate FM channel that carries the same information, but has a better SNR. For example, when traveling, a user may pass through a region where a number of channels carry the same station. When the user passes from one area to the next, the FM receiver can automatically switch to another channel with a stronger signal to spare the user from having to manually change the channel to continue listening to the same station.

## Audio Features

A number of features are implemented in the BCM43438 to provide the best possible audio experience for the user.

- Mono/Stereo Blend or Switch—The BCM43438 provides automatic control of the stereo or mono settings based on the FM signal carrier-to-noise ratio (C/N). This feature is used to maintain the best possible audio SNR based on the FM channel condition. Two modes of operation are supported:
  - Blend: In this mode, fine control of stereo separation is used to achieve optimal audio quality over a wide range of input C/N. The amount of separation is fully programmable. In Figure 28, the separation is programmed to maintain a minimum 50 dB SNR across the blend range.
  - Switch: In this mode, the audio switches from full stereo to full mono at a predetermined level to maintain optimal audio quality. The stereo-to-mono switch point and the mono-to-stereo switch points are fully programmable to provide the desired amount of audio SNR. In Figure 29, the switch point is programmed to switch to mono to maintain a 40 dB SNR.

**Figure 28: Blending and Switching Usage**

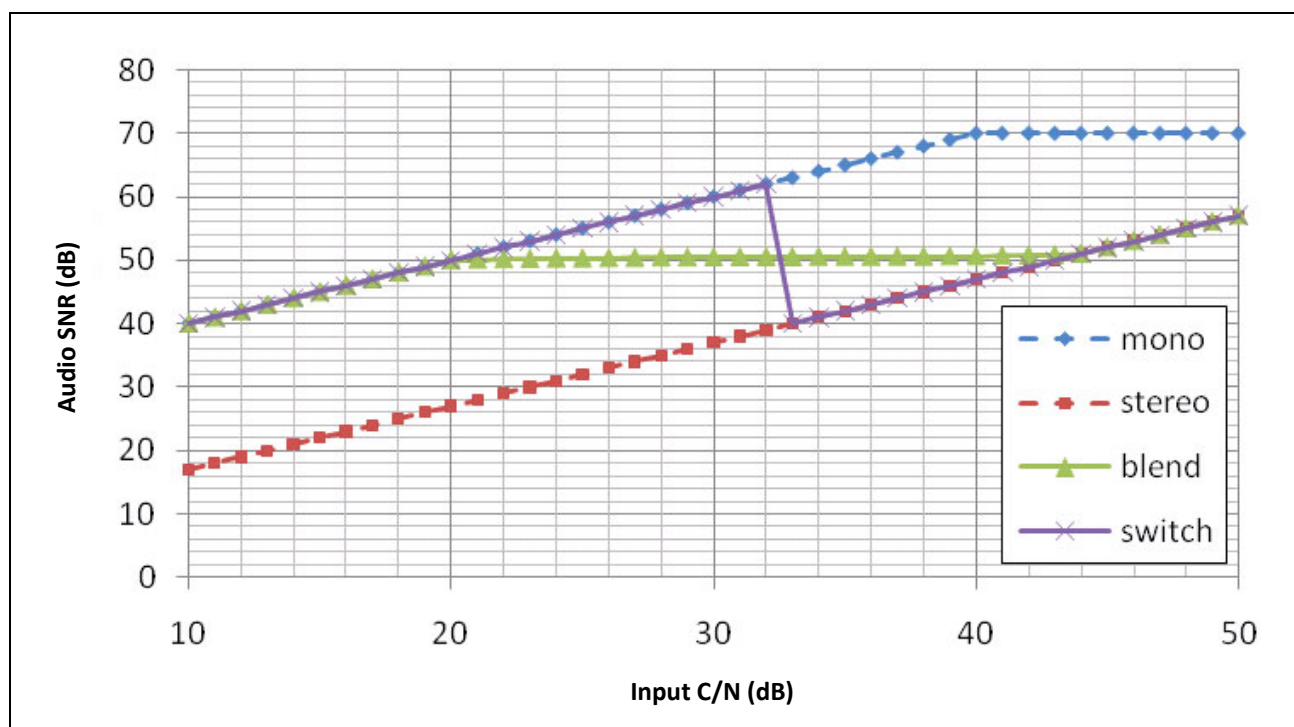
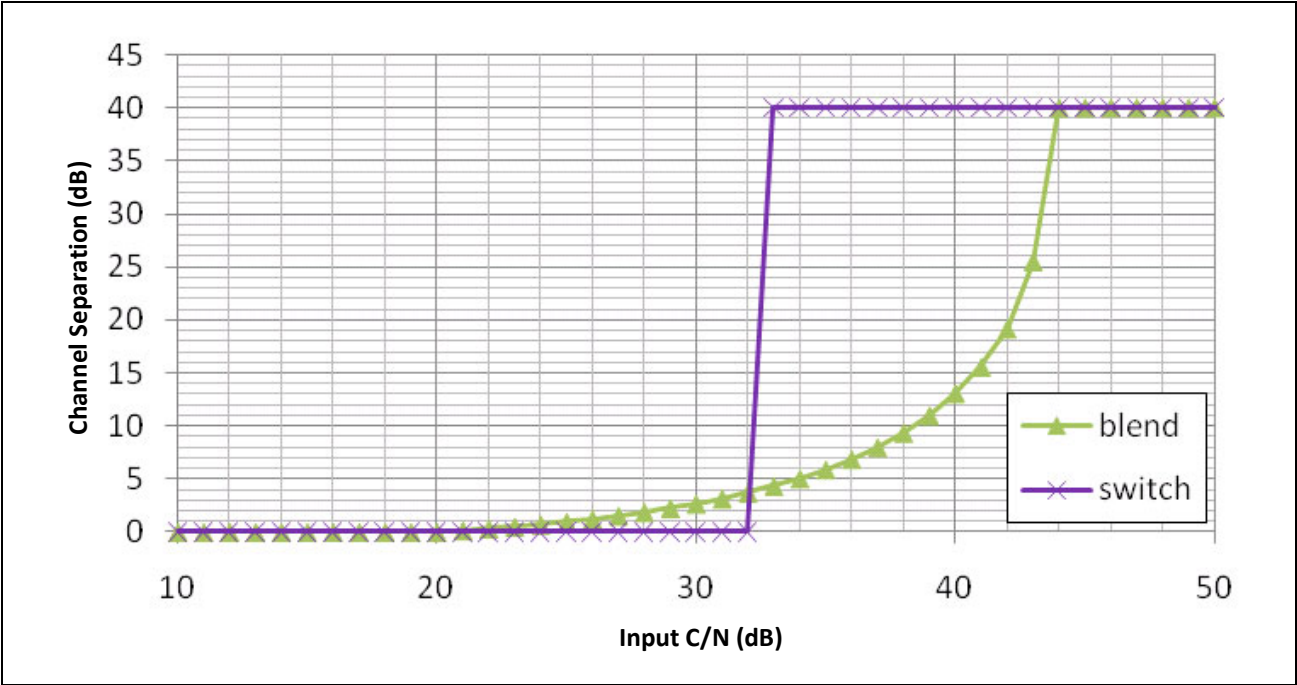
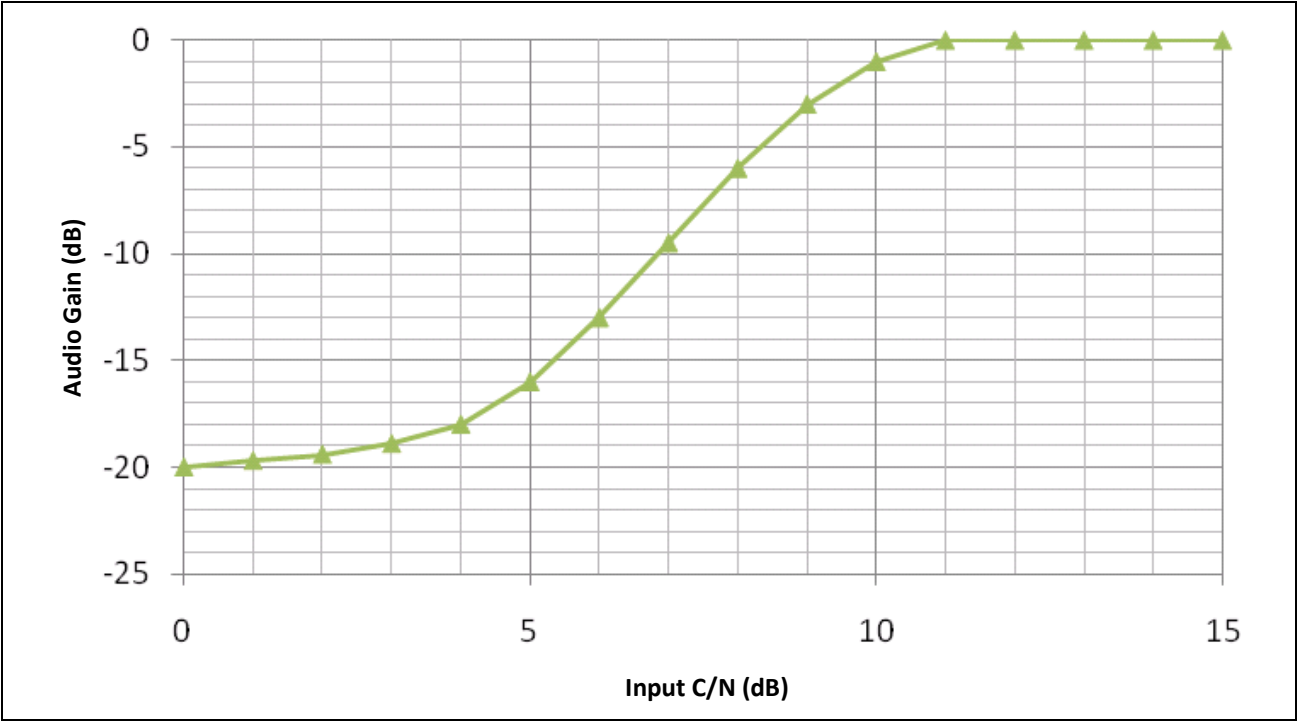


Figure 29: Blending and Switching Separation



- Soft Mute—Improves the user experience by dynamically muting the output audio proportionate to the FM signal C/N. This prevents a blast of static to the user. The mute characteristic is fully programmable to accommodate fine tuning of the output signal level. An example mute characteristic is shown in [Figure 30](#).

Figure 30: Soft Muting Characteristic





- **High Cut**—A programmable high-cut filter is provided to reduce the amount of high-frequency noise caused by static in the output audio signal. Like the soft mute circuit, it is fully programmable to provide any amount of high cut based on the FM signal C/N.
- **Audio Pause Detect**—The FM receiver monitors the magnitude of the audio signal and notifies the host through an interrupt when the magnitude of the signal has fallen below the threshold set for a programmable period. This feature can be used to provide alternate frequency jumps during periods of silence to minimize disturbances to the listener. Filtering techniques are used within the audio pause detection block to provide more robust presence-to-silence detection and silence-to-presence detection.
- **Automatic Antenna Tuning**—The BCM43438 has an on-chip automatic antenna tuning network. When used with a single off-chip inductor, the on-chip circuitry automatically chooses an optimal on-chip matching component to obtain the highest signal strength for the desired frequency. The high-Q nature of this matching network simultaneously provides out-of-band blocking protection as well as a reduction of radiated spurious emissions from the FM antenna. It is designed to accommodate a wide range of external wire antennas.

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## RDS/RBDS

The BCM43438 integrates a RDS/RBDS modem, the decoder includes programmable filtering and buffering functions. The RDS/RBDS data can be read out through the HCI interface.

In addition, the RDS/RBDS receive functionality supports the following:

- Block decoding, error correction, and synchronization
- A flywheel synchronization feature, allowing the host to set parameters for acquisition, maintenance, and loss of sync. (It is possible to set up the BCM43438 such that synchronization is achieved when a minimum of two good blocks (error free) are decoded in sequence. The number of good blocks required for sync is programmable.)
- Storage capability up to 126 blocks of RDS data
- Full or partial block-B match detection with host interruption
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection with host interruption
- Automatic frequency jumping
- Block-E filtering
- Soft muting
- Signal dependent mono/stereo blending

## Section 12: CPU and Global Functions

### WLAN CPU and Memory Subsystem

The BCM43438 includes an integrated ARM Cortex-M3 processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM architecture v7-M with support for the Thumb-2 instruction set. ARM Cortex-M3 provides a 30% performance gain over ARM7TDMI.

At 0.19  $\mu\text{W}/\text{MHz}$ , the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/ $\mu\text{W}$ . It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for code and data access (Icode/Dcode and system buses). ARM Cortex-M3 supports extensive debug features including real-time tracing of program execution.

On-chip memory for the CPU includes 512 KB SRAM and 640 KB ROM.

### One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 1024-bit One-Time Programmable (OTP) memory, which is read by system software after a device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address, can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP memory programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package. Documentation on the OTP development process is available on the Broadcom customer support portal (<http://www.broadcom.com/support>).

## GPIO Interface

Five general purpose I/O (GPIO) pins are available on the BCM43438 that can be used to connect to various external devices.

GPIOs are tristated by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors.

GPIO\_0 is normally used as a WL\_HOST\_WAKE signal.

The BCM43438 supports a 2-wire coexistence configuration using GPIO\_1 and GPIO\_2.

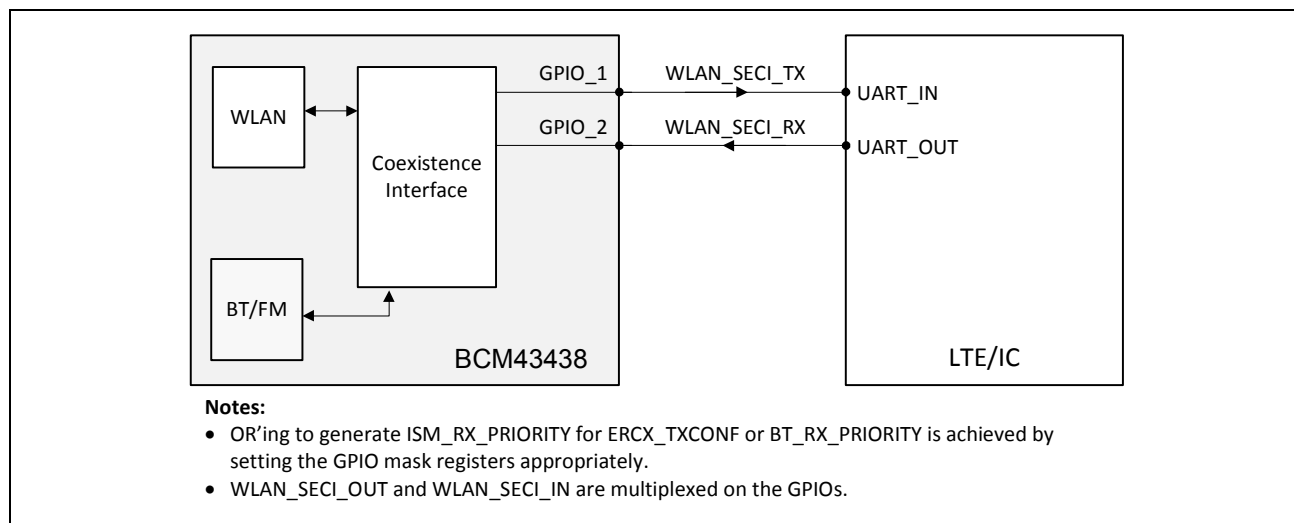
## External Coexistence Interface

The BCM43438 supports a 2-wire coexistence interface to enable signaling between the device and an external colocated wireless device in order to manage wireless medium sharing for optimal performance. The external colocated device can be any of the following ICs: GPS, WiMAX, LTE, or UWB. An LTE IC is used in this section for illustration.

Figure 31 shows a 2-wire LTE coexistence example. The following definitions apply to the GPIOs in the figure:

- GPIO\_1: WLAN\_SECI\_TX output to an LTE IC.
- GPIO\_2: WLAN\_SECI\_RX input from an LTE IC.

**Figure 31: 2-Wire Coexistence Interface to an LTE IC**



See Figure 27 on page 68 and Table 13: "UART Timing Specifications," on page 68 for UART timing.

## JTAG Interface

The BCM43438 supports the IEEE 1149.1 JTAG boundary scan standard over SDIO for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

## UART Interface

One UART interface can be enabled by software as an alternate function on the JTAG pins. UART\_RX is available on the JTAG\_TDI pin, and UART\_TX is available on the JTAG\_TDO pin.

The UART is primarily for debugging during development. By adding an external RS-232 transceiver, this UART enables the BCM43438 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of  $64 \times 8$  in each direction.

## Section 13: WLAN Software Architecture

### Host Software Architecture

The host driver (DHD) provides a transparent connection between the host operating system and the BCM43438 media (for example, WLAN) by presenting a network driver interface to the host operating system and communicating with the BCM43438 over an interface-specific bus (SPI, SDIO, and so on) to:

- Forward transmit and receive frames between the host network stack and the BCM43438 device.
- Pass control requests from the host to the BCM43438 device, returning the BCM43438 device responses.

The driver communicates with the BCM43438 over the bus using a control channel and a data channel to pass control messages and data messages. The actual message format is based on the BDC protocol.

### Device Software Architecture

The wireless device, protocol, and bus drivers are run on the embedded ARM processor using a Broadcom-defined operating system called HND RTE, which transfers data over a propriety Broadcom format over the SDIO/SPI interface between the host and device (BDC/LMAC). The data portion of the format consists of IEEE 802.11 frames wrapped in a Broadcom encapsulation. The host architecture provides all missing functionality between a network device and the Broadcom device interface. The host can also be customized to provide functionality between the Broadcom device interface and a full network device interface.

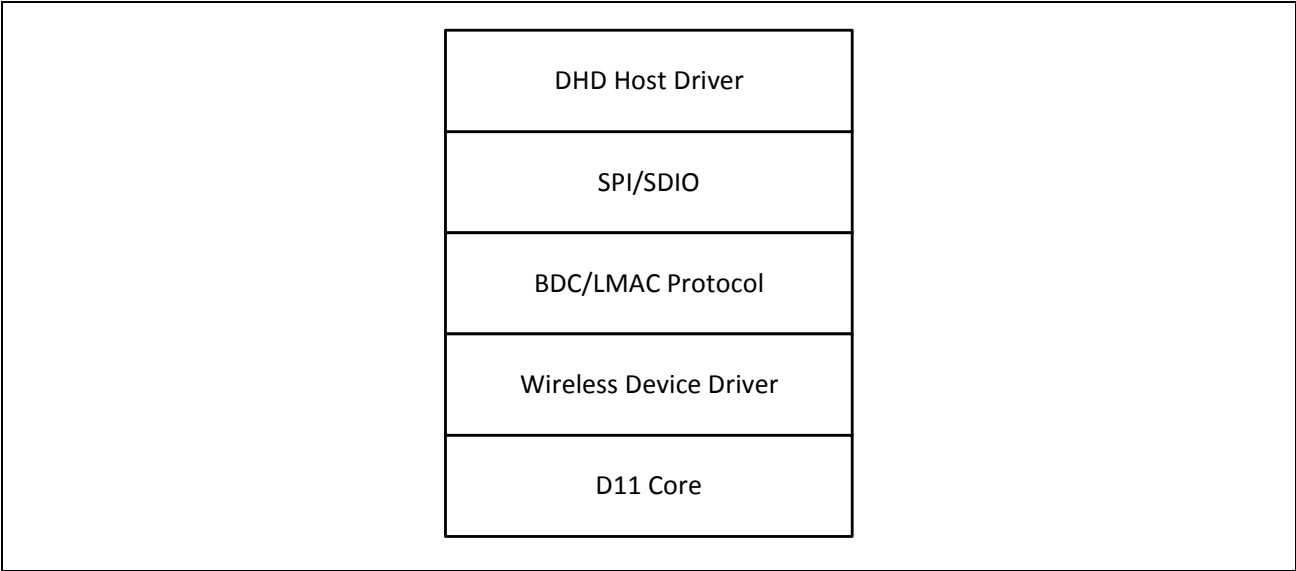
This transfer requires a message-oriented (framed) interconnect between the host and device. The SDIO bus is an addressed bus—each host-initiated bus operation contains an explicit device target address—and does not natively support a higher-level data frame concept. Broadcom has implemented a hardware/software message encapsulation scheme that ignores the bus operation code address and prefixes each frame with a 4-byte length tag for framing. The device presents a packet-level interface over which data, control, and asynchronous event (from the device) packets are supported.

The data and control packets received from the bus are initially processed by the bus driver and then passed on to the protocol driver. If the packets are data packets, they are transferred to the wireless device driver (and out through its medium), and a data packet received from the device medium follows the same path in the reverse direction. If the packets are control packets, the protocol header is decoded by the protocol driver. If the packets are wireless IOCTL packets, the IOCTL API of the wireless driver is called to configure the wireless device. The microcode running in the D11 core processes all time-critical tasks.

## Remote Downloader

When the BCM43438 powers up, the DHD initializes and downloads the firmware to run in the device.

**Figure 32: WLAN Software Architecture**



## Wireless Configuration Utility

The device driver that supports the Broadcom IEEE 802.11 family of wireless solutions provides an input/output control (IOCTL) interface for making advanced configuration settings. The IOCTL interface makes it possible to make settings that are normally not possible when using just the native operating system-specific IEEE 802.11 configuration mechanisms. The utility uses IOCTLs to query or set a number of different driver/chip operating properties.

## Section 14: Pinout and Signal Descriptions

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### Ball Map

[Figure 33 on page 80](#) shows the 63-ball WLPGA ball map.

Figure 33: 63-Ball WLBGA Ball Map (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	
1	BT_UART_RXD	BT_DEV_WAKE	BT_HOST_WAKE		FM_RF_IN	BT_VCO_VDD	BT_IF_VDD	BT_PAVDD	WLRF_2G_eLG	WLRF_2G_RF		WLRF_PA_VDD	1
2	BT_UART_TXD	BT_UART_CTS_N	FM_OUT1	FM_OUT2	FM_RF_VDD	BTFM_PLL_VDD	BTFM_PLL_VSS	BT_IF_VSS	WLRF_LNA_GND	WLRF_GENERAL_GND	WLRF_PA_GND	WLRF_VDD_1P35	2
3			BT_UART_RTS_N	VDDC	FM_RF_VSS			BT_VCO_VSS	WLRF_GPIO		WLRF_VCO_GND	WLRF_XTAL_VD1P2	3
4		BT_PCM_OUT	BT_PCM_IN	VSSC			VDDC	WLRF_AFE_GND			WLRF_XTAL_GND	WLRF_XTAL_XOP	4
5	BT_PCM_CLK	BT_PCM_SYNC				LPO_IN			VSSC		GPIO_2	WLRF_XTAL_XON	5
6	SR_VLX	PMU_AVSS	VOUT_CLDO	VOUT_LNLD0	BT_REG_ON	WCC_VDDIO	WL_REG_ON	GPIO_1	GPIO_0	SDIO_DATA_0	SDIO_CMD	CLK_REQ	6
7	SR_PVSS	SR_VDDBAT5V	LDO_VDD1P5		VOUT_3P3	LDO_VDDBAT5V		SDIO_DATA_1	SDIO_DATA_3		SDIO_DATA_2	SDIO_CLK	7
	A	B	C	D	E	F	G	H	J	K	L	M	

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## WLBGA Ball List in Ball Number Order with X-Y Coordinates

Table 14 provides ball numbers and names in ball number order and includes the X and Y coordinates.

**Table 14: BCM43438 WLBGA Ball List — Ordered By Ball Number**

<b>Ball Number</b>	<b>Ball Name</b>	<b>X Coordinate</b>	<b>Y Coordinate</b>
A1	BT_UART_RXD	5111.08	222.2
A2	BT_UART_TXD	5111.08	666.66
A5	BT_PCM_CLK	5111.08	1999.98
A6	SR_VLX	5111.06	2444.42
A7	SR_PVSS	5111.06	2888.86
B1	BT_DEV_WAKE	4666.64	222.2
B2	BT_UART_CTS_N	4666.64	666.66
B4	BT_PCM_OUT	4666.64	1555.54
B5	BT_PCM_SYNC	4666.64	1999.98
B6	PMU_AVSS	4666.62	2444.42
B7	SR_VBAT5V	4666.62	2888.86
C1	BT_HOST_WAKE	4222.19	222.2
C2	FM_OUT1	4222.18	666.66
C3	BT_UART_RTS_N	4222.19	1111.1
C4	BT_PCM_IN	4222.19	1555.54
C6	VOUT_CLDO	4222.18	2444.42
C7	LDO_VDD1P5	4222.18	2888.86
D2	FM_OUT2	3777.74	666.66
D3	VDDC	3777.75	1111.1
D4	VSSC	3777.75	1555.54
D6	VOUT_LNLDO	3777.74	2444.42
E1	FM_RF_IN	3333.3	222.22
E2	FM_RF_VDD	3333.3	666.66
E3	FM_RF_VSS	3333.3	1111.1
E6	BT_REG_ON	3333.3	2444.42
E7	VOUT_3P3	3333.3	2888.86
F1	BT_VCO_VDD	2888.86	222.22
F2	BTFM_PLL_VDD	2888.86	666.66
F5	LPO_IN	2888.86	1999.98
F6	WCC_VDDIO	2888.86	2444.43
F7	LDO_VDDBAT5V	2888.86	2888.86
G1	BT_IF_VDD	2444.42	222.22
G2	BTFM_PLL_VSS	2444.42	666.66

**Table 14: BCM43438 WLBGA Ball List — Ordered By Ball Number**

<b>Ball Number</b>	<b>Ball Name</b>	<b>X Coordinate</b>	<b>Y Coordinate</b>
G4	VDDC	2444.42	1555.54
G6	WL_REG_ON	2444.42	2444.43
H1	BT_PAVDD	1999.98	222.22
H2	BT_IF_VSS	1999.98	666.66
H3	BT_VCO_VSS	1999.98	1111.1
H4	WLRF_AFE_GND	1999.98	1555.54
H6	GPIO_1	1999.98	2444.43
H7	SDIO_DATA_1	1999.98	2888.88
J1	WLRF_2G_eLG	1555.54	222.22
J2	WLRF_LNA_GND	1555.54	666.66
J3	WLRF_GPIO	1555.54	1111.1
J5	VSSC	1555.53	1999.98
J6	GPIO_0	1555.53	2444.43
J7	SDIO_DATA_3	1555.53	2888.88
K1	WLRF_2G_RF	1111.1	222.22
K2	WLRF_GENERAL_GND	1111.1	666.66
K6	SDIO_DATA_0	1111.09	2444.43
L2	WLRF_PA_GND	666.66	666.66
L3	WLRF_VCO_GND	666.66	1111.1
L4	WLRF_XTAL_GND	666.66	1555.54
L5	GPIO_2	666.65	1999.98
L6	SDIO_CMD	666.65	2444.43
L7	SDIO_DATA_2	666.65	2888.88
M1	WLRF_PA_VDD	222.22	222.22
M2	WLRF_VDD_1P35	222.22	666.66
M3	WLRF_XTAL_VDD1P2	222.22	1111.1
M4	WLRF_XTAL_XOP	222.22	1555.54
M5	WLRF_XTAL_XON	222.22	1999.98
M6	CLK_REQ	222.2	2444.43
M7	SDIO_CLK	222.2	2888.88

## WLBGA Ball List Ordered By Ball Name

Table 15 provides the ball numbers and names in ball name order.

**Table 15: BCM43438 WLBGA Ball List — Ordered By Ball Name**

<b>Ball Name</b>	<b>Ball Number</b>	<b>Ball Name</b>	<b>Ball Number</b>
BT_DEV_WAKE	B1	SDIO_CMD	L6
BT_HOST_WAKE	C1	SDIO_DATA_0	K6
BT_IF_VDD	G1	SDIO_DATA_1	H7
BT_IF_VSS	H2	SDIO_DATA_2	L7
BT_PAVDD	H1	SDIO_DATA_3	J7
BT_PCM_CLK	A5	SR_PVSS	A7
BT_PCM_IN	C4	SR_VDDBAT5V	B7
BT_PCM_OUT	B4	SR_VLX	A6
BT_PCM_SYNC	B5	VDDC	D3
BT_REG_ON	E6	VDDC	G4
BT_UART_CTS_N	B2	VOUT_3P3	E7
BT_UART_RTS_N	C3	VOUT_CLDO	C6
BT_UART_RXD	A1	VOUT_LNLDO	D6
BT_UART_TXD	A2	VSSC	D4
BT_VCO_VDD	F1	VSSC	J5
BT_VCO_VSS	H3	WCC_VDDIO	F6
BTFM_PLL_VDD	F2	WL_REG_ON	G6
BTFM_PLL_VSS	G2	WLRF_2G_eLG	J1
CLK_REQ	M6	WLRF_2G_RF	K1
FM_OUT1	C2	WLRF_AFE_GND	H4
FM_OUT2	D2	WLRF_GENERAL_GND	K2
FM_RF_IN	E1	WLRF_GPIO	J3
FM_RF_VDD	E2	WLRF_LNA_GND	J2
FM_RF_VSS	E3	WLRF_PA_GND	L2
GPIO_0	J6	WLRF_PA_VDD	M1
GPIO_1	H6	WLRF_VCO_GND	L3
GPIO_2	L5	WLRF_VDD_1P35	M2
LDO_VDD1P5	C7	WLRF_XTAL_GND	L4
LDO_VDDBAT5V	F7	WLRF_XTAL_VDD1P2	M3
LPO_IN	F5	WLRF_XTAL_XON	M5
PMU_AVSS	B6	WLRF_XTAL_XOP	M4
SDIO_CLK	M7		

## Signal Descriptions

Table 16 provides the WLPGA package signal descriptions.

**Table 16: WLPGA Signal Descriptions**

<b>Signal Name</b>	<b>WLPGA Ball</b>	<b>Type</b>	<b>Description</b>
<b>RF Signal Interface</b>			
WLRF_2G_RF	K1	O	2.4 GHz BT and WLAN RF output port
<b>SDIO Bus Interface</b>			
SDIO_CLK	M7	I	SDIO clock input
SDIO_CMD	L6	I/O	SDIO command line
SDIO_DATA_0	K6	I/O	SDIO data line 0
SDIO_DATA_1	H7	I/O	SDIO data line 1.
SDIO_DATA_2	L7	I/O	SDIO data line 2. Also used as a strapping option (see Table 19 on page 90).
SDIO_DATA_3	J7	I/O	SDIO data line 3
<b>Note:</b> Per Section 6 of the SDIO specification, 10 to 100 kΩ pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.			
<b>WLAN GPIO Interface</b>			
WLRF_GPIO	J3	I/O	Test pin. Not connected in normal operation.
<b>Clocks</b>			
WLRF_XTAL_XON	M5	O	XTAL oscillator output
WLRF_XTAL_XOP	M4	I	XTAL oscillator input
CLK_REQ	M6	O	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
LPO_IN	F5	I	External sleep clock input (32.768 kHz). If an external 32.768 kHz clock cannot be provided, pull this pin low. However, BLE will be always on and cannot go to deep sleep.
<b>FM Receiver</b>			
FM_OUT1	C2	O	FM analog output 1
FM_OUT2	D2	O	FM analog output 2
FM_RF_IN	E1	I	FM radio antenna port
FM_RF_VDD	E2	I	FM power supply

**Table 16: WLBGA Signal Descriptions (Cont.)**

<b>Signal Name</b>	<b>WLBGA Ball</b>	<b>Type</b>	<b>Description</b>
<b>Bluetooth PCM</b>			
BT_PCM_CLK	A5	I/O	PCM clock; can be master (output) or slave (input)
BT_PCM_IN	C4	I	PCM data input sensing
BT_PCM_OUT	B4	O	PCM data output
BT_PCM_SYNC	B5	I/O	PCM sync; can be master (output) or slave (input)
<b>Bluetooth UART and Wake</b>			
BT_UART_CTS_N	B2	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
BT_UART_RTS_N	C3	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
BT_UART_RXD	A1	I	UART serial input. Serial data input for the HCI UART interface.
BT_UART_TXD	A2	O	UART serial output. Serial data output for the HCI UART interface.
BT_DEV_WAKE	B1	I/O	DEV_WAKE or general-purpose I/O signal
BT_HOST_WAKE	C1	I/O	HOST_WAKE or general-purpose I/O signal

**Note:** By default, the Bluetooth BT WAKE signals provide GPIO/WAKE functionality, and the UART pins provide UART functionality. Through software configuration, the PCM interface can also be routed over the BT\_WAKE/UART signals as follows:

- PCM\_CLK on the UART\_RTS\_N pin
- PCM\_OUT on the UART\_CTS\_N pin
- PCM\_SYNC on the BT\_HOST\_WAKE pin
- PCM\_IN on the BT\_DEV\_WAKE pin

In this case, the BT HCI transport included sleep signaling will operate using UART\_RXD and UART\_TXD; that is, using a 3-Wire UART Transport.

**Table 16: WLBGA Signal Descriptions (Cont.)**

<b>Signal Name</b>	<b>WLBGA Ball</b>	<b>Type</b>	<b>Description</b>
<b>Miscellaneous</b>			
WL_REG_ON	G6	I	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	E6	I	Used by PMU to power up or power down the internal regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming.
GPIO_0	J6	I/O	Programmable GPIO pins. This pin becomes an output pin when it is used as WLAN_HOST_WAKE/out-of-band signal.
GPIO_1	H6	I/O	Programmable GPIO pins
GPIO_2	L5	I/O	Programmable GPIO pins
WLRFB_2G_eLG	J1	I	Connect to an external inductor. See the reference schematic for details.
<b>Integrated Voltage Regulators</b>			
SR_VDDBAT5V	B7	I	SR VBAT input power supply
SR_VLX	A6	O	CBUCK switching regulator output. See <a href="#">Table 33 on page 115</a> for details of the inductor and capacitor required on this output.
LDO_VDDBAT5V	F7	I	LDO VBAT
LDO_VDD1P5	C7	I	LNLDO input
VOUT_LNLDO	D6	O	Output of low-noise LNLDO
VOUT_CLDO	C6	O	Output of core LDO
<b>Bluetooth Power Supplies</b>			
BT_PAVDD	H1	I	Bluetooth PA power supply
BT_IF_VDD	G1	I	Bluetooth IF block power supply
BTFM_PLL_VDD	F2	I	Bluetooth RF PLL power supply
BT_VCO_VDD	F1	I	Bluetooth RF power supply

**Table 16: WLBGA Signal Descriptions (Cont.)**

<b>Signal Name</b>	<b>WLBGA Ball</b>	<b>Type</b>	<b>Description</b>
<b>Power Supplies</b>			
WLRF_XTAL_VDD1P2	M3	I	XTAL oscillator supply
WLRF_PA_VDD	M1	I	Power amplifier supply
WCC_VDDIO	F6	O	1.8V–3.3V VDDIO supply for WLAN and BT.
WLRF_VDD_1P35	M2	I	LNLDO input supply
VDDC	D3, G4	I	Core supply for WLAN and BT.
VOUT_3P3	E7	O	3.3V output supply. See the reference schematic for details.
<b>Ground</b>			
BT_IF_VSS	H2	I	1.2V Bluetooth IF block ground
BTFM_PLL_VSS	G2	I	Bluetooth/FM RF PLL ground
BT_VCO_VSS	H3	I	1.2V Bluetooth RF ground
FM_RF_VSS	E3	I	FM RF ground
PMU_AVSS	B6	I	Quiet ground
SR_PVSS	A7	I	Switcher-power ground
VSSC	D4, J5	I	Core ground for WLAN and BT
WLRF_AFE_GND	H4	I	AFE ground
WLRF_LNA_GND	J2	I	2.4 GHz internal LNA ground
WLRF_GENERAL_GND	K2	I	Miscellaneous RF ground
WLRF_PA_GND	L2	I	2.4 GHz PA ground
WLRF_VCO_GND	L3	I	VCO/LO generator ground
WLRF_XTAL_GND	L4	I	XTAL ground

## WLAN GPIO Signals and Strapping Options

The pins listed in [Table 17](#) are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to ground using a 10 k $\Omega$  resistor or less.



**Note:** Refer to the reference board schematics for more information.

**Table 17: GPIO Functions and Strapping Options**

<b>Pin Name</b>	<b>WLPGA Pin #</b>	<b>Default</b>	<b>Function</b>	<b>Description</b>
SDIO_DATA_2	L7	1	WLAN host interface select	This pin selects the WLAN host interface mode. The default is SDIO. For gSPI, pull this pin low.



## Chip Debug Options

The chip can be accessed for debugging via the JTAG interface, multiplexed on the SDIO\_DATA\_0 through SDIO\_DATA\_3 (and SDIO\_CLK) I/O or the Bluetooth PCM I/O depending on the bootstrap state of GPIO\_1 and GPIO\_2.

Table 18 shows the debug options of the device.

**Table 18: Chip Debug Options**

<b>JTAG_SEL</b>	<b>GPIO_2</b>	<b>GPIO_1</b>	<b>Function</b>	<b>SDIO I/O Pad Function</b>	<b>BT PCM I/O Pad Function</b>
0	0	0	Normal mode	SDIO	BT PCM
0	0	1	JTAG over SDIO	JTAG	BT PCM
0	1	0	JTAG over BT PCM	SDIO	JTAG
0	1	1	SWD over GPIO_1/ GPIO_2	SDIO	BT PCM

## I/O States

The following notations are used in Table 19 on page 90:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 19: I/O States

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present	Power Rail
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200k)	Input; PD (of 200k)	–	–
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200k)	Input; PD (of 200k)	–	–
CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high.	PD	Open drain. Active high.	Open drain. Active high.	–	BT_VDDO
BT_HOST_WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	I/O; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_DEV_WAKE	I/O	Y	I/O; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_UART_CTS	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_RTS	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input; PU	–	BT_VDDO
SDIO_DATA_0	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_DATA_1	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PD	SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_DATA_2	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> PD	SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_DATA_3	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_CMD	I/O	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	–	WL_VDDIO
SDIO_CLK	I	N	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	SDIO MODE -> NoPull	–	WL_VDDIO
BT_PCM_CLK	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_IN	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_OUT	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input; NoPull (Note 4)	Input; NoPull (Note 4)	High-Z, NoPull	Input, PD	Input, PD	–	BT_VDDO
JTAG_SEL	I	Y	PD	PD	PD	PD	PD	PD	WL_VDDIO
GPIO_0	I/O	Y	PD	PD	NoPull	PD	PD	PD	WL_VDDIO
GPIO_1	I/O	Y	NoPull	NoPull	NoPull	NoPull	NoPull	NoPull	WL_VDDIO

Table 19: I/O States (Cont.)

Name	I/O	Keeper	Active Mode	Low Power State/ Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON=1; WL_REG_ON=1)	(WL_REG_ON=1 and BT_REG_ON=0) and VDDIOs Are Present	(WL_REG_ON=0 and BT_REG_ON=1) and VDDIOs Are Present	Power Rail
GPIO_2	I/O	Y	PU	PU	NoPull	PU	PU	PU	WL_VDDIO

**Note:**

1. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the Power-down state.
2. If there is no keeper, and it is an input and there is Nopull, then the pad should be driven to prevent leakage due to a floating pad (e.g., SDIO\_CLK).
3. In the Power-down state (xx\_REG\_ON = 0): High-Z; NoPull => The pad is disabled because power is not supplied.
4. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
5. GPIO\_0 through GPIO\_2 can be configured to operate as inputs or outputs in Deep-Sleep mode before entering the mode.
6. The GPIO pull states for the Active and Low-Power states are hardware defaults. They can all be subsequently programmed as pull-ups or pull-downs.
7. Regarding GPIO pins, the following are the pull-up and pull-down values for both 3.3V and 1.8V VDDIO:

	Minimum (kΩ)	Typical (kΩ)	Maximum (kΩ)
3.3V VDDIO pull-downs:	51.5	44.5	38
3.3V VDDIO pull-ups:	37.4	39.5	44.5
1.8V VDDIO pull-downs:	64	83	116
1.8V VDDIO pull-ups:	65	86	118

## Section 15: DC Characteristics



**Note:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

### Absolute Maximum Ratings



**Caution!** The absolute maximum ratings in [Table 20](#) indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Excluding VBAT, operation at the absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 20: Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	VBAT	−0.5 to +6.0 <sup>a</sup>	V
DC supply voltage for digital I/O	VDDIO	−0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	−0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	—	−0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	−0.5 to 1.32	V
DC supply voltage for core	VDDC	−0.5 to 1.32	V
Maximum undershoot voltage for I/O <sup>b</sup>	V <sub>undershoot</sub>	−0.5	V
Maximum overshoot voltage for I/O <sup>b</sup>	V <sub>overshoot</sub>	VDDIO + 0.5	V
Maximum junction temperature	T <sub>j</sub>	125	°C

a. Continuous operation at 6.0V is supported.

b. Duration not to exceed 25% of the duty cycle.

## Environmental Ratings

The environmental ratings are shown in [Table 21](#).

**Table 21: Environmental Ratings**

Characteristic	Value	Units	Conditions/Comments
Ambient temperature ( $T_A$ )	–30 to +70°C <sup>a</sup>	°C	Operation
Storage temperature	–40 to +125°C	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

- a. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for –10°C to 55°C.

## Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

**Table 22: ESD Specifications**

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human Body Model Contact Discharge per JEDEC EID/ JESD22-A114	1250	V
Machine Model (MM)	ESD_HAND_MM	Machine Model Contact	50	V
CDM	ESD_HAND_CDM	Charged Device Model Contact Discharge per JEDEC EIA/ JESD22-C101	175	V

## Recommended Operating Conditions and DC Characteristics

Functional operation is not guaranteed outside the limits shown in [Table 23](#), and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

**Table 23: Recommended Operating Conditions and DC Characteristics**

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0 <sup>a</sup>	–	4.8 <sup>b</sup>	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
<b>SDIO Interface I/O Pins</b>					
For VDDIO_SD = 1.8V:					
Input high voltage	VIH	1.27	–	–	V
Input low voltage	VIL	–	–	0.58	V
Output high voltage @ 2 mA	VOH	1.40	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO_SD = 3.3V:					
Input high voltage	VIH	$0.625 \times \text{VDDIO}$	–	–	V
Input low voltage	VIL	–	–	$0.25 \times \text{VDDIO}$	V
Output high voltage @ 2 mA	VOH	$0.75 \times \text{VDDIO}$	–	–	V
Output low voltage @ 2 mA	VOL	–	–	$0.125 \times \text{VDDIO}$	V
<b>Other Digital I/O Pins</b>					
For VDDIO = 1.8V:					
Input high voltage	VIH	$0.65 \times \text{VDDIO}$	–	–	V
Input low voltage	VIL	–	–	$0.35 \times \text{VDDIO}$	V
Output high voltage @ 2 mA	VOH	$\text{VDDIO} - 0.45$	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	$\text{VDDIO} - 0.4$	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V

**Table 23: Recommended Operating Conditions and DC Characteristics (Cont.)**

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
RF Switch Control Output Pins <sup>c</sup>					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C <sub>IN</sub>	–	–	5	pF

- The BCM43438 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 4.8V.
- The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration over the lifetime of the device are allowed.
- Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

## Section 16: WLAN RF Specifications

The BCM43438 includes an integrated direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.



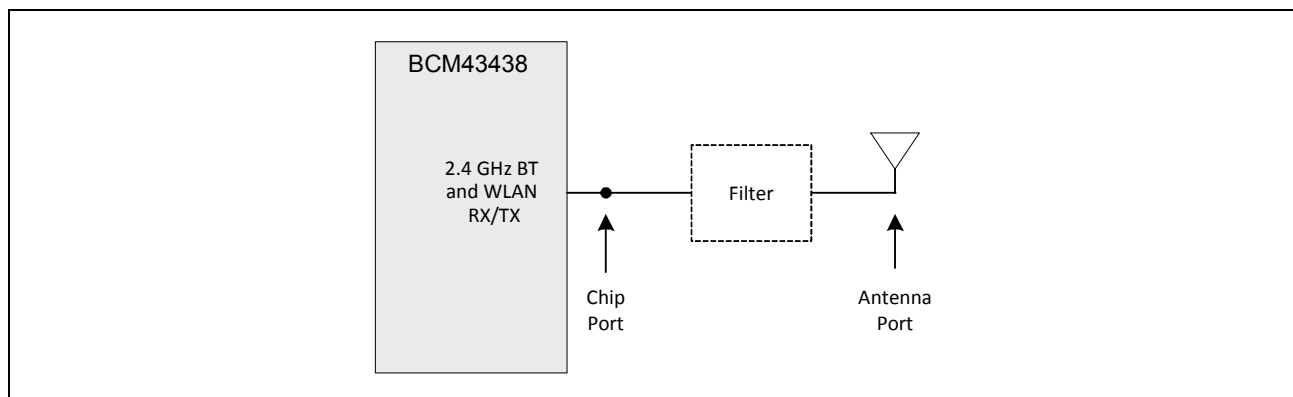
**Note:** Values in this data sheet are design goals and may change based on device characterization results.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in [Table 21: “Environmental Ratings,” on page 93](#) and [Table 23: “Recommended Operating Conditions and DC Characteristics,” on page 94](#). Functional operation outside these limits is not guaranteed.

Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

**Figure 34: RF Port Location**



**Note:** All specifications apply at the antenna port unless otherwise specified.



## 2.4 GHz Band General RF Specifications

**Table 24: 2.4 GHz Band General RF Specifications**

<i>Item</i>	<i>Condition</i>	<i>Minimum</i>	<i>Typical</i>	<i>Maximum</i>	<i>Unit</i>
TX/RX switch time	Including TX ramp down	–	–	5	μs
RX/TX switch time	Including TX ramp up	–	–	2	μs

## WLAN 2.4 GHz Receiver Performance Specifications



**Note:** The specifications in [Table 25](#) apply at the antenna port. An RF path loss of 2.5 dB is assumed between the chip output and the antenna port.

**Table 25: WLAN 2.4 GHz Receiver Performance Specifications**

<i>Parameter</i>	<i>Condition/Notes</i>	<i>Minimum</i>	<i>Typical</i>	<i>Maximum</i>	<i>Unit</i>
Frequency range	–	2400	–	2500	MHz
Operating temperature	–	–30	25	85	°C
RX sensitivity (8% PER for 1024 octet PSDU) at WLAN RF port	1 Mbps DSSS	–95	–97	–	dBm
	2 Mbps DSSS	–91	–93	–	dBm
	5.5 Mbps DSSS	–89	–91	–	dBm
	11 Mbps DSSS	–86	–88	–	dBm
RX sensitivity (10% PER for 1000 octet PSDU) at WLAN RF port	6 Mbps OFDM	–89	–91	–	dBm
	9 Mbps OFDM	–88	–90	–	dBm
	12 Mbps OFDM	–85	–87	–	dBm
	18 Mbps OFDM	–83	–85	–	dBm
	24 Mbps OFDM	–80	–82	–	dBm
	36 Mbps OFDM	–78	–80	–	dBm
	48 Mbps OFDM	–74	–76	–	dBm
	54 Mbps OFDM	–73	–75	–	dBm

**Table 25: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)**

<b>Parameter</b>	<b>Condition/Notes</b>		<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
RX sensitivity (10% PER for 4096 octet PSDU) at WLAN RF port. Defined for default parameters: GF, 800 ns GI.	20 MHz channel spacing for all MCS rates					
	256-QAM, R = 5/6		-65	-67	—	dBm
	256-QAM, R = 3/4		-67	-69	—	dBm
	MCS7		-69	-71	—	dBm
	MCS6		-71	-73	—	dBm
	MCS5		-72	-74	—	dBm
	MCS4		-77	-79	—	dBm
	MCS3		-80	-82	—	dBm
	MCS2		-82	-84	—	dBm
	MCS1		-84	-86	—	dBm
	MCS0		-88	-90	—	dBm
Blocking level @ WLAN RF port for 1dB RX sensitivity degradation (without external filtering). <sup>a</sup>	698–716 MHz	WCDMA, LTE	-28	—	—	dBm
	776–787 MHz	WCDMA, LTE	-28	—	—	dBm
	824–849 MHz	GSM850	-19 <sup>b</sup>	—	—	dBm
	824–849 MHz	WCDMA, LTE	-28 <sup>c</sup>	—	—	dBm
	880–915 MHz	GSM900	-19	—	—	dBm
	880–915 MHz	WCDMA, LTE	-28	—	—	dBm
	1710–1785 MHz	GSM1800	-22	—	—	dBm
	1710–1785 MHz	WCDMA, LTE	-28	—	—	dBm
	1850–1910 MHz	GSM1900	-22	—	—	dBm
	1850–1910 MHz	WCDMA, LTE	-28	—	—	dBm
	1880–1920 MHz	TD-SCDMA	-33	—	—	dBm
	1900–1920 MHz	LTE	-28	—	—	dBm
	1910–1930 MHz	LTE	-28	—	—	dBm
	1920–1980 MHz	WCDMA, LTE	-28	—	—	dBm
	1930–1990 MHz	LTE	-32	—	—	dBm
	2010–2025 MHz	TD-SCDMA	-31	—	—	dBm
	2500–2570 MHz	WCDMA, LTE	-50	—	—	dBm
	2570–2620 MHz	LTE	-50	—	—	dBm
	3168–4752 MHz	UWB	-28	—	—	dBm
	3402–3620 MHz	WiMAX	-23	—	—	dBm
	6336–8976 MHz	UWB	-21	—	—	dBm
Maximum receive level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		-3.5	—	—	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		-9.5	—	—	dBm
	@ 6–54 Mbps (10% PER, 1000 octets)		-13	—	—	dBm
LPF 3-dB bandwidth	—	—	9	—	10	MHz

**Table 25: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)**

<b>Parameter</b>	<b>Condition/Notes</b>		<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Adjacent channel rejection- DSSS. (Difference between interfering and desired signal [25 MHz apart] at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes.)	11 Mbps DSSS	-70 dBm	35	—	—	dB
Adjacent channel rejection- OFDM. (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1000 <sup>d</sup> octet PSDU with desired signal level as specified in Condition/Notes.)	6 Mbps OFDM	-79 dBm	16	—	—	dB
	9 Mbps OFDM	-78 dBm	15	—	—	dB
	12 Mbps OFDM	-76 dBm	13	—	—	dB
	18 Mbps OFDM	-74 dBm	11	—	—	dB
	24 Mbps OFDM	-71 dBm	8	—	—	dB
	36 Mbps OFDM	-67 dBm	4	—	—	dB
	48 Mbps OFDM	-63 dBm	0	—	—	dB
	54 Mbps OFDM	-62 dBm	-1	—	—	dB
RCPI accuracy <sup>e</sup>	65 Mbps OFDM	-61 dBm	-2	—	—	dB
	Range -98 dBm to -75 dBm		-3	—	3	dB
	Range above -75 dBm		-5	—	5	dB
Return loss	Zo = 50Ω across the dynamic range.		10	—	—	dB

- The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
- Minimum value is -23 dB for channel 11.
- Minimum value is -36 dBm for channel 11.
- For 65 Mbps, the size is 4096.
- The minimum and maximum values shown have a 95% confidence level.

## WLAN 2.4 GHz Transmitter Performance Specifications



**Note:** The specifications in [Table 26](#) apply at the antenna port. An RF path loss of 2.5 dB is assumed between the chip output and the antenna port.

**Table 26: WLAN 2.4 GHz Transmitter Performance Specifications**

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	—		2400	—	2500	MHz
Transmitted power in cellular and FM bands at RF port (at 18.5 dBm, 90% duty cycle, 1 Mbps CCK). <sup>a</sup>	76–108 MHz	FM RX	—	–161	–159	dBm/Hz
	170–240 MHz	DAB	—	–161	–159	dBm/Hz
	470–862 MHz	DVB-H	—	–161	–159	dBm/Hz
	728–746 MHz	WCDMA, LTE	—	–161	–159	dBm/Hz
	746–757 MHz	WCDMA, LTE	—	–161	–159	dBm/Hz
	869–894 MHz	WCDMA, LTE	—	–161	–159	dBm/Hz
	925–960 MHz	GSM, WCDMA, LTE	—	–161	–159	dBm/Hz
	1570–1580 MHz	GPS	—	–155	–153	dBm/Hz
	1592–1610 MHz	GLONASS	—	–155	–153	dBm/Hz
	1805–1880 MHz	GSM, WCDMA, LTE	—	–155	–153	dBm/Hz
	1880–1920 MHz	TD-SCDMA	—	–134	–132	dBm/Hz
	1850–1910 MHz	WCDMA, LTE	—	–134	–132	dBm/Hz
	1910–1930 MHz	WCDMA, LTE	—	–134	–132	dBm/Hz
	1900–1920 MHz	WCDMA, LTE	—	–134	–132	dBm/Hz
	1930–1990 MHz	GSM, WCDMA, LTE	—	–134	–132	dBm/Hz
Harmonic level at RF port (at 18 dBm with 90% duty cycle, 1 Mbps CCK)	2010–2075 MHz	TD-SCDMA	—	–125.3	–123.3	dBm/Hz
	2110–2170 MHz	WCDMA, LTE	—	–125.3	–123.3	dBm/Hz
	4.8–5.0 GHz	2nd harmonic	—	–19.5	–12.8	dBm/MHz
	7.2–7.5 GHz	3rd harmonic	—	–37.7	–26.7	dBm/MHz

**Table 26: WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)**

<b>Parameter</b>	<b>Condition/Notes</b>		<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
TX power at RF port for highest power level setting at 25°C, VBAT = 3.6V, and spectral mask and EVM compliance <sup>b</sup>	<b>EVM Does Not Exceed</b>					
	IEEE 802.11b (DSSS/CCK)	–9 dB	18.5	–	–	dBm
	OFDM, BPSK	–8 dB	18	–	–	dBm
	OFDM, QPSK	–13 dB	18	–	–	dBm
	OFDM, 16-QAM	–19 dB	18	–	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	15.5	–	–	dBm
	OFDM, 64-QAM (R = 5/6)	–27 dB	15	–	–	dBm
	OFDM, 256-QAM (R = 5/6)	–32 dB	12.5	–	–	dBm
TX power control dynamic range	–		9	–	–	dB
Closed loop TX power variation at highest power level setting (at RF port)	Across full temperature and voltage range. Applies across 5 to 21 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Zo = 50		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	VSWR = 2:1.	EVM degradation	–	3.5	–	dB
		Output power variation	–	±2	–	dB
		ACPR-compliant power level	–	15	–	dBm
	VSWR = 3:1.	EVM degradation	–	4	–	dB
		Output power variation	–	±3	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. TX power for channel 1 and channel 11 is specified separately by nonvolatile memory parameters to ensure band-edge compliance.

## General Spurious Emissions Specifications

**Table 27: General Spurious Emissions Specifications**

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
TX emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–44	–41	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–68	–65	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm
RX/standby emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–54	–51	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–88	–85	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm

**Note:** The specifications in this table apply at the RF port.

## Section 17: Bluetooth RF Specifications

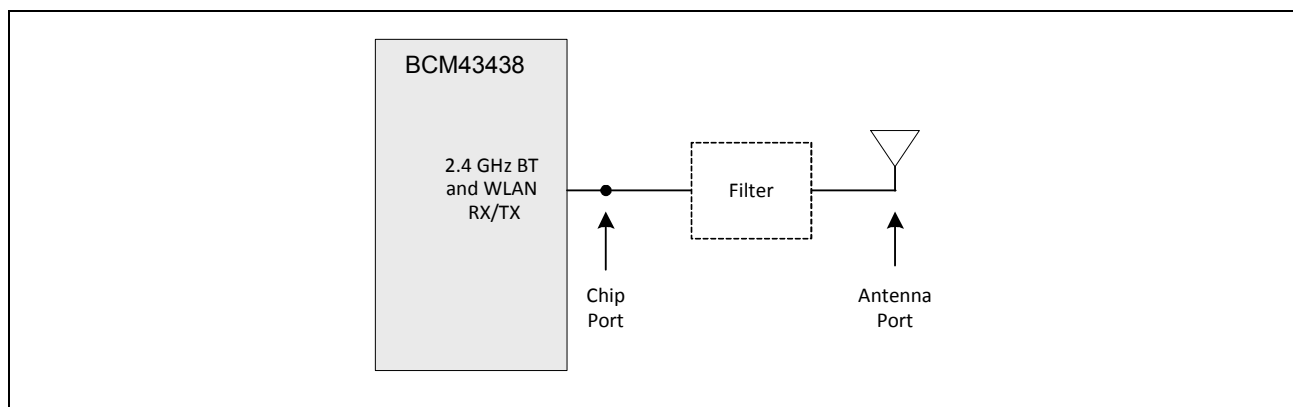


**Note:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 21: “Environmental Ratings,” on page 93](#) and [Table 23: “Recommended Operating Conditions and DC Characteristics,” on page 94](#). Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

**Figure 35: RF Port Location for Bluetooth Testing**



**Note:** All Bluetooth specifications apply at the chip port unless otherwise specified.

**Table 28: Bluetooth Receiver RF Specifications**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>Note:</b> The specifications in this table are measured at the chip output port unless otherwise specified.					
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	–	–92.5	–	dBm
	$\pi/4$ -DQPSK, 0.01% BER, 2 Mbps	–	–94.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–88.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at antenna	–	–	–	–20	dBm
<b>Interference Performance<sup>a</sup></b>					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I $\geq 3$ MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	–30	dB
C/I $\geq 3$ MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	–40	dB
C/I image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	–7	dB
C/I 1 MHz adjacent to image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–	–20	dB
C/I co-channel	8-DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25	dB
C/I $\geq 3$ MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0.0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13	dB
<b>Out-of-Band Blocking Performance (CW)</b>					
30–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm



**Table 28: Bluetooth Receiver RF Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>Out-of-Band Blocking Performance, Modulated Interferer (LTE)</b>					
<b>GFSK (1 Mbps)</b>					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
<b><math>\pi/4</math> DPSK (2 Mbps)</b>					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
<b>8DPSK (3 Mbps)</b>					
2310 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2330 MHz	LTE band40 TDD 20M BW	–	–19	–	dBm
2350 MHz	LTE band40 TDD 20M BW	–	–20	–	dBm
2370 MHz	LTE band40 TDD 20M BW	–	–24	–	dBm
2510 MHz	LTE band7 FDD 20M BW	–	–24	–	dBm
2530 MHz	LTE band7 FDD 20M BW	–	–21	–	dBm
2550 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
2570 MHz	LTE band7 FDD 20M BW	–	–20	–	dBm
<b>Out-of-Band Blocking Performance, Modulated Interferer (Non-LTE)</b>					
<b>GFSK (1 Mbps)<sup>a</sup></b>					
698–716 MHz	WCDMA	–	–12	–	dBm
776–849 MHz	WCDMA	–	–12	–	dBm
824–849 MHz	GSM850	–	–12	–	dBm
824–849 MHz	WCDMA	–	–11	–	dBm
880–915 MHz	E-GSM	–	–11	–	dBm
880–915 MHz	WCDMA	–	–16	–	dBm
1710–1785 MHz	GSM1800	–	–15	–	dBm
1710–1785 MHz	WCDMA	–	–18	–	dBm

**Table 28: Bluetooth Receiver RF Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
1850–1910 MHz	GSM1900	–	–20	–	dBm
1850–1910 MHz	WCDMA	–	–17	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18	–	dBm
1920–1980 MHz	WCDMA	–	–18	–	dBm
2010–2025 MHz	TD-SCDMA	–	–18	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
<b><math>\pi/4</math> DPSK (2 Mbps)<sup>a</sup></b>					
698–716 MHz	WCDMA	–	–8	–	dBm
776–794 MHz	WCDMA	–	–8	–	dBm
824–849 MHz	GSM850	–	–9	–	dBm
824–849 MHz	WCDMA	–	–9	–	dBm
880–915 MHz	E-GSM	–	–8	–	dBm
880–915 MHz	WCDMA	–	–8	–	dBm
1710–1785 MHz	GSM1800	–	–14	–	dBm
1710–1785 MHz	WCDMA	–	–14	–	dBm
1850–1910 MHz	GSM1900	–	–15	–	dBm
1850–1910 MHz	WCDMA	–	–14	–	dBm
1880–1920 MHz	TD-SCDMA	–	–16	–	dBm
1920–1980 MHz	WCDMA	–	–15	–	dBm
2010–2025 MHz	TD-SCDMA	–	–17	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
<b>8DPSK (3 Mbps)<sup>a</sup></b>					
698–716 MHz	WCDMA	–	–11	–	dBm
776–794 MHz	WCDMA	–	–11	–	dBm
824–849 MHz	GSM850	–	–11	–	dBm
824–849 MHz	WCDMA	–	–12	–	dBm
880–915 MHz	E-GSM	–	–11	–	dBm
880–915 MHz	WCDMA	–	–11	–	dBm
1710–1785 MHz	GSM1800	–	–16	–	dBm
1710–1785 MHz	WCDMA	–	–15	–	dBm
1850–1910 MHz	GSM1900	–	–17	–	dBm
1850–1910 MHz	WCDMA	–	–17	–	dBm
1880–1920 MHz	TD-SCDMA	–	–17	–	dBm
1920–1980 MHz	WCDMA	–	–17	–	dBm
2010–2025 MHz	TD-SCDMA	–	–18	–	dBm
2500–2570 MHz	WCDMA	–	–21	–	dBm
<b>RX LO Leakage</b>					
2.4 GHz band	–	–	–90.0	–80.0	dBm

**Table 28: Bluetooth Receiver RF Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>Spurious Emissions</b>					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
869–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

- a. The Bluetooth reference level for the required signal at the Bluetooth chip port is 3 dB higher than the typical sensitivity level.

**Table 29: Bluetooth Transmitter RF Specifications<sup>a</sup>**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	11.0	–	dBm
QPSK TX power at Bluetooth		–	8.0	–	dBm
8PSK TX power at Bluetooth		–	8.0	–	dBm
Power control step		2	4	8	dB
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz <  M – N  < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26.0	dBc
1.5 MHz <  M – N  < 2.5 MHz		–	–31	–20.0	dBm
M – N  ≥ 2.5 MHz <sup>b</sup>		–	–43	–40.0	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0 <sup>c,d</sup>	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 <sup>d,e,f</sup>	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm
Out-of-Band Noise Floor <sup>g</sup>					
65–108 MHz	FM RX	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–146	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–146	–	dBm/Hz
925–960 MHz	E-GSM	–	–146	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–144	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–143	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–137	–	dBm/Hz

- a. Unless otherwise specified, the specifications in this table apply at the chip output port, and output power specifications are with the temperature correction algorithm and TSSI enabled.
- b. Typically measured at an offset of ±3 MHz.
- c. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.
- d. The spurious emissions during Idle mode are the same as specified in [Table 29 on page 108](#).
- e. Specified at the Bluetooth antenna port.
- f. Meets this specification using a front-end band-pass filter.
- g. Transmitted power in cellular and FM bands at the Bluetooth antenna port. See [Figure 35 on page 103](#) for location of the port.

**Table 30: Local Oscillator Performance**

<b>Parameter</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>LO Performance</b>				
Lock time	–	72	–	μs
Initial carrier frequency tolerance	–	±25	±75	kHz
<b>Frequency Drift</b>				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 μs
<b>Frequency Deviation</b>				
00001111 sequence in payload <sup>a</sup>	140	155	175	kHz
10101010 sequence in payload <sup>b</sup>	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload.

b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

**Table 31: BLE RF Specifications**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Frequency range	–	2402		2480	MHz
RX sense <sup>a</sup>	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power <sup>b</sup>	–	–	8.5	–	dBm
Mod Char: delta f1 average	–	225	255	275	kHz
Mod Char: delta f2 max <sup>c</sup>	–	99.9	–	–	%
Mod Char: ratio	–	0.8	0.95	–	%

a. The Bluetooth tester is set so that Dirty TX is on.

b. BLE TX power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc.). The output is capped at 12 dBm. The BLE TX power at the antenna port cannot exceed the 10 dBm specification limit.

c. At least 99.9% of all delta F2 max. frequency values recorded over 10 packets must be greater than 185 kHz.

## Section 18: FM Receiver Specifications



**Note:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in [Table 21: “Environmental Ratings,” on page 93](#) and [Table 23: “Recommended Operating Conditions and DC Characteristics,” on page 94](#). Typical values apply for the following conditions:

- VBAT = 3.6V.
- Ambient temperature +25°C.

**Table 32: FM Receiver Specifications**

Parameter	Conditions <sup>a</sup>	Minimum	Typical	Maximum	Units
<b>RF Parameters</b>					
Operating frequency <sup>b</sup>	Frequencies inclusive	65	–	108	MHz
Sensitivity <sup>c</sup>	FM only, SNR ≥ 26 dB	–	–0.5	–	dBμV EMF
		–	0.95	–	μV EMF
		–	–6.5	–	dBμV
Receiver adjacent channel selectivity <sup>c,d</sup>	Measured for 30 dB SNR at audio output. Signal of interest: 23 dBμV EMF (14.1 μV EMF).				
	At ±200 kHz.	–	51	–	dB
	At ±300 kHz.	–	62	–	dB
Intermediate signal-plus-noise to noise ratio (S + N)/N, stereo <sup>c</sup>	Vin = 20 dBμV (10 μV EMF).	45	53	–	dB
Intermodulation performance <sup>c,d</sup>	Blocker level increased until desired at 30 dB SNR. Wanted signal: 33 dBμV EMF (45 μV EMF) Modulated interferer: At $f_{\text{Wanted}} \pm 400$ kHz and $\pm 4$ MHz. CW interferer: At $f_{\text{Wanted}} \pm 800$ kHz and $\pm 8$ MHz.	–	55	–	dBc
AM suppression, mono <sup>c</sup>	Vin = 23 dBμV EMF (14.1 μV EMF). AM at 400 Hz with m = 0.3. No A-weighted or any other filtering applied.	40	–	–	dB

**Table 32: FM Receiver Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions<sup>a</sup></b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Units</b>
<b>RDS</b>					
RDS sensitivity <sup>e,f</sup>	RDS deviation = 1.2 kHz.	–	16	–	dB $\mu$ V EMF
		–	6.3	–	$\mu$ V EMF
		–	10	–	dB $\mu$ V
	RDS deviation = 2 kHz.	–	12	–	dB $\mu$ V EMF
		–	4	–	$\mu$ V EMF
		–	6	–	dB $\mu$ V
RDS selectivity <sup>f</sup>	Wanted Signal: 33 dB $\mu$ V EMF (45 $\mu$ V EMF), 2 kHz RDS deviation. Interferer: $\Delta f$ = 40 kHz, $f_{mod}$ = 1 kHz.				
	$\pm 200$ kHz	–	49	–	dB
	$\pm 300$ kHz	–	52	–	dB
	$\pm 400$ kHz	–	52	–	dB
<b>RF Input</b>					
RF input impedance	–	1.5	–	–	k $\Omega$
Antenna tuning cap	–	2.5	–	30	pF
Maximum input level <sup>c</sup>	SNR > 26 dB.	–	–	113	dB $\mu$ V EMF
		–	–	446	mV EMF
		–	–	107	dB $\mu$ V
RF conducted emissions	Local oscillator breakthrough measured on the reference port.	–	–	–55	dBm
	869–894 MHz, 925–960 MHz, 1805–1880 MHz, and 1930–1990 MHz. GPS.	–	–	–90	dBm

**Table 32: FM Receiver Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions<sup>a</sup></b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Units</b>
RF blocking levels at the FM antenna input with a 40 dB SNR (assumes a 50Ω input and excludes spurs)	GSM850, E-GSM (standard); BW = 0.2 MHz. 824–849 MHz, 880–915 MHz.	–	7	–	dBm
	GSM 850, E-GSM (edge); BW = 0.2 MHz. 824–849 MHz, 880–915 MHz.	–	0	–	dBm
	GSM DCS 1800, PCS 1900 (standard, edge); BW = 0.2 MHz. 1710–1785 MHz, 1850–1910 MHz.	–	12	–	dBm
	WCDMA: II (I), III (IV,X); BW = 5 MHz. 1710–1785 MHz (1710–1755 MHz, 1710–1770 MHz), 1850–1980 MHz (1920–1980 MHz).	–	12	–	dBm
	WCDMA: V (VI), VIII, XII, XIII, XIV; BW = 5 MHz. 824–849 MHz (830–840 MHz), 880–915 MHz.	–	5	–	dBm
	CDMA2000, CDMA One; BW = 1.25 MHz. 776–794 MHz, 824–849 MHz, 887–925 MHz.	–	0	–	dBm
	CDMA2000, CDMA One; BW= 1.25 MHz. 1750–1780 MHz, 1850–1910 MHz, 1920–1980 MHz.	–	12	–	dBm
	Bluetooth; BW = 1 MHz. 2402–2480 MHz.	–	11	–	dBm
	LTE, Band 38, Band 40, XGP Band	–	11	–	dBm
	WLAN-g/b; BW = 20 MHz. 2400–2483.5 MHz.	–	11	–	dBm
	WLAN-a; BW = 20 MHz. 4915–5825 MHz.	–	6	–	dBm
<b>Tuning</b>					
Frequency step	–	10	–	–	kHz
Settling time	Single frequency switch in any direction to a frequency within the 88–108 MHz or 76–90 MHz bands. Time measured to within 5 kHz of the final frequency.	–	150	–	μs
Search time	Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (or in the reverse direction) assuming no channels are found.	–	–	8	sec



**Table 32: FM Receiver Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions<sup>a</sup></b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Units</b>
<b>General Audio</b>					
Audio output level <sup>g</sup>	–	–14.5	–	–12.5	dBFS
Maximum audio output level <sup>h</sup>	–	–	–	0	dBFS
DAC audio output level	Conditions: Vin = 66 dBμV EMF (2 mV EMF), Δf = 22.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz	72	–	88	mV RMS
Maximum DAC audio output level <sup>h</sup>	–	–	333	–	mV RMS
Audio DAC output level difference <sup>i</sup>	–	–1	–	1	dB
Left and right AC mute	FM input signal fully muted with DAC enabled	60	–	–	dB
Left and right hard mute	FM input signal fully muted with DAC disabled	80	–	–	dB
Soft mute attenuation and start level	Muting is performed dynamically, proportional to the desired FM input signal C/N. The muting characteristic is fully programmable. See <a href="#">“Audio Features” on page 71</a> .				
Maximum signal plus noise-to-noise ratio (S + N)/N, mono <sup>i</sup>	–	–	69	–	dB
Maximum signal plus noise-to-noise ratio (S + N)/N, stereo <sup>g</sup>	–	–	64	–	dB
Total harmonic distortion, mono	Vin = 66 dBμV EMF(2 mV EMF):				
	Δf = 75 kHz, fmod = 400 Hz.	–	–	0.8	%
	Δf = 75 kHz, fmod = 1 kHz.	–	–	0.8	%
	Δf = 75 kHz, fmod = 3 kHz.	–	–	0.8	%
	Δf = 100 kHz, fmod = 1 kHz.	–	–	1.0	%
Total harmonic distortion, stereo	Vin = 66 dBμV EMF (2 mV EMF), Δf = 67.5 kHz, fmod = 1 kHz, Δf pilot = 6.75 kHz, L = R	–	–	1.5	%
Audio spurious products <sup>i</sup>	Range from 300 Hz to 15 kHz with respect to a 1 kHz tone.	–	–	–60	dBc
Audio bandwidth, upper (–3 dB point)	Vin = 66 dBμV EMF (2 mV EMF) Δf = 8 kHz, for 50 μs	15	–	–	kHz
Audio bandwidth, lower (–3 dB point)		–	–	20	Hz
Audio in-band ripple	100 Hz to 13 kHz, Vin = 66 dBμV EMF (2 mV EMF), Δf = 8 kHz, for 50 μs.	–0.5	–	0.5	dB
Deemphasis time constant tolerance	With respect to 50 and 75 μs.	–	–	±5	%

**Table 32: FM Receiver Specifications (Cont.)**

Parameter	Conditions <sup>a</sup>	Minimum	Typical	Maximum	Units
RSSI range	With 1 dB resolution and ±5 dB accuracy at room temperature.	3	—	83	dBμV EMF
		1.41	—	1.41E+4	μV EMF
		−3	—	77	dBμV
Stereo Decoder					
Stereo channel separation	Forced Stereo mode Vin = 66 dBμV EMF (2 mV EMF), Δf = 67.5 kHz, fmod = 1 kHz, Δf Pilot = 6.75 kHz, R = 0, L = 1	—	48	—	dB
Mono stereo blend and switching	Dynamically proportional to the desired FM input signal C/N. The blending and switching characteristics are fully programmable. See “Audio Features” on page 71.				
Pilot suppression	Vin = 66 dBμV EMF (2 mV EMF), Δf = 75 kHz, fmod = 1 kHz.	46	—	—	dB
Pause Detection					
Audio level at which a pause is detected	Relative to 1-kHz tone, Δf = 22.5 kHz.	—	—	—	—
	4 values in 3 dB steps	−21	—	−12	dB
Audio pause duration	4 values	20	—	40	ms

- The following conditions are applied to all relevant tests unless otherwise indicated: Preemphasis and deemphasis of 50  $\mu$ s, R = L for mono, BAF = 300 Hz to 15 kHz, A-weighted filtering applied.
- Contact your Broadcom representative for applications operating between 65–76 MHz.
- Signal of interest:  $\Delta f$  = 22.5 kHz,  $f_{mod}$  = 1 kHz.
- Interferer:  $\Delta f$  = 22.5 kHz,  $f_{mod}$  = 1 kHz.
- RDS sensitivity numbers are for 87.5–108 MHz only.
- $V_{in}$  =  $\Delta f$  = 32 kHz,  $f_{mod}$  = 1 kHz,  $\Delta f$  pilot = 7.5 kHz, and with an interferer for 95% of blocks decoded with no errors after correction, over a sample of 5000 blocks.
- $V_{in}$  = 66 dB $\mu$ V EMF (2 mV EMF),  $\Delta f$  = 22.5 kHz,  $f_{mod}$  = 1 kHz,  $\Delta f$  pilot = 6.75 kHz.
- $V_{in}$  = 66 dB $\mu$ V EMF (2 mV EMF),  $\Delta f$  = 100 kHz,  $f_{mod}$  = 1 kHz,  $\Delta f$  pilot = 6.75 kHz.
- $V_{in}$  = 66 dB $\mu$ V EMF (2 mV EMF),  $\Delta f$  = 22.5 kHz,  $f_{mod}$  = 1 kHz.

## Section 19: Internal Regulator Electrical Specifications



**Note:** Values in this data sheet are design goals and are subject to change based on device characterization results.

Functional operation is not guaranteed outside of the specification limits provided in this section.

### Core Buck Switching Regulator

**Table 33: Core Buck Switching Regulator (CBUCK) Specifications**

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	2.4	3.6	4.8 <sup>a</sup>	V
PWM mode switching frequency	CCM, load > 100 mA VBAT = 3.6V.	–	4	–	MHz
PWM output current	–	–	–	370	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V.	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static load, max. ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, Cout > 1.9 µF, ESL < 200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak efficiency at 200 mA load, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	85	–	%
PFM mode efficiency	10 mA load current, inductor DCR = 200 mΩ, VBAT = 3.6V, VOUT = 1.35V	–	77	–	%
Start-up time from power down	VDDIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V	–	400	500	µs
External inductor	0603 size, 2.2 µH ±20%, DCR = 0.2Ω ± 25%	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, 4.7 µF ±20%, 10V	2.0 <sup>b</sup>	4.7	10 <sup>c</sup>	µF

**Table 33: Core Buck Switching Regulator (CLOCK) Specifications (Cont.)**

<b>Specification</b>	<b>Notes</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7 μF ±20%, 10V	0.67 <sup>b</sup>	4.7	–	μF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	μs

- a. The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
- b. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.
- c. Total capacitance includes those connected at the far end of the active load.

## 3.3V LDO (LDO3P3)

**Table 34: LDO3P3 Specifications**

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, $V_{in}$	Min. = $V_o + 0.2V = 3.5V$ dropout voltage requirement must be met under maximum load for performance specifications.	3.1	3.6	4.8 <sup>a</sup>	V
Output current	–	0.001	–	450	mA
Nominal output voltage, $V_o$	Default = 3.3V.	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	66	85	$\mu A$
Line regulation	$V_{in}$ from ( $V_o + 0.2V$ ) to 4.8V, max. load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o + 0.2V$ , $V_o = 3.3V$ , $C_o = 4.7 \mu F$ , Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	$\mu s$
External output capacitor, $C_o$	Ceramic, X5R, 0402, (ESR: 5 m $\Omega$ –240 m $\Omega$ ), $\pm 10\%$ , 10V	1.0 <sup>b</sup>	4.7	5.64	$\mu F$
External input capacitor	For SR_VDDBATA5V pin (shared with band gap) Ceramic, X5R, 0402, (ESR: 30m-200 m $\Omega$ ), $\pm 10\%$ , 10V. Not needed if sharing VBAT capacitor 4.7 $\mu F$ with SR_VDDBATP5V.	–	4.7	–	$\mu F$

- The maximum continuous voltage is 4.8V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
- Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

## CLDO

**Table 35: CLDO Specifications**

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, $V_{in}$	Min. = $1.2 + 0.15V = 1.35V$ dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	200	mA
Output voltage, $V_o$	Programmable in 10 mV steps. Default = 1.2V	0.95	1.2	1.26	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	13	–	$\mu A$
	200 mA load	–	1.24	–	mA
Line regulation	$V_{in}$ from ( $V_o + 0.15V$ ) to 1.5V, maximum load	–	–	5	mV/V
Load regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage current	Power down	–	5	20	$\mu A$
	Bypass mode	–	1	3	$\mu A$
PSRR	@1 kHz, $V_{in} \geq 1.35V$ , $C_o = 4.7 \mu F$	20	–	–	dB
Start-up time of PMU	VDDIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	$\mu s$
LDO turn-on time	LDO turn-on time when rest of the chip is up.	–	140	180	$\mu s$
External output capacitor, $C_o$	Total ESR: 5 m $\Omega$ –240 m $\Omega$	1.1 <sup>a</sup>	2.2	–	$\mu F$
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	$\mu F$

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

## LNLDO

**Table 36: LNLDO Specifications**

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, $V_{in}$	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$ ) dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.1	–	150	mA
Output voltage, $V_O$	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout voltage	At maximum load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	10	12	$\mu A$
	Max. load	–	970	990	$\mu A$
Line regulation	$V_{in}$ from ( $V_O + 0.15V$ ) to 1.5V, 200 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 200 mA: $V_{in} \geq (V_O + 0.12V)$	–	0.025	0.045	mV/mA
Leakage current	Power-down, junction temp. = 85°C	–	5	20	$\mu A$
Output noise	@30 kHz, 60–150 mA load $C_O = 2.2 \mu F$	–	–	60	$nV/\sqrt{Hz}$
	@100 kHz, 60–150 mA load $C_O = 2.2 \mu F$	–	–	35	
PSRR	@1 kHz, $V_{in} \geq (V_O + 0.15V)$ , $C_O = 4.7 \mu F$	20	–	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	140	180	$\mu s$
External output capacitor, $C_O$	Total ESR (trace/capacitor): 5 m $\Omega$ –240 m $\Omega$	0.5 <sup>a</sup>	2.2	4.7	$\mu F$
External input capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CLOCK output. Total ESR (trace/capacitor): 30 m $\Omega$ –200 m $\Omega$	–	1	2.2	$\mu F$

a. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

## Section 20: System Power Consumption



### Note:

- Values in this data sheet are design goals and are subject to change based on device characterization.
- Unless otherwise stated, these values apply for the conditions specified in [Table 23: "Recommended Operating Conditions and DC Characteristics," on page 94.](#)

## WLAN Current Consumption

The tables in this subsection show the typical, total current consumed by the BCM43438 when configured to use external PAs. To calculate the total solution's current consumption, add the external PA's current consumption to these numbers. All values shown are with the Bluetooth core in reset mode with Bluetooth and FM are off.

### 2.4 GHz Mode

**Table 37: 2.4 GHz Mode WLAN Power Consumption**

Mode	VBAT = 3.6V, VDDIO = 1.8V, T <sub>A</sub> 25°C	
	VBAT (mA)	VDDIO (μA) <sup>a</sup>
<b>Sleep Modes</b>		
Radio off <sup>b</sup>	TBD	TBD
Sleep <sup>c</sup>	TBD	TBD
IEEE Power Save, DTIM=1 - single RX <sup>d</sup>	0.85	TBD
IEEE Power Save, DTIM=3 - single RX <sup>e</sup>	0.3	TBD
<b>Active Modes</b>		
Continuous RX mode MCS7 - HT20 - 1SS <sup>e, f</sup>	30	TBD
CRS- HT20 <sup>g</sup>	TBD	TBD
Continuous TX mode 1 Mbps <sup>g, h</sup>	TBD	TBD
Continuous TX mode MCS7 - HT20 - 1SS - 1 TX <sup>g, i</sup> @ +18 dBm	245	TBD

- VDDIO is specified with all pins idle (not switching) and not driving any loads.
- WL\_REG\_ON and BT\_REG\_ON are both low. All supplies are present.
- Idle, not associated, or inter-beacon.
- Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3x DTIM intervals.
- Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
- Measured using packet engine test mode.
- Carrier sense (CCA) when no carrier present.
- Duty cycle is 100%. Excludes external PA contribution.



## Bluetooth and FM Current Consumption

The Bluetooth, BLE, and FM current consumption measurements are shown in [Table 38](#).



**Note:**

- The WLAN core is in reset (WLAN\_REG\_ON = low) for all measurements provided in [Table 38](#).
- For FM measurements, the Bluetooth core is in Sleep mode.
- The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

**Table 38: Bluetooth BLE and FM Current Consumption**

<b>Operating Mode</b>	<b>VBAT (VBAT = 3.6V) Typical</b>	<b>VDDIO (VDDIO = 1.8V) Typical</b>	<b>Units</b>
Sleep	6	150	μA
Standard 1.28s Inquiry Scan	193	162	μA
500 ms Sniff Master	214	172	μA
DM1/DH1 Master	22.3	–	mA
DM3/DH3 Master	26.9	–	mA
DM5/DH5 Master	27.32	–	mA
3DH5/3DH1 Master	24.8	–	mA
SCO HV3 Master	10.86	–	mA
FMRX Analog Audio only <sup>a</sup>	8.6	–	mA
FMRX Analog Audio + RDS <sup>a</sup>	8.6	–	mA
BLE Scan <sup>b</sup>	187	164	μA
BLE Adv. – Unconnectable 1.00 sec	93	163	μA
BLE Connected 1 sec	71	163	μA

a. In Mono/Stereo blend mode.

b. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

# Section 21: Interface Timing and AC Characteristics



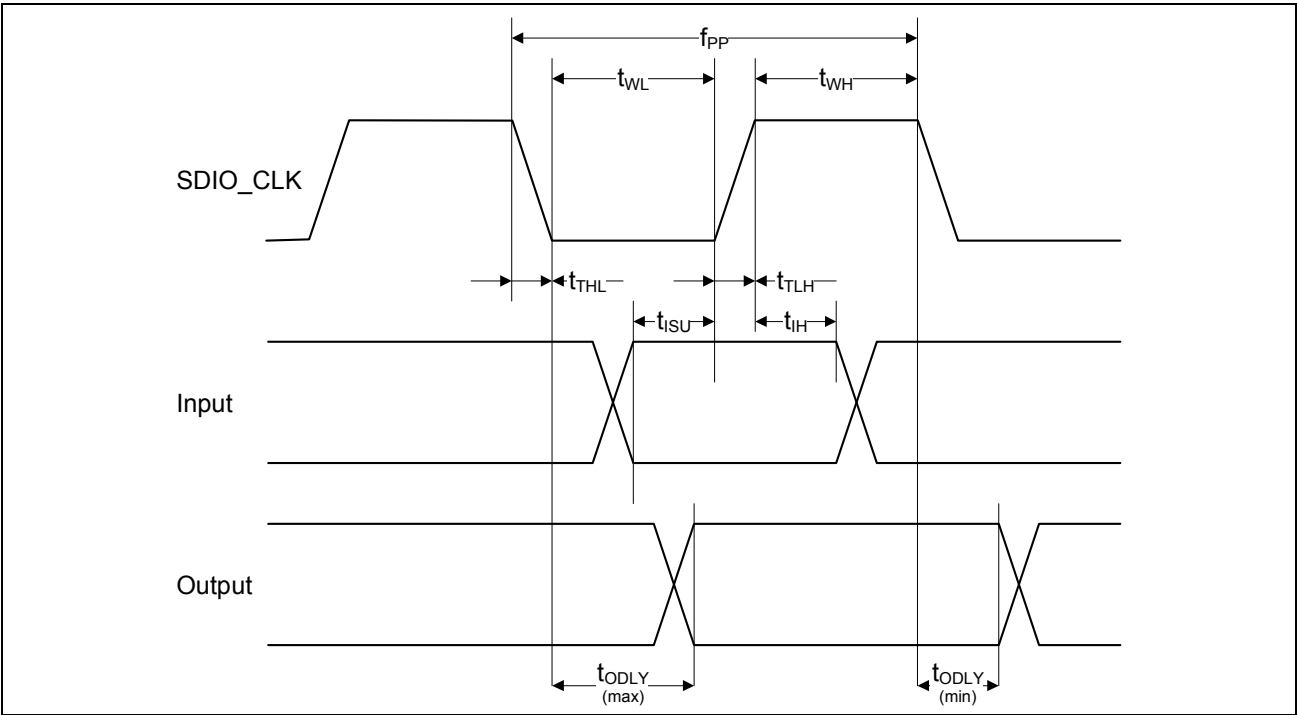
**Note:** Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in [Table 21 on page 93](#) and [Table 23 on page 94](#). Functional operation outside of these limits is not guaranteed.

## SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of [Figure 36](#) and [Table 39 on page 123](#).

**Figure 36: SDIO Bus Timing (Default Mode)**



**Table 39: SDIO Bus Timing <sup>a</sup> Parameters (Default Mode)**

<b>Parameter</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
Frequency—Data Transfer mode	fPP	0	—	25	MHz
Frequency—Identification mode	fOD	0	—	400	kHz
Clock low time	tWL	10	—	—	ns
Clock high time	tWH	10	—	—	ns
Clock rise time	tTLH	—	—	10	ns
Clock fall time	tTHL	—	—	10	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	tISU	5	—	—	ns
Input hold time	tIH	5	—	—	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time—Data Transfer mode	tODLY	0	—	14	ns
Output delay time—Identification mode	tODLY	0	—	50	ns

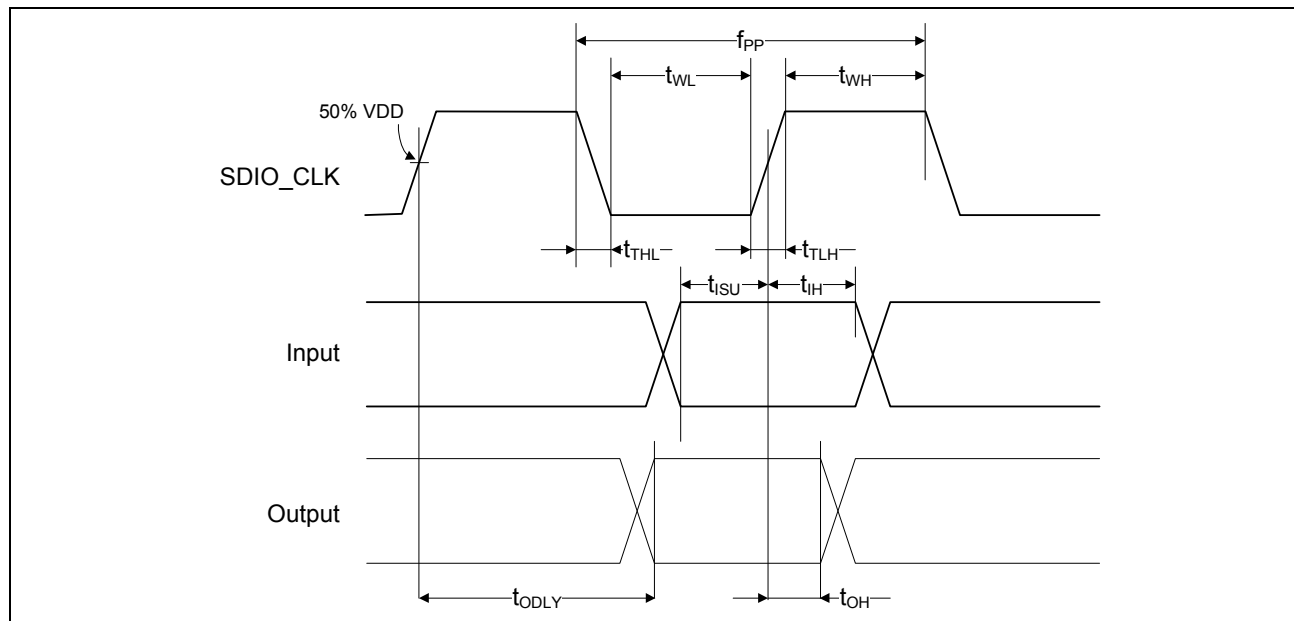
a. Timing is based on  $CL \leq 40$  pF load on command and data.

b.  $\min(V_{ih}) = 0.7 \times V_{DDIO}$  and  $\max(V_{il}) = 0.2 \times V_{DDIO}$ .

## SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of [Figure 37](#) and [Table 40](#).

**Figure 37: SDIO Bus Timing (High-Speed Mode)**



**Table 40: SDIO Bus Timing<sup>a</sup> Parameters (High-Speed Mode)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (all values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	tISU	6	–	–	ns
Input hold time	tIH	2	–	–	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

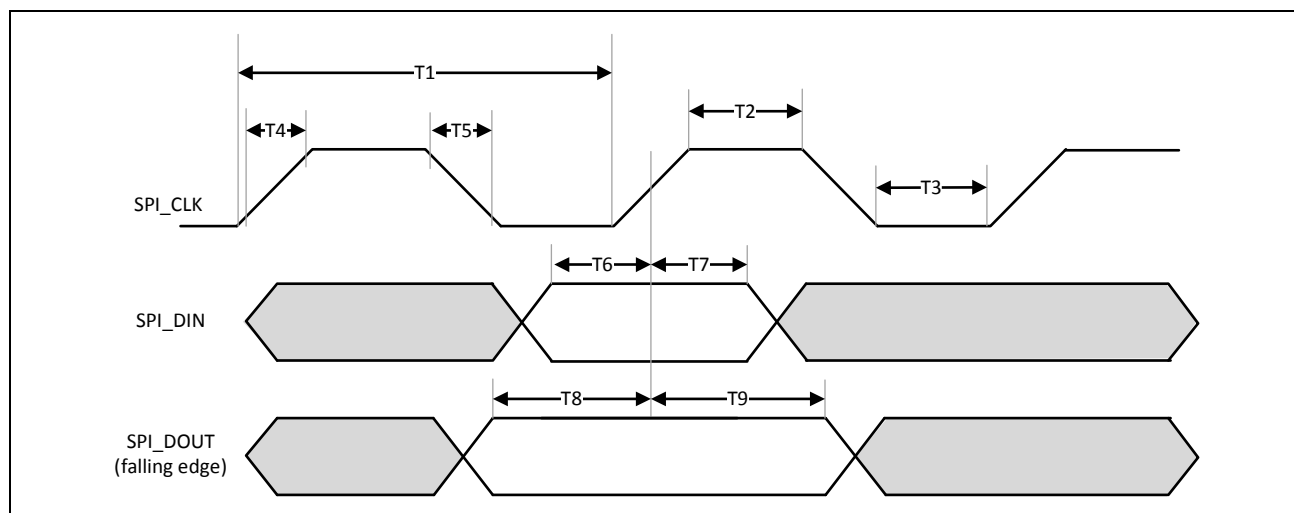
a. Timing is based on  $CL \leq 40$  pF load on command and data.

b.  $\min(V_{ih}) = 0.7 \times V_{DDIO}$  and  $\max(V_{il}) = 0.2 \times V_{DDIO}$ .

## gSPI Signal Timing

The gSPI device always samples data on the rising edge of the clock.

**Figure 38: gSPI Timing**



**Table 41: gSPI Timing Parameters**

Parameter	Symbol	Minimum	Maximum	Units	Note
Clock period	T1	20.8	–	ns	$F_{\max} = 50 \text{ MHz}$
Clock high/low	T2/T3	$(0.45 \times T1) - T4$	$(0.55 \times T1) - T4$	ns	–
Clock rise/fall time	T4/T5	–	2.5	ns	–
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock <sup>a</sup>	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX <sup>c</sup>	–	–	–	ns	Last falling edge to CSX high

a. SPI\_CSx remains active for entire duration of gSPI read/write/write\_read transaction (that is, overall words for multiple word transaction)

## JTAG Timing

*Table 42: JTAG Timing Characteristics*

<b>Signal Name</b>	<b>Period</b>	<b>Output Maximum</b>	<b>Output Minimum</b>	<b>Setup</b>	<b>Hold</b>
TCK	125 ns	—	—	—	—
TDI	—	—	—	20 ns	0 ns
TMS	—	—	—	20 ns	0 ns
TDO	—	100 ns	0 ns	—	—
JTAG_TRST	250 ns	—	—	—	—

## Section 22: Power-Up Sequence and Timing

### Sequencing of Reset and Regulator Control Signals

The BCM43438 has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see [Figure 39 on page 128](#) through [Figure 42 on page 129](#)). The timing values indicated are minimum required values; longer delays are also acceptable.

**Note:**

- The WL\_REG\_ON and BT\_REG\_ON signals are OR'ed in the BCM43438. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL\_REG\_ON and one for BT\_REG\_ON), then only one of the two signals needs to be high to enable the BCM43438 regulators.
- The reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.
- The BCM43438 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold (see [Table 23: "Recommended Operating Conditions and DC Characteristics," on page 94](#)). Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.
- VBAT and VDDIO should not rise faster than 40  $\mu$ s. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

### Description of Control Signals

- **WL\_REG\_ON:** Used by the PMU to power up the WLAN section. It is also OR-gated with the BT\_REG\_ON input to control the internal BCM43438 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT\_REG\_ON and WL\_REG\_ON pins are low, the regulators are disabled.
- **BT\_REG\_ON:** Used by the PMU (OR-gated with WL\_REG\_ON) to power up the internal BCM43438 regulators. If both the BT\_REG\_ON and WL\_REG\_ON pins are low, the regulators are disabled. When this pin is low and WL\_REG\_ON is high, the BT section is in reset.



**Note:** For both the WL\_REG\_ON and BT\_REG\_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

## Control Signal Timing Diagrams

Figure 39: WLAN = ON, Bluetooth = ON

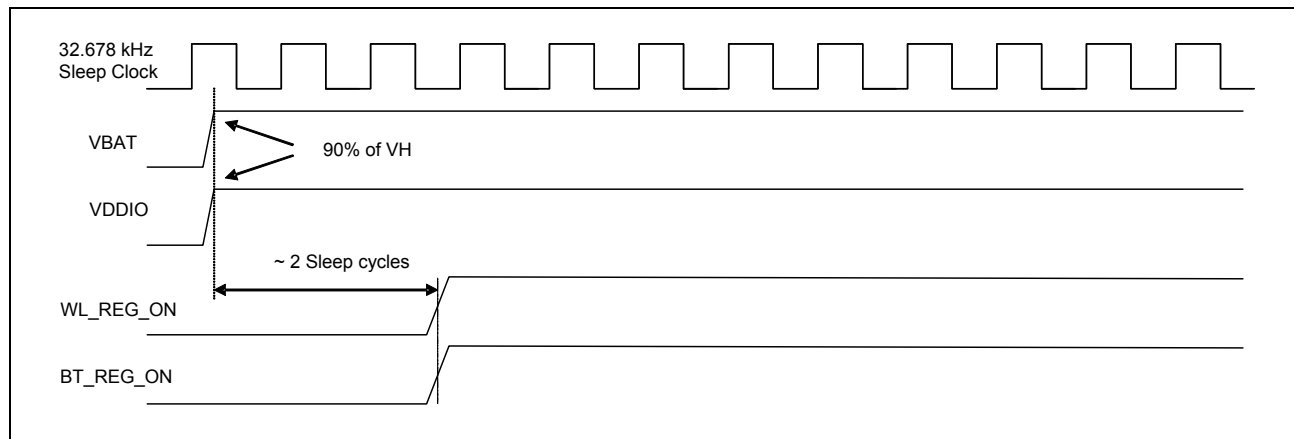


Figure 40: WLAN = OFF, Bluetooth = OFF

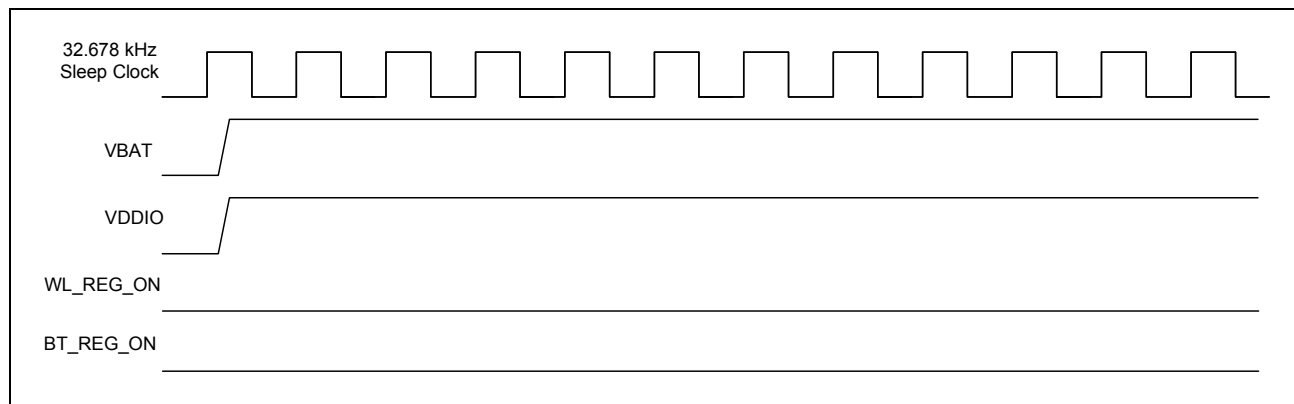
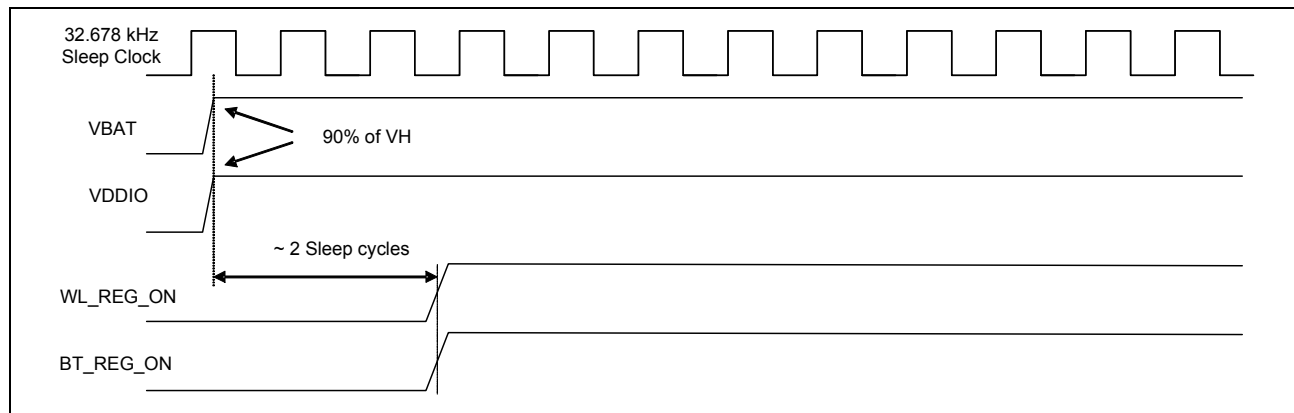
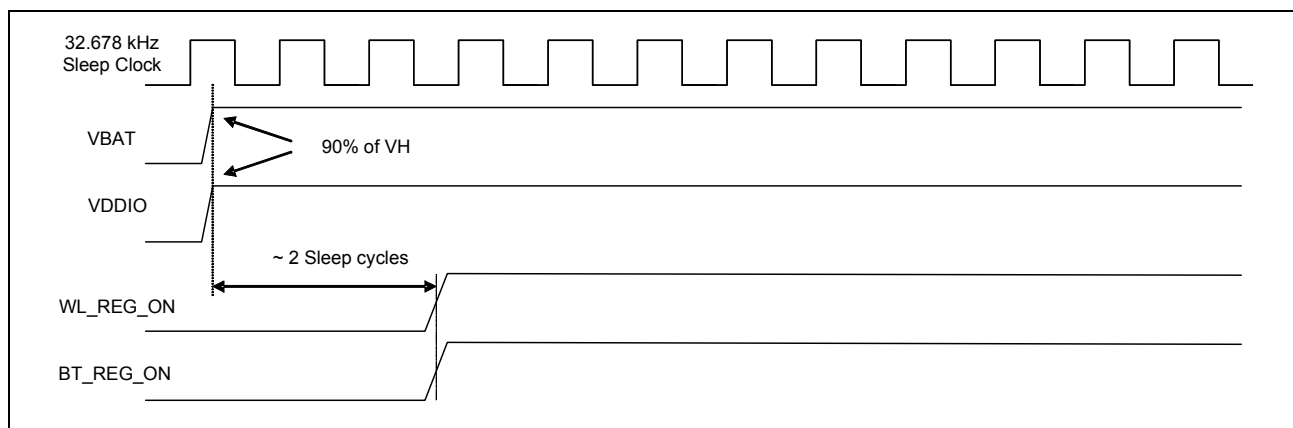


Figure 41: WLAN = ON, Bluetooth = OFF





**Figure 42: WLAN = OFF, Bluetooth = ON**

## Section 23: Package Information

### Package Thermal Characteristics

**Table 43: Package Thermal Characteristics<sup>a</sup>**

Characteristic	Value in Still Air
$\theta_{JA}$ (°C/W)	44.88
$\theta_{JB}$ (°C/W)	1.20
$\theta_{JC}$ (°C/W)	0.20
$\Psi_{JT}$ (°C/W)	0.04
$\Psi_{JB}$ (°C/W)	14.21
Maximum Junction Temperature $T_J$ (°C) <sup>b</sup>	125
Maximum Power Dissipation (W)	1.2

- a. No heat sink,  $T_A = 70^\circ\text{C}$ . This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51-7 (101.6 mm x 114.3 mm x 1.6 mm) and  $P = 1.2\text{W}$  continuous dissipation.
- b. Absolute junction temperature limits maintained through active thermal monitoring and dynamic TX duty cycle limiting.

### Junction Temperature Estimation and PSI Versus $\theta_{JC}$

Package thermal characterization parameter PSI-JT ( $\Psi_{JT}$ ) yields a better estimation of actual junction temperature ( $T_J$ ) versus using the junction-to-case thermal resistance parameter Theta-JC ( $\theta_{JC}$ ). The reason for this is  $\theta_{JC}$  assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package.  $\Psi_{JT}$  takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

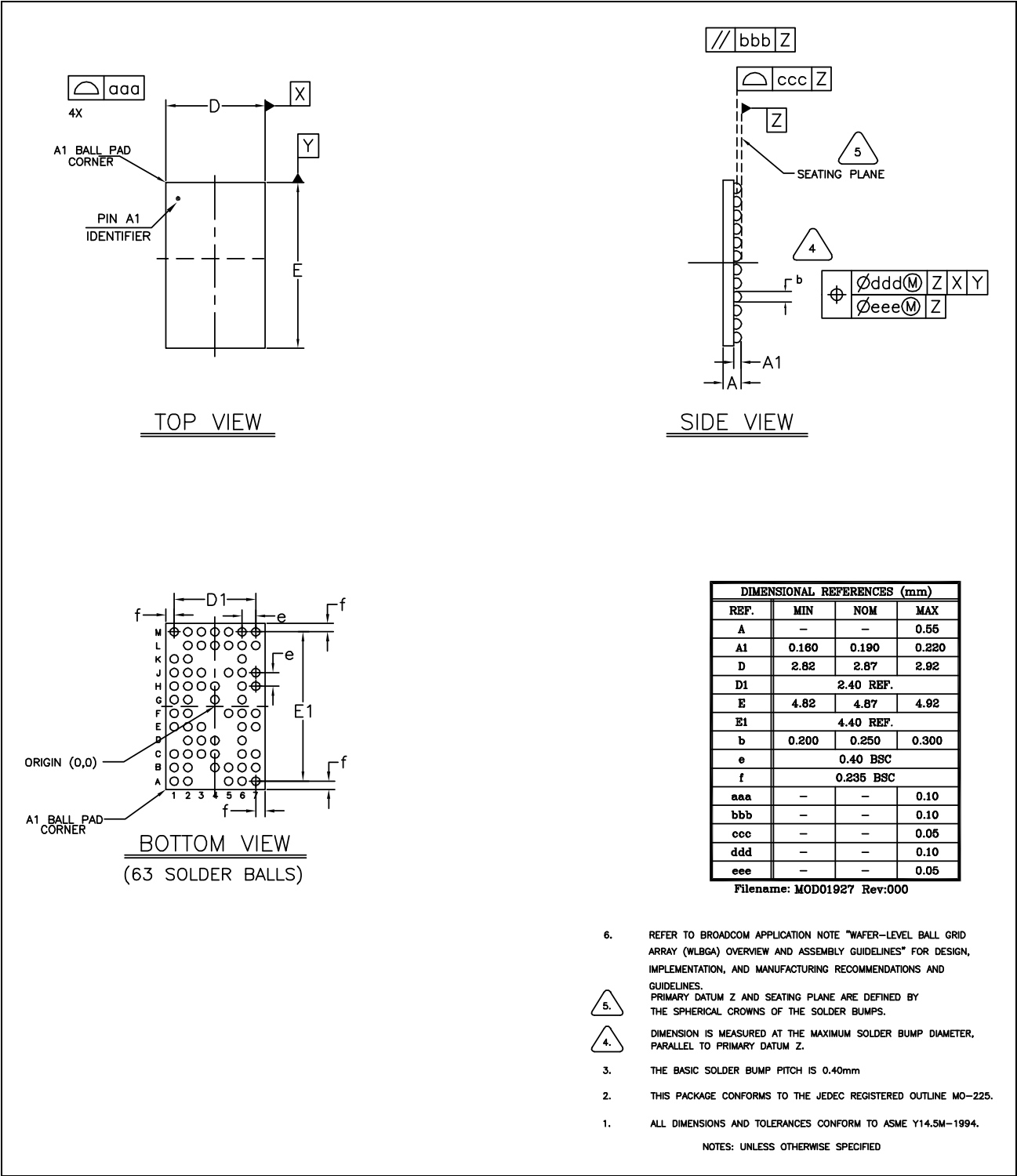
Where:

- $T_J$  = junction temperature at steady-state condition, °C
- $T_T$  = package case top center temperature at steady-state condition, °C
- $P$  = device power dissipation, Watts
- $\Psi_{JT}$  = package thermal characteristics (no airflow), °C/W

## Section 24: Mechanical Information

[Figure 43](#) shows the mechanical drawing for the BCM43438 WLBGA package.

Figure 43: 63-Ball WLBGA Mechanical Information



## Section 25: Ordering Information

<i><b>Part Number</b></i>	<i><b>Package</b></i>	<i><b>Description</b></i>	<i><b>Operating Ambient Temperature</b></i>
BCM43438KUBG	63-ball WLBGA halogen-free package (4.87 mm x 2.87 mm, 0.40 pitch)	2.4 GHz single-band WLAN IEEE 802.11n + BT 4.1 + FMRX	–30°C to +85°C
<b>Note:</b> Add a “T” to the end of the part number to specify “Tape and Reel”.			

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