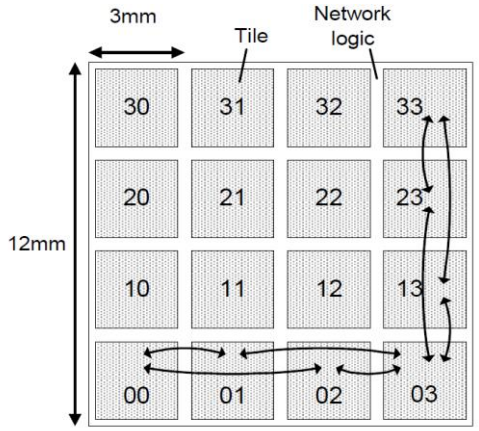
Reliable Network-on-Chip Architecture for Reliable Applications

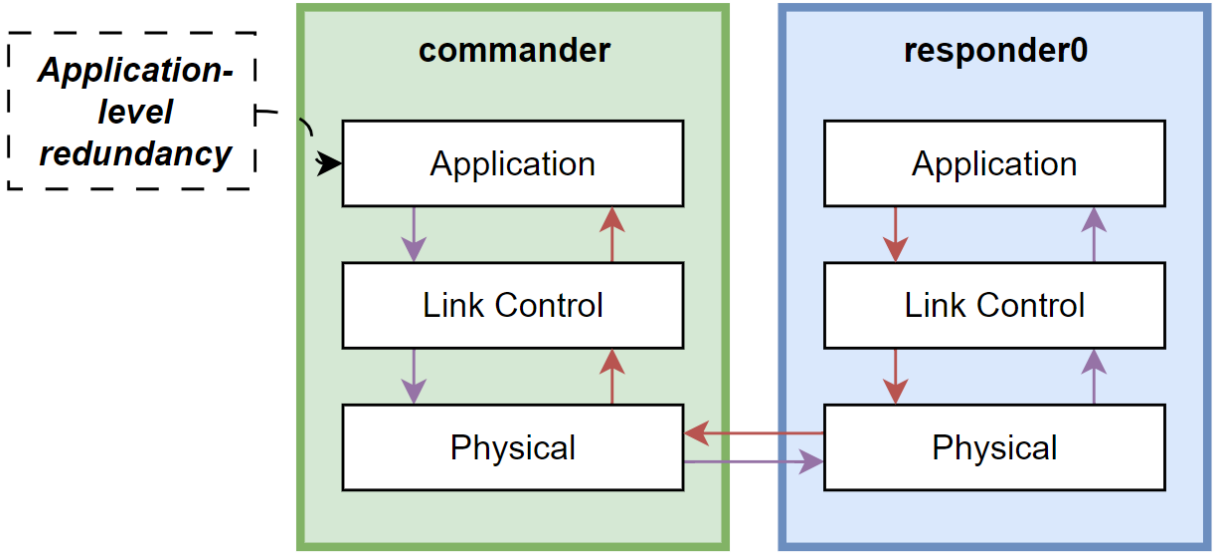
Michael Grieco

Introduction

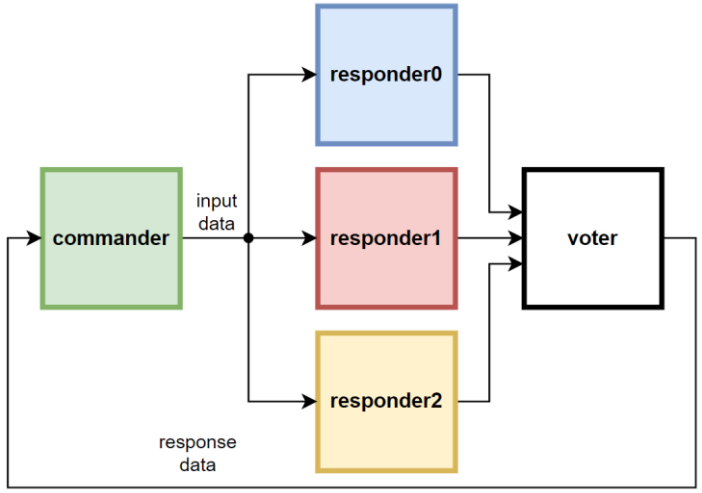


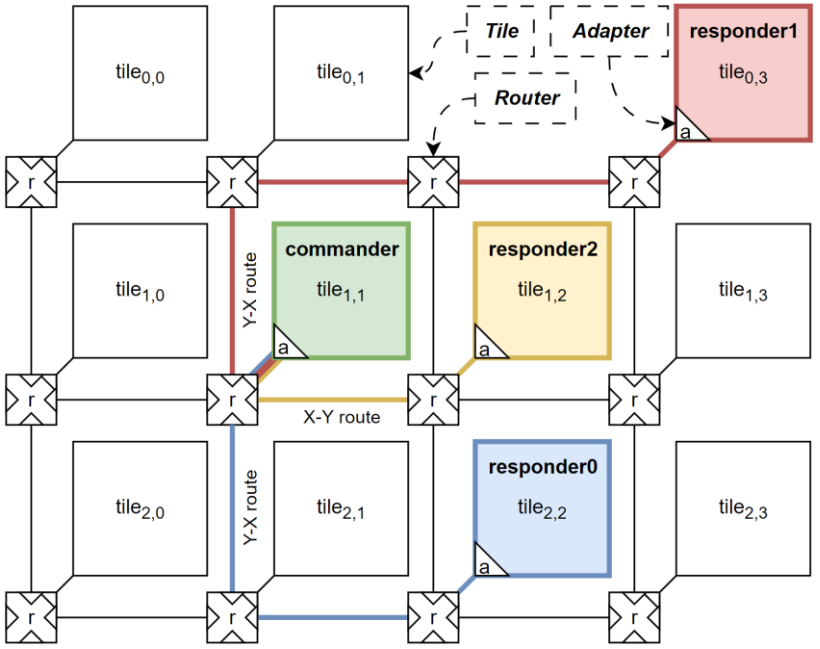
Dally, 2001.

Network-on-Chip



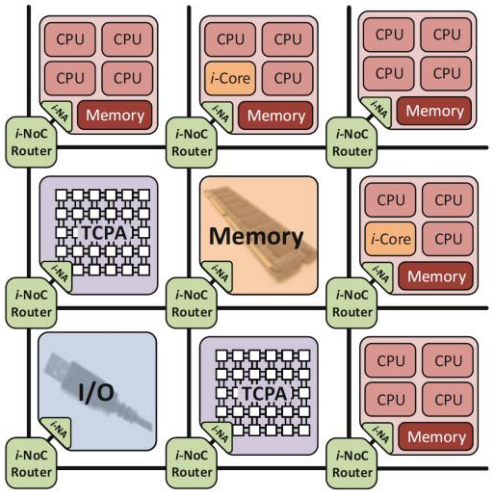
Fault-tolerance mechanisms



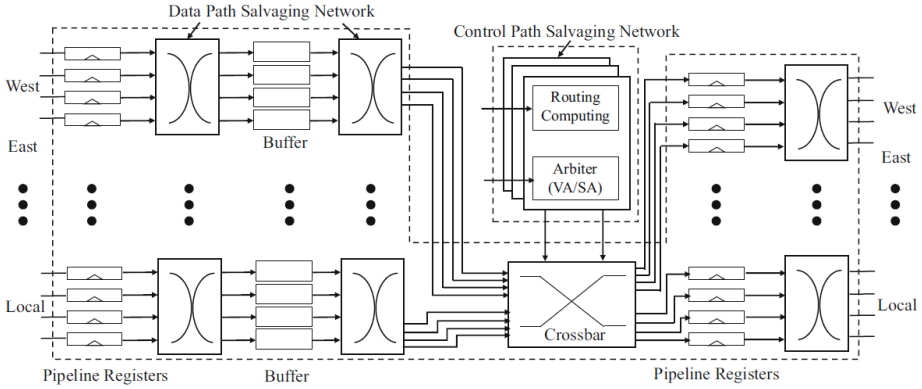


Related Work

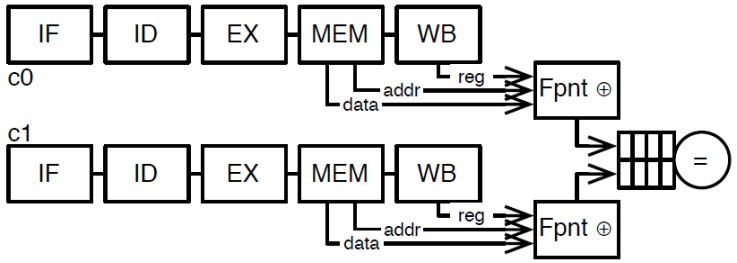
NoC-specific fault tolerance, **newer**



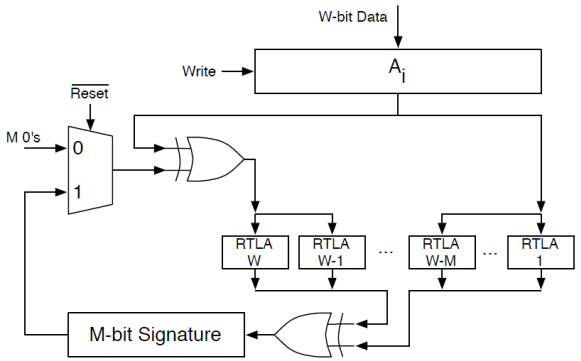
Weichslgartner et al., 2018.



Li et al., 2023.



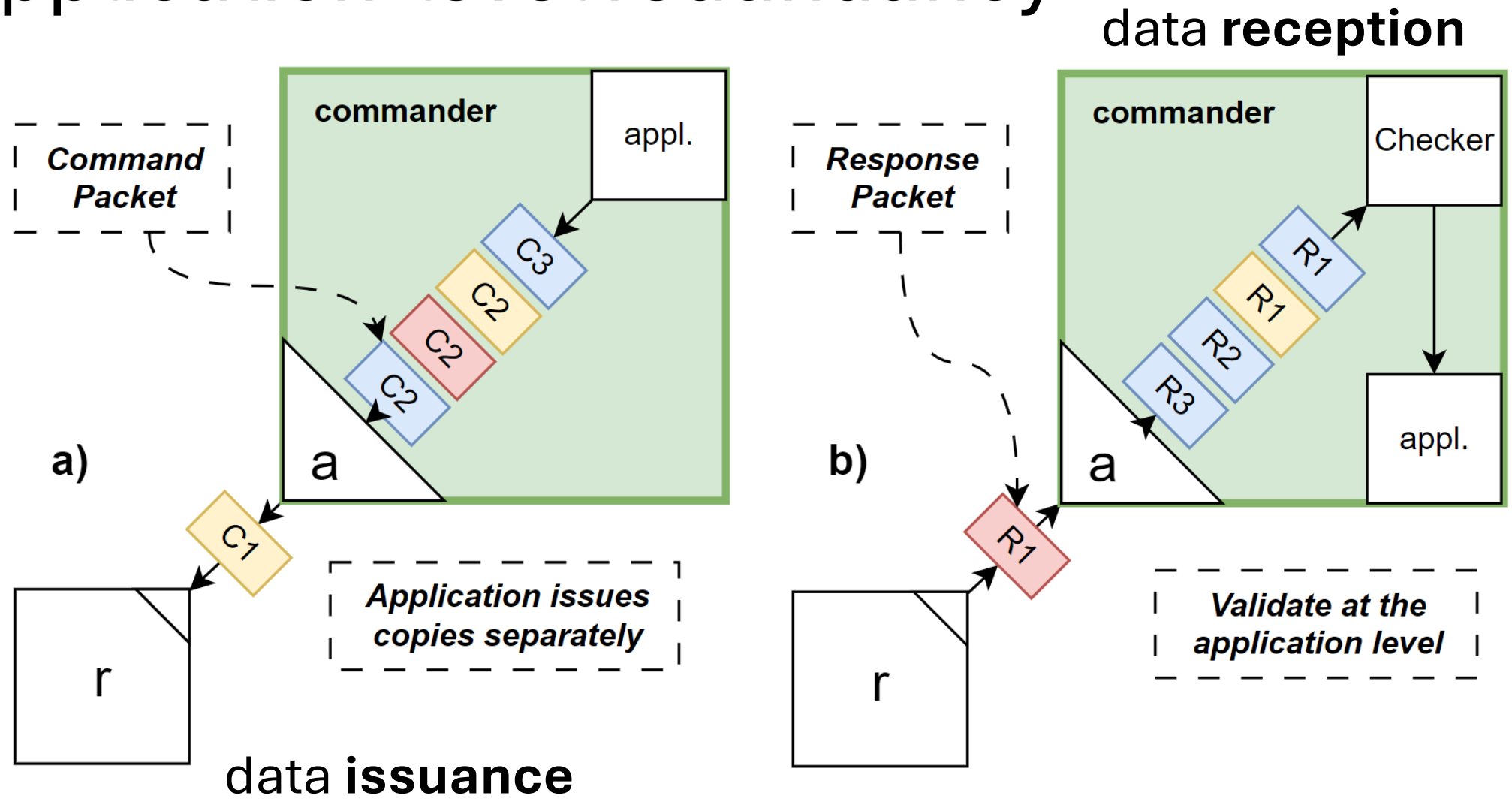
Meyer et al., 2011.



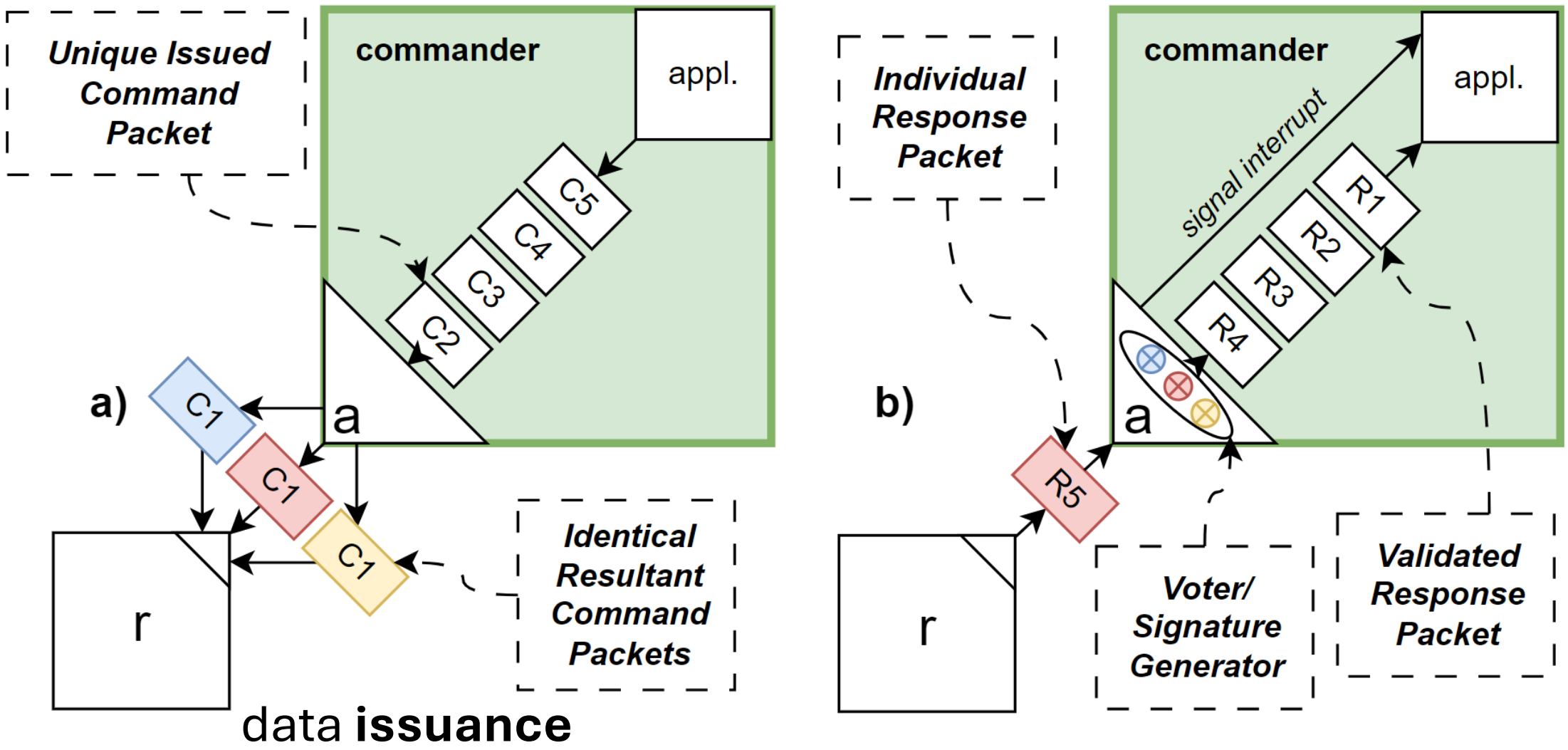
Caplan et al., 2014.

Redundancy-related methodologies, **not as new**

Application-level redundancy

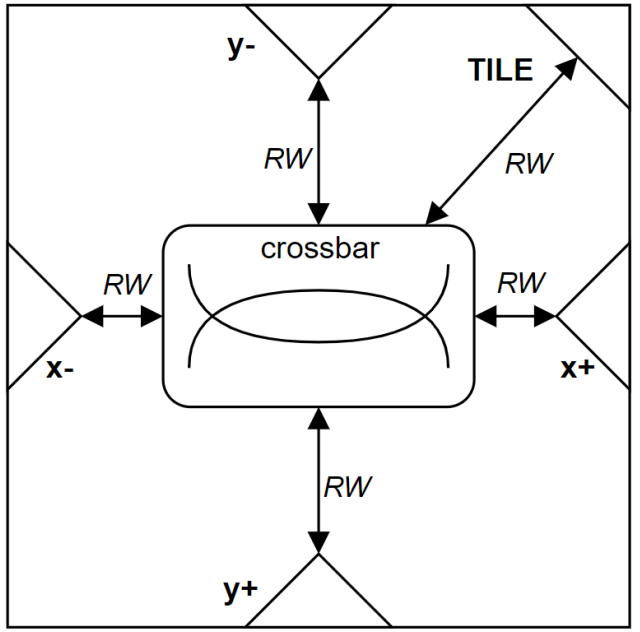


Solution

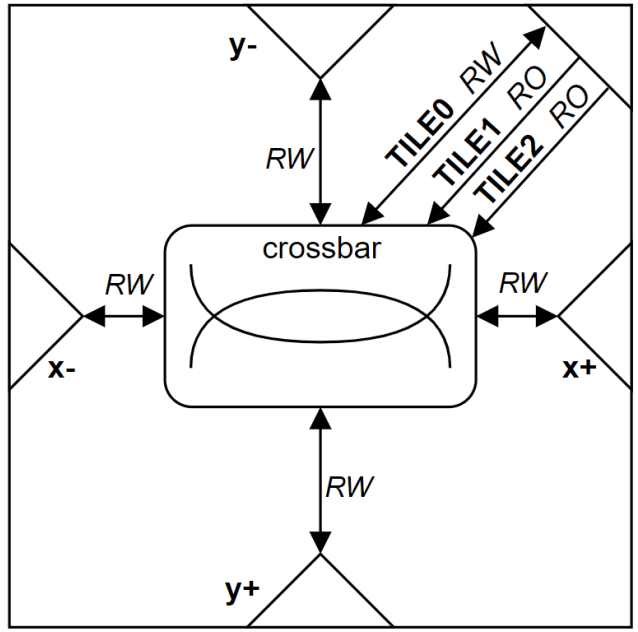


Solution

- Port types – RW, RO, WO
- Three ports with the adapter
- Crossbar: 7 input, 5 output



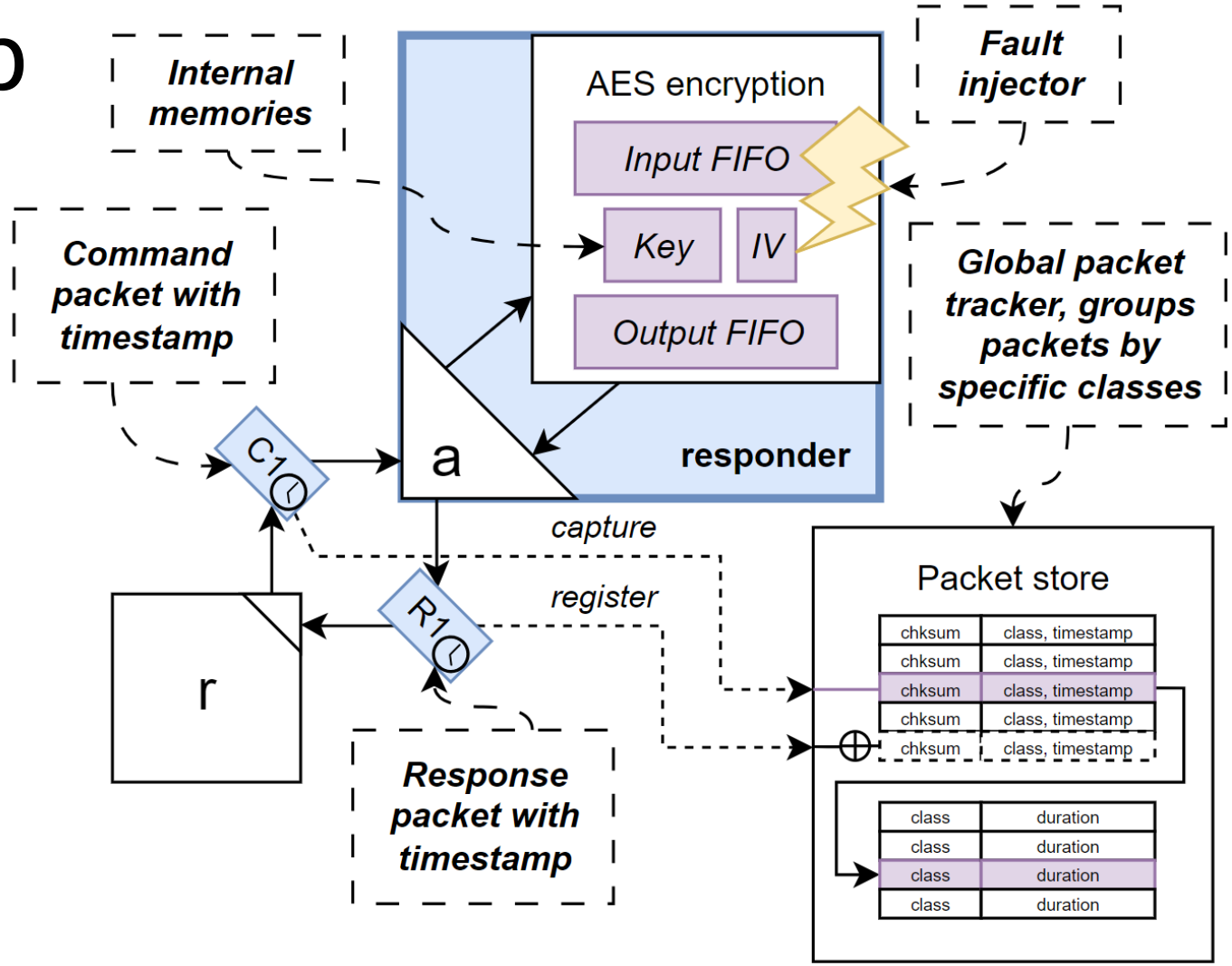
typical mesh router arch.



proposed router mesh arch.

Experimental Setup

- SystemC model of NoC
  - Typical mesh
  - With/without custom redundancy
  - TMR for AES-256-CBC
- Tools
  - latency measure
  - fault injection



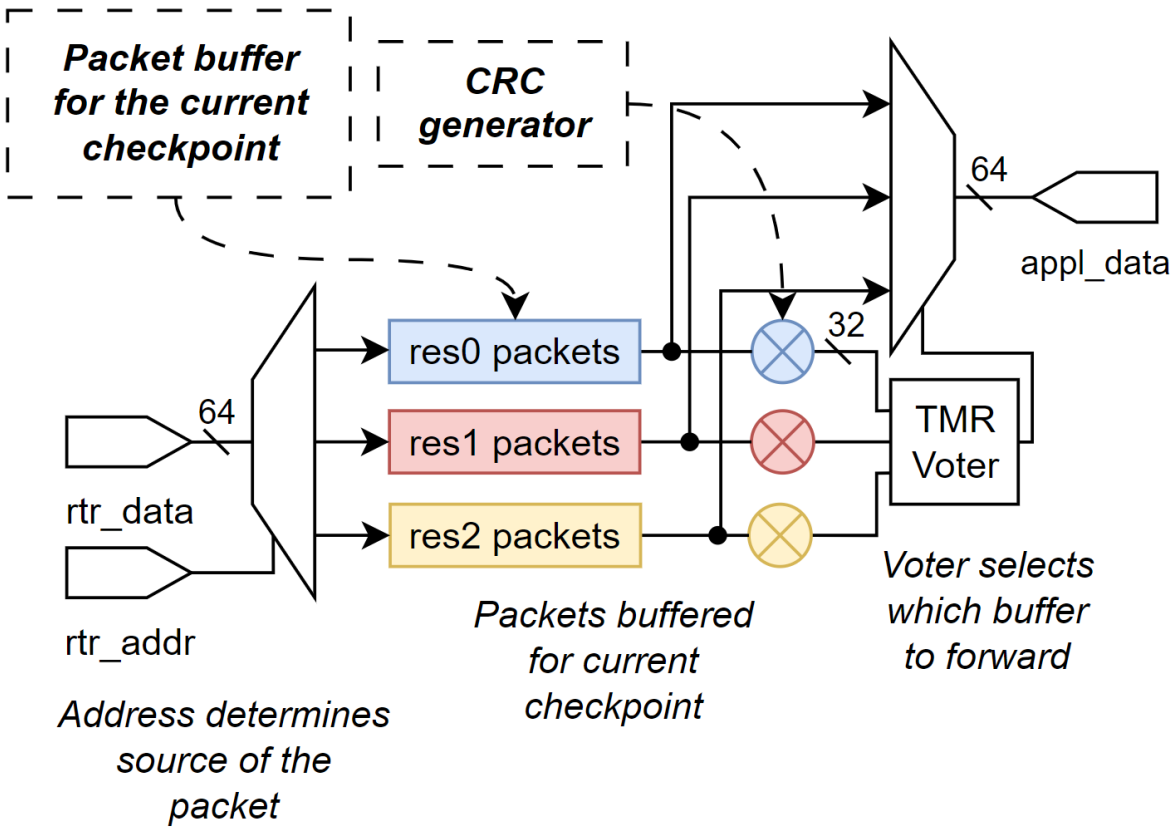
Results – fault-tolerance

- Functional compliance
- Compare to expected output

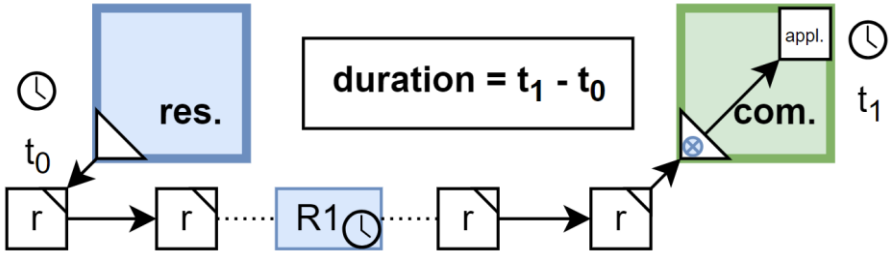
```
58 ns - Completed simulation, checking output...
Final report: 128 bytes compared, 0 errors
```

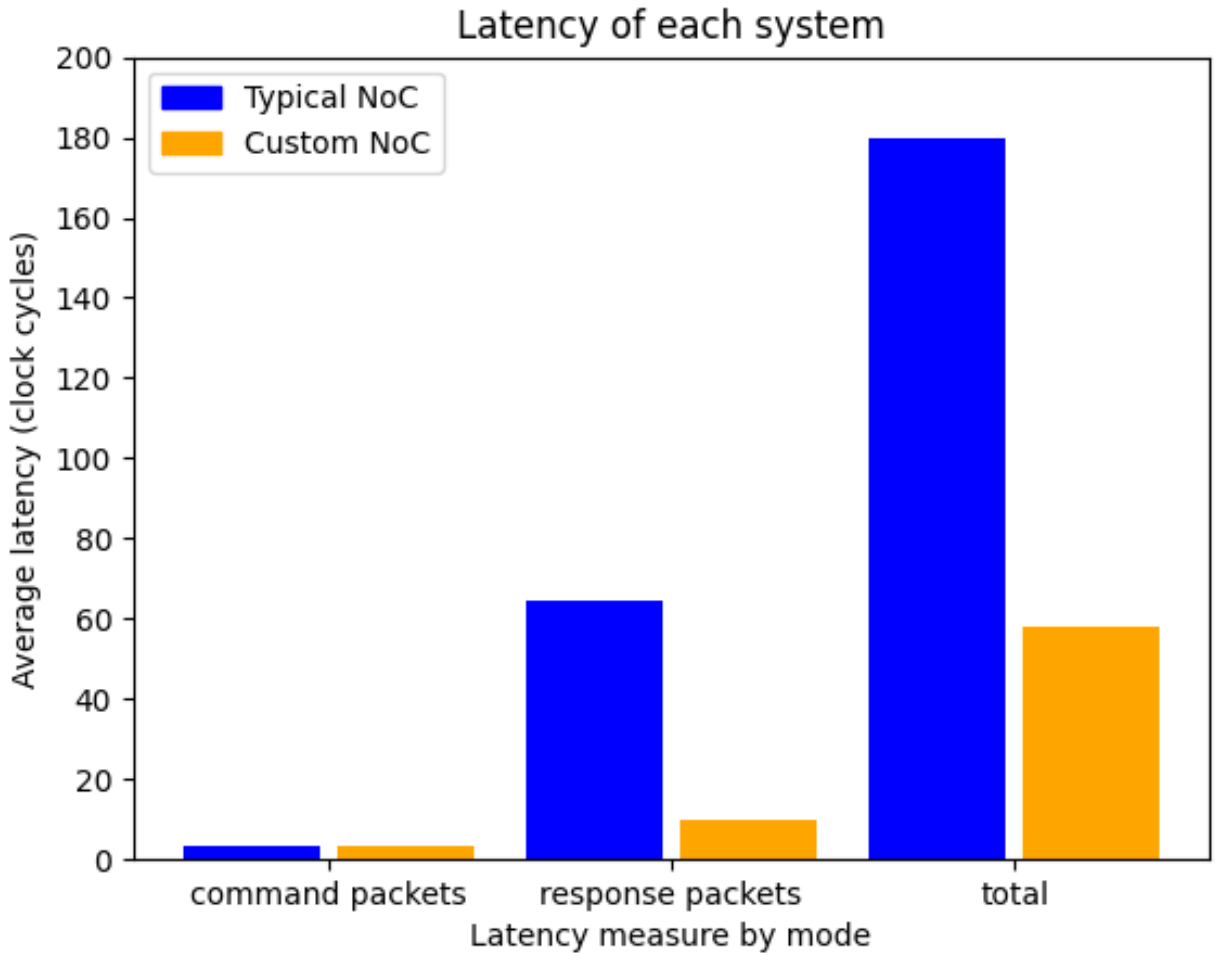
```
60 ns - Error detected in checkpoint at byte 00000020
60 ns - [commander]: Received interrupt with signal 1
60 ns - Completed simulation, checking output...
Final report: 32 bytes compared, 0 errors

Info: /OSCI/SystemC: Simulation stopped by user.
Total of 11 faults over 48 bytes.
```



Results – latency

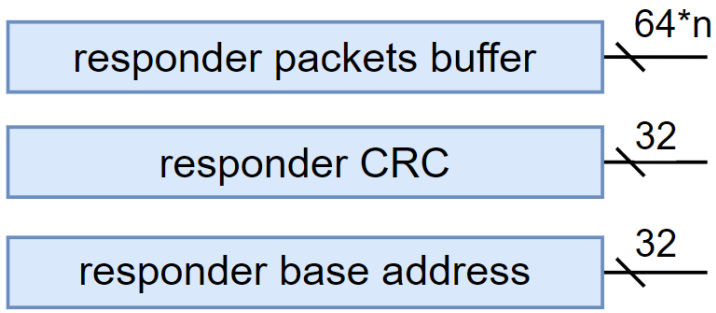


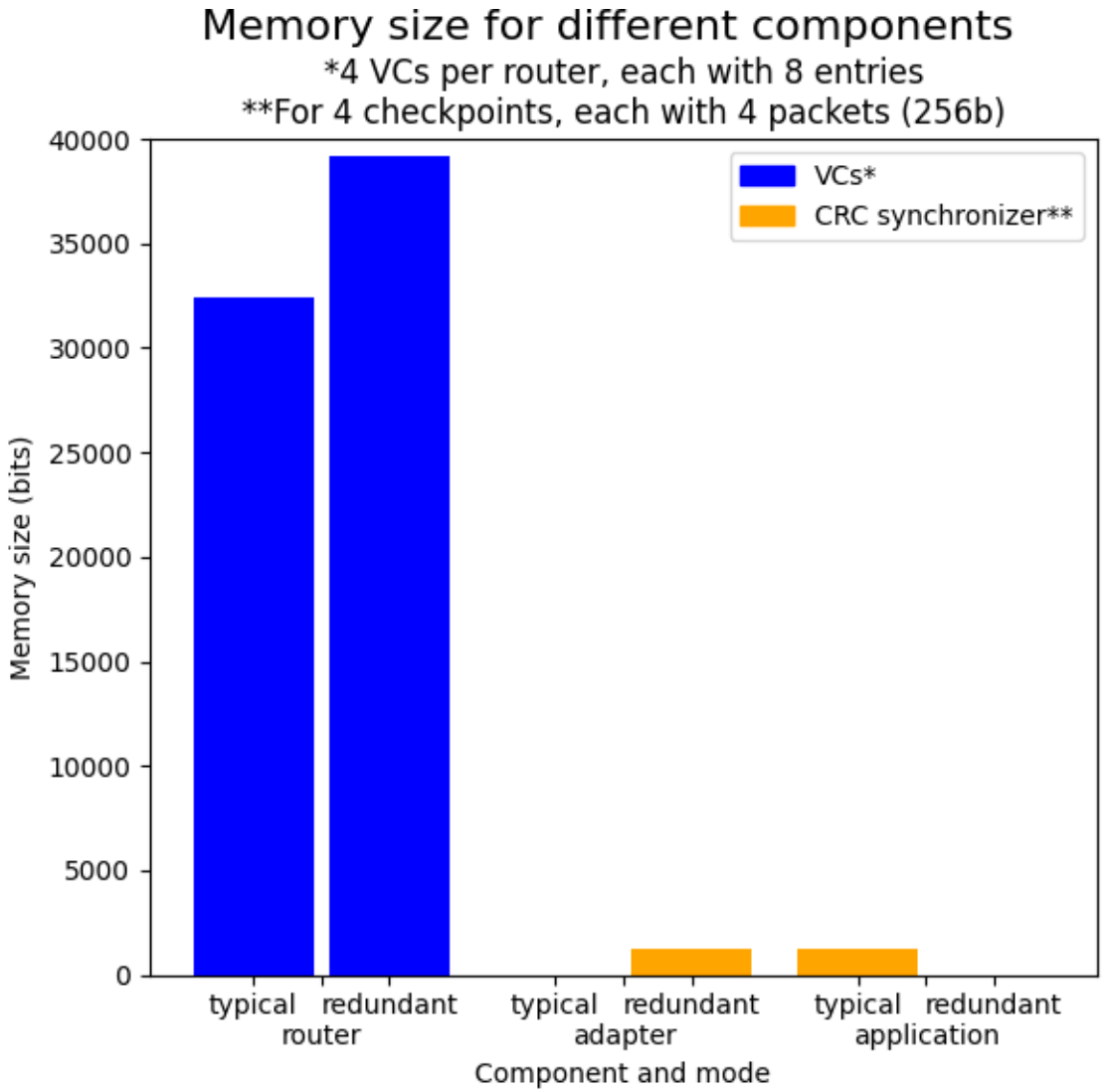


Results – memory

- Additional VC buffers
- Additional ports
  - Share data, …
  - Different output address

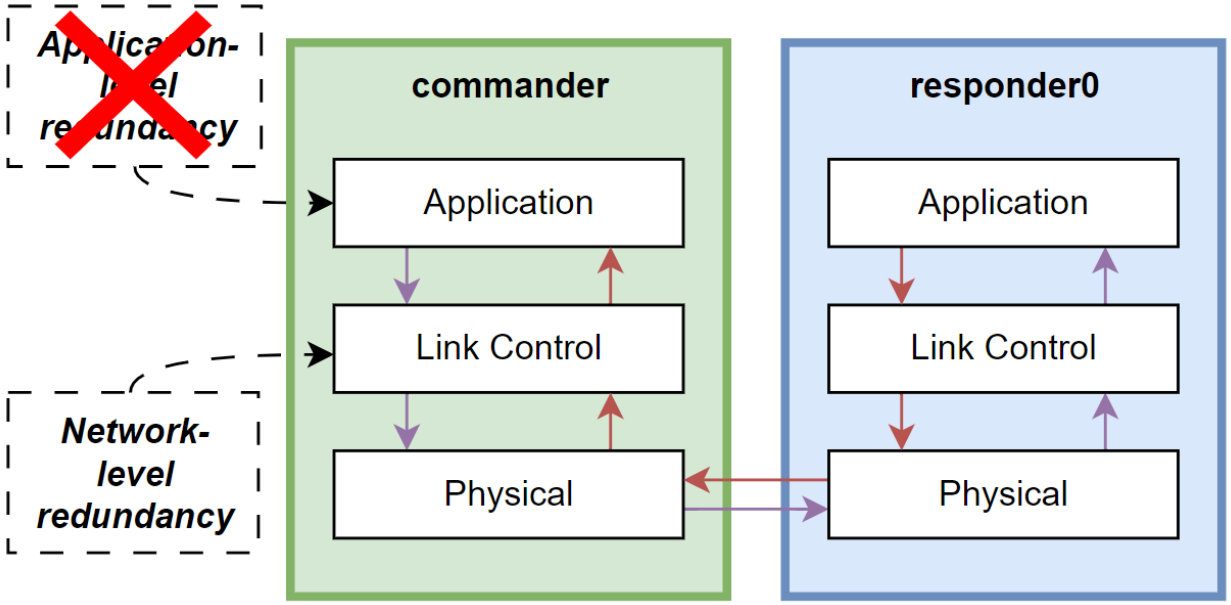
Per redundant module (i.e., x3)

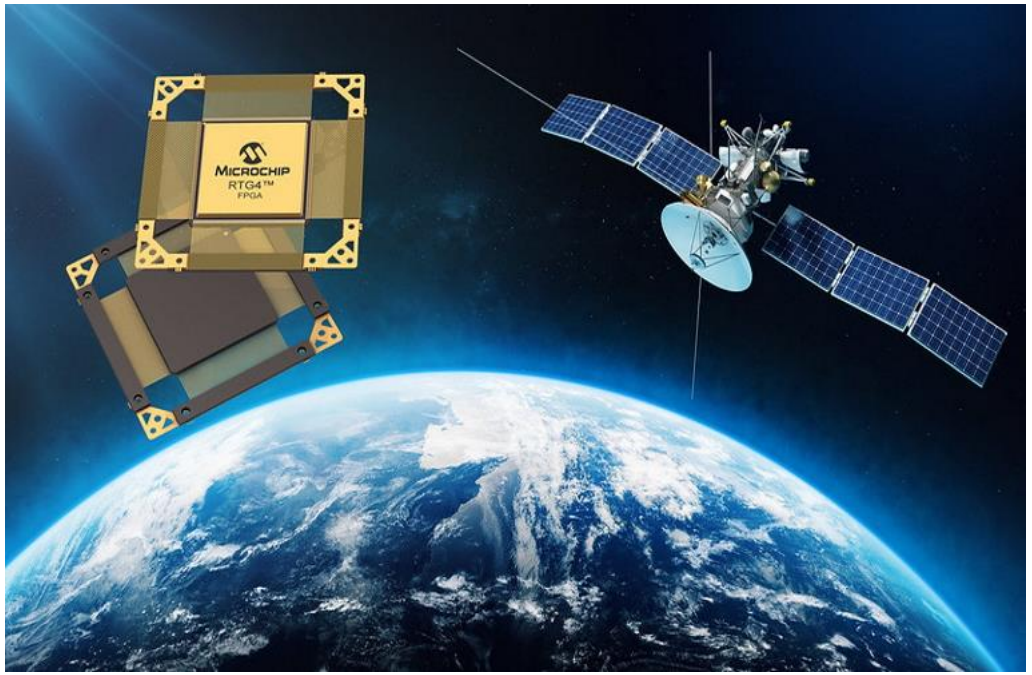




Conclusion

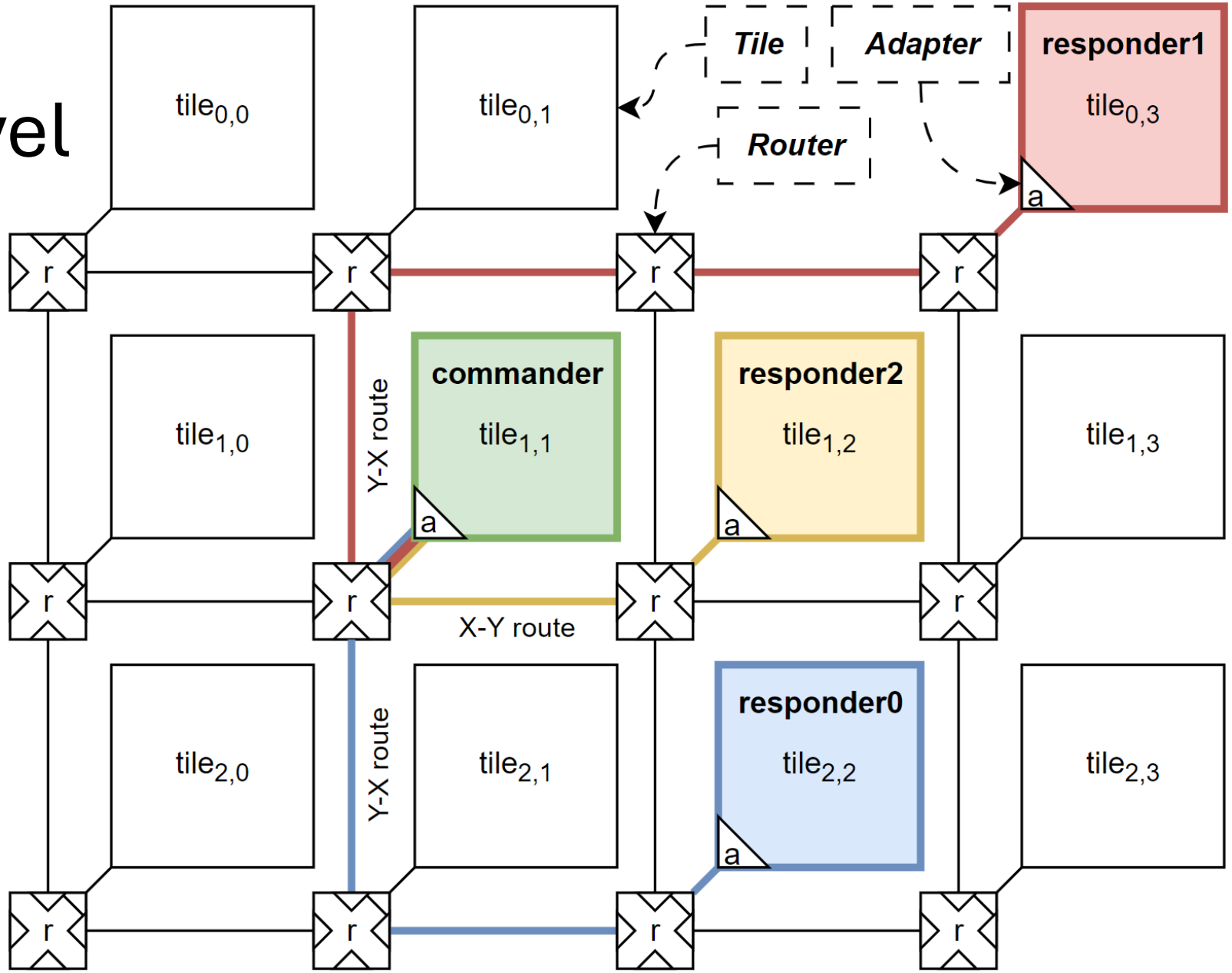
- Combination with other work





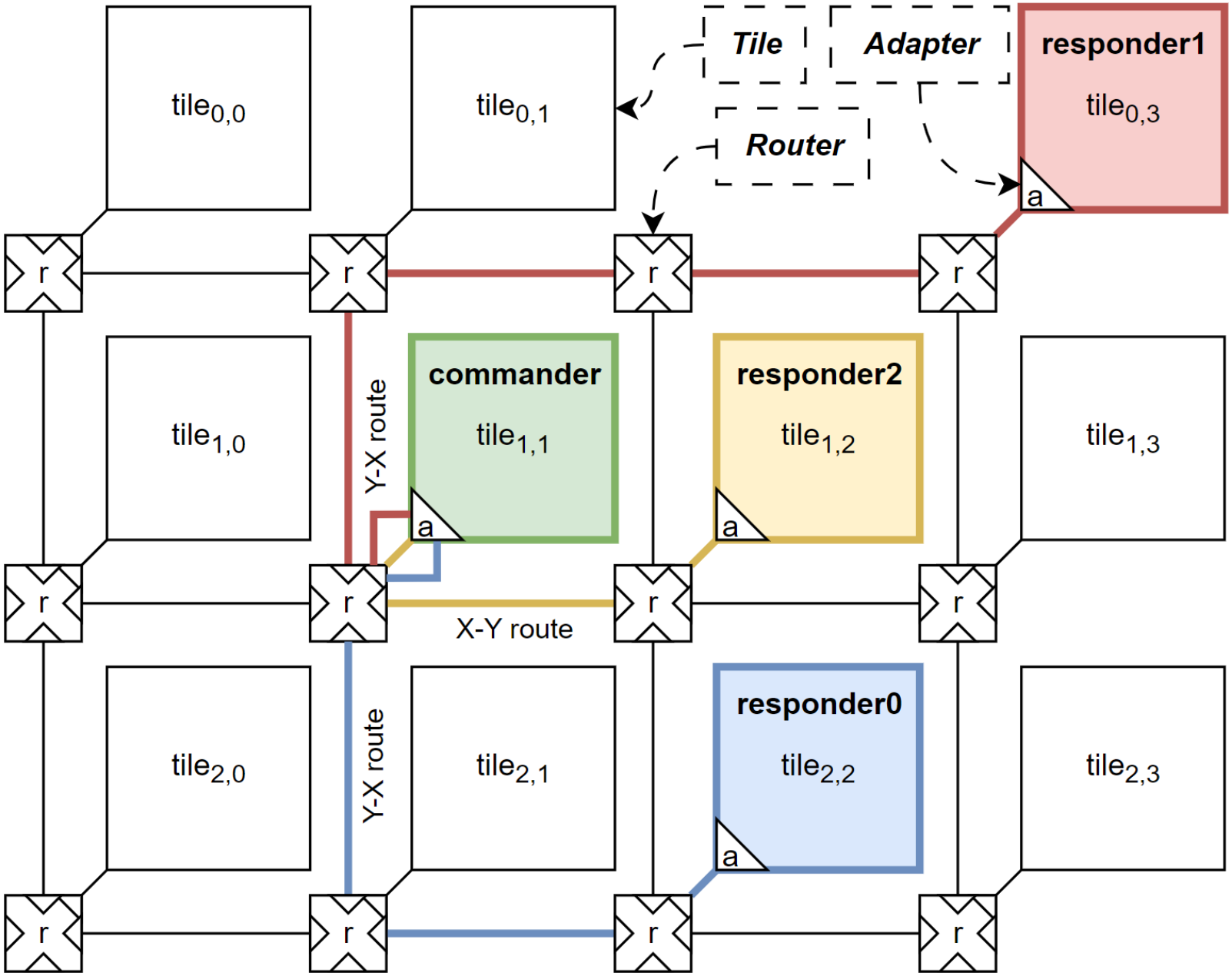
Application-level redundancy

- Separate packet for each destination



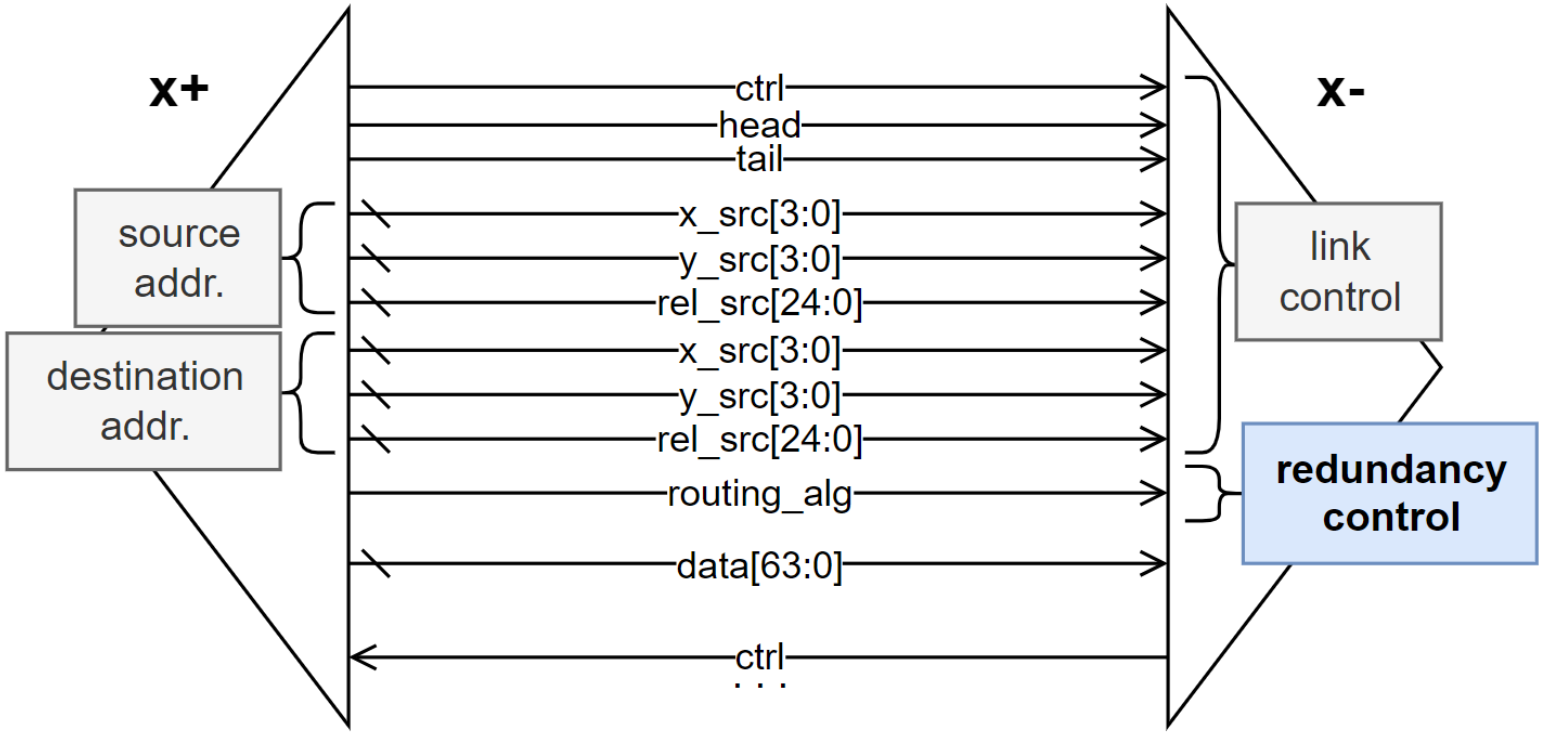
Solution

- Same packet copied



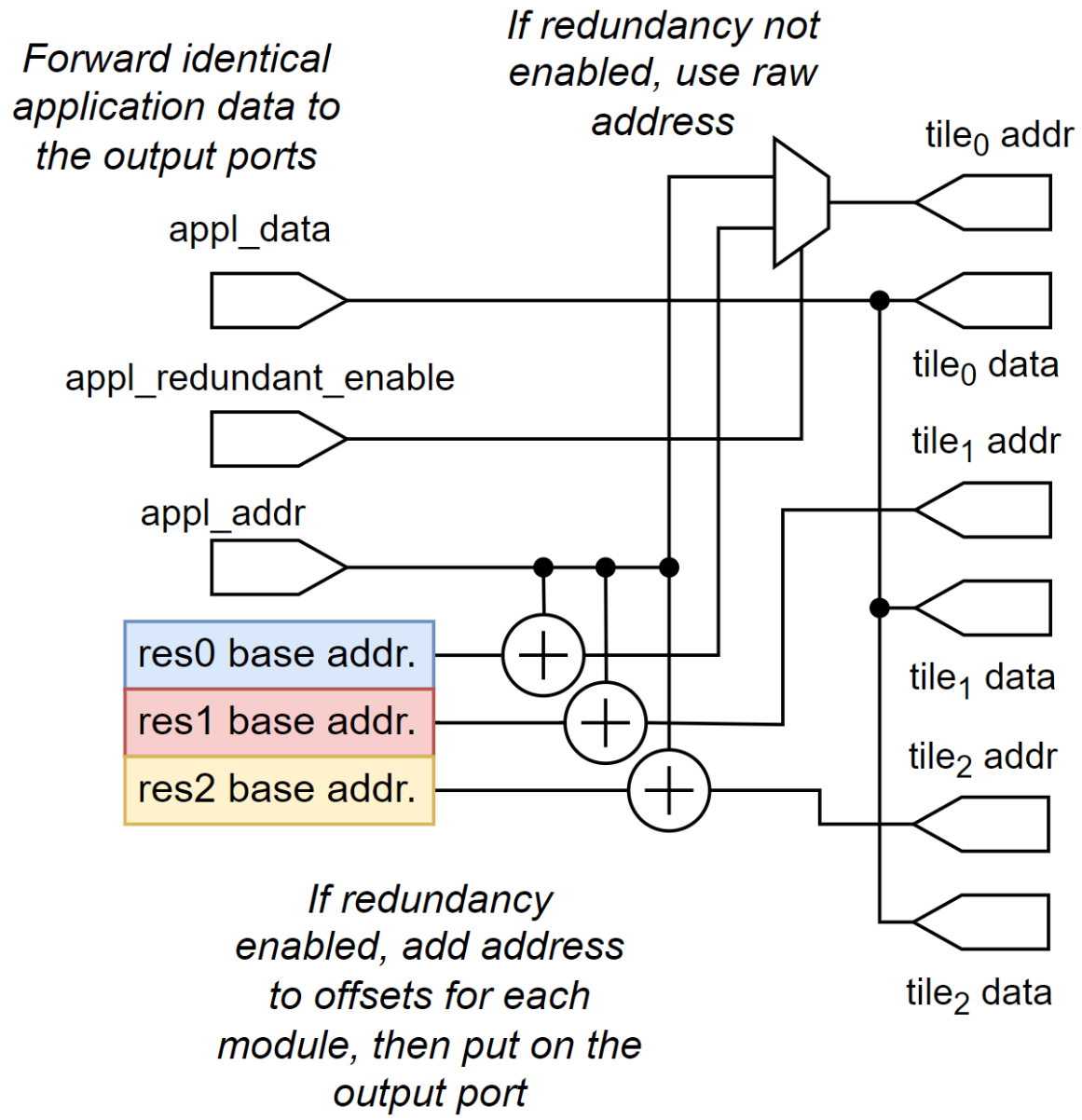
Solution

- Updated router interface



Solution

- Adapter control logic



Experimental Setup – fault-injection

- Define probability of fault per byte per time step