

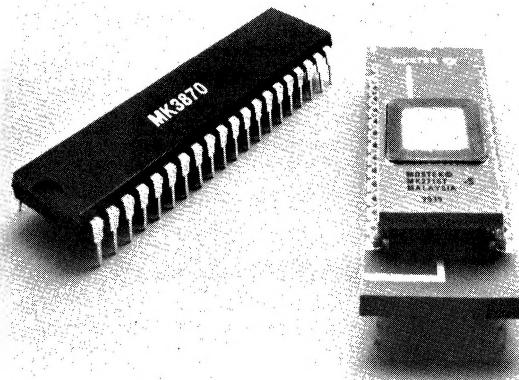
MOSTEK®

3870 SINGLE CHIP MICRO FAMILY

MK3870 and MK38P70

MK3870 FEATURES

- Available with 1K, 2K, 3K, or 4K bytes of mask programmable ROM memory
- 64 bytes scratchpad RAM
- Available with 64 bytes executable RAM
- 32 bits (4 ports) TTL compatible I/O
- Programmable binary timer
 - Interval timer mode
 - Pulse width measurement mode
 - Event counter mode
- External interrupt input
- Crystal, LC, RC, or external time base options
- Low power (275 mW typ.)
- Single +5 volt supply



MK38P70 FEATURES

- EPROM version of MK3870
- Piggyback PROM (P-PROM)™ package
- Accepts 24 pin or 28 pin EPROM memories
- Identical pinout as MK3870
- In-Socket emulation of MK3870

GENERAL DESCRIPTION

The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MK3870 can execute a set of more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK3870 features 1-4K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK3870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the

MK3870 PIN CONNECTIONS

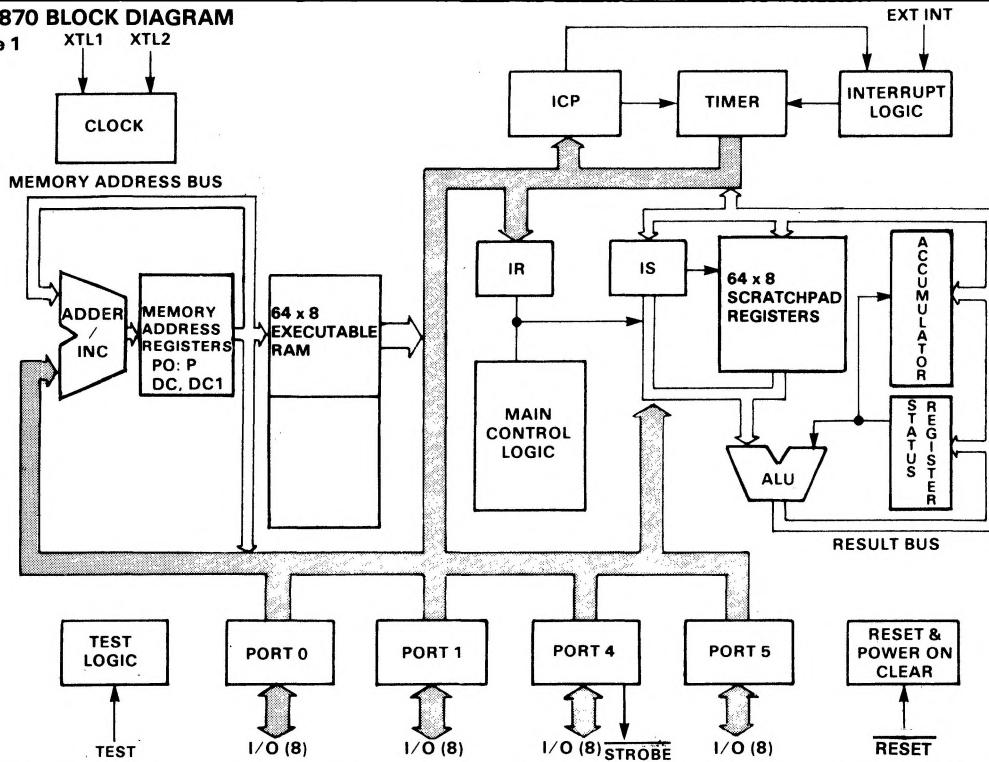
XTL1	1	40	V _{cc}
XTL2	2	39	RESET
P0.0	3	38	EXT INT
P0.1	4	37	PT0
P0.2	5	36	PT1
P0.3	6	35	PT2
STROBE	7	34	PT3
P4.0	8	33	P5.0
P4.1	9	32	P5.1
P4.2	10	31	P5.2
P4.3	11	30	P5.3
P4.4	12	29	P5.4
P4.5	13	28	P5.5
P4.6	14	27	P5.6
P4.7	15	26	P5.7
P0.7	16	25	PT7
P0.6	17	24	PT6
P0.5	18	23	PT5
P0.4	19	22	PT4
GND	20	21	TEST

MK38P70 PIN CONNECTIONS

XTL1	1	40	V _{cc}
XTL2	2	39	RESET
P0.0	3	38	EXT INT
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P0.3	6	35	PT2
STROBE	7	34	PT3
P4.0	8	33	P5.0
P4.1	9	32	P5.1
P4.2	10	31	P5.2
P4.3	11	30	P5.3
P4.4	12	29	P5.4
P4.5	13	28	P5.5
P4.6	14	27	P5.6
P4.7	15	26	P5.7
P0.7	16	25	PT7
P0.6	17	24	PT6
P0.5	18	23	PT5
P0.4	19	22	PT4
GND	20	21	TEST

MK3870 BLOCK DIAGRAM

Figure 1 XTL1 XTL2



event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK3870 and MK38P70: Crystal, LC, RC, or external clock. In addition, the user can specify either a $\pm 10\%$ power supply tolerance or a $\pm 5\%$ power supply tolerance.

The MK38P70 microcomputer is the PROM based version of the MK3870. It is called the piggyback PROM (P-PROM)TM because of its packaging concept. This concept allows a standard 24-pin or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P70 retains exactly the same pinout and architectural features as other members of the 3870 family. The MK38P70 is discussed in more detail in a later section.

FUNCTIONAL PIN DESCRIPTION

P0-0--P0-7, P1-0--P1-7, P4-0--P4-7, and P5-0--P5-7 are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

STROBE is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the P4-0--P4-7> pins during an output instruction.

RESET may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.

TEST is an input, used only in testing the MK3870. For normal circuit function this pin may be left unconnected, but

PIN NAME	DESCRIPTION	TYPE
P0-0 -- P0-7	I/O Port 0	Bidirectional
P1-0 -- P1-7	I/O Port 1	Bidirectional
P4-0 -- P4-7	I/O Port 4	Bidirectional
P5-0 -- P5-7	I/O Port 5	Bidirectional
STROBE	Ready Strobe	Output
EXT INT	External Interrupt	Input
RESET	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V _{CC} , GND	Power Supply Lines	Input

it is recommended that TEST be grounded.

V_{CC} is the power supply input (single +5v).

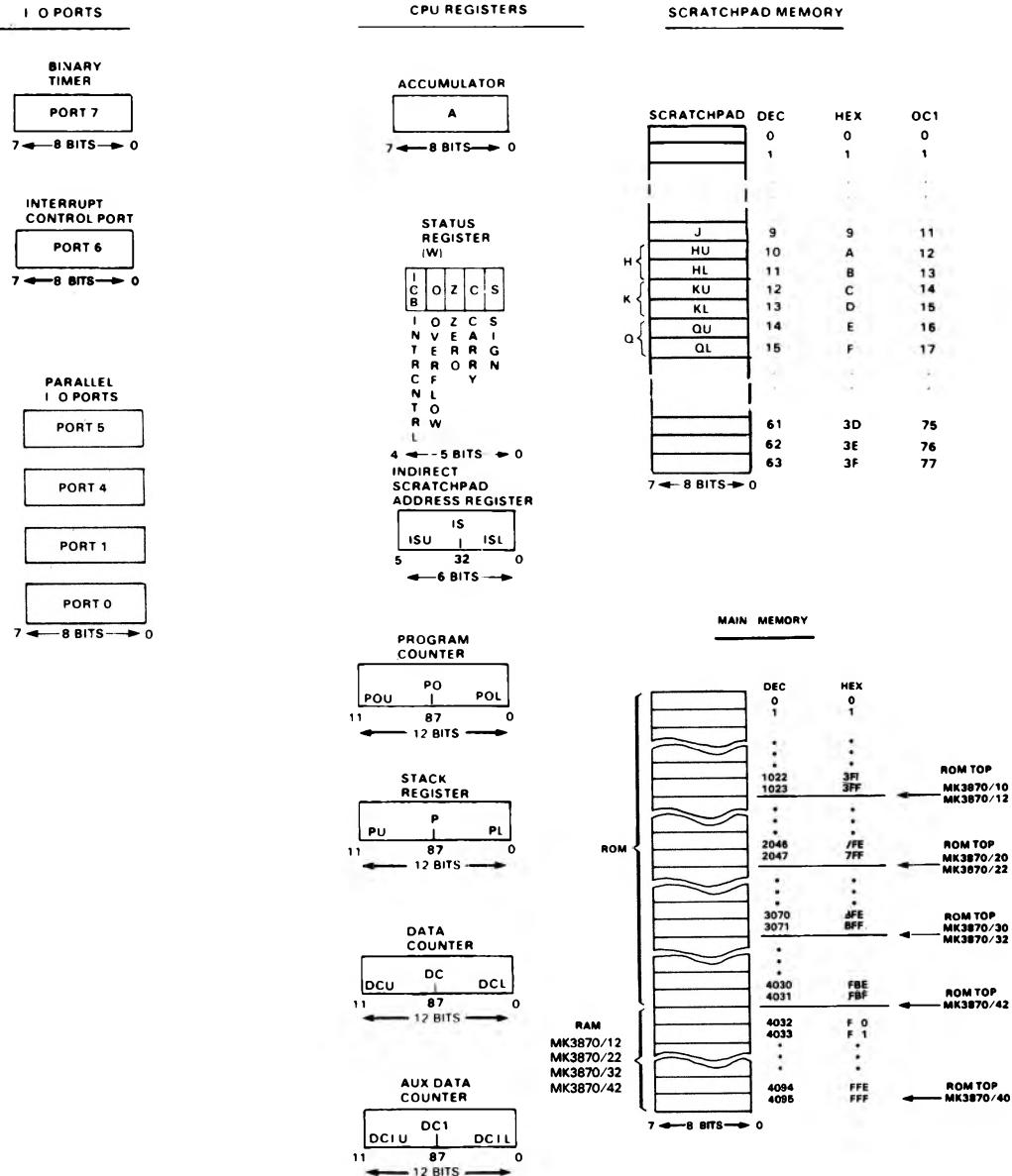
MK3870 ARCHITECTURE

The basic functional elements of the MK3870 are shown in Figure 1. A programming model is shown in Figure 2. The

architecture is common to all members of the 3870 family. All 3870 devices are instruction set compatible and differ only in amount and type of ROM, RAM, and I/O. The unique features of the MK3870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to all 3870 family devices.

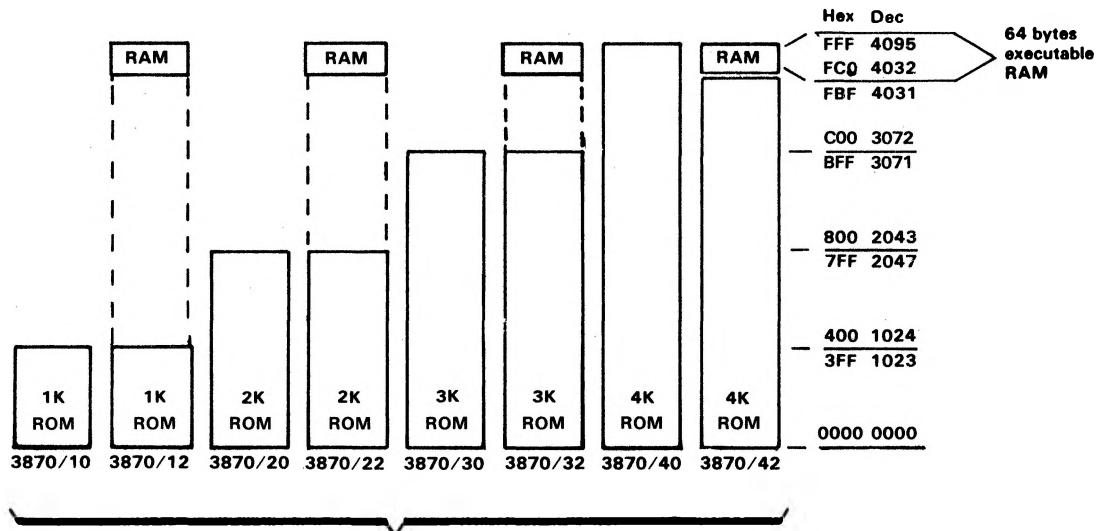
MK3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



**MK3870 MAIN MEMORY
SIZES AND TYPES BY SLASH NUMBERS**

Figure 3



All devices contain 64 bytes of scratchpad RAM.

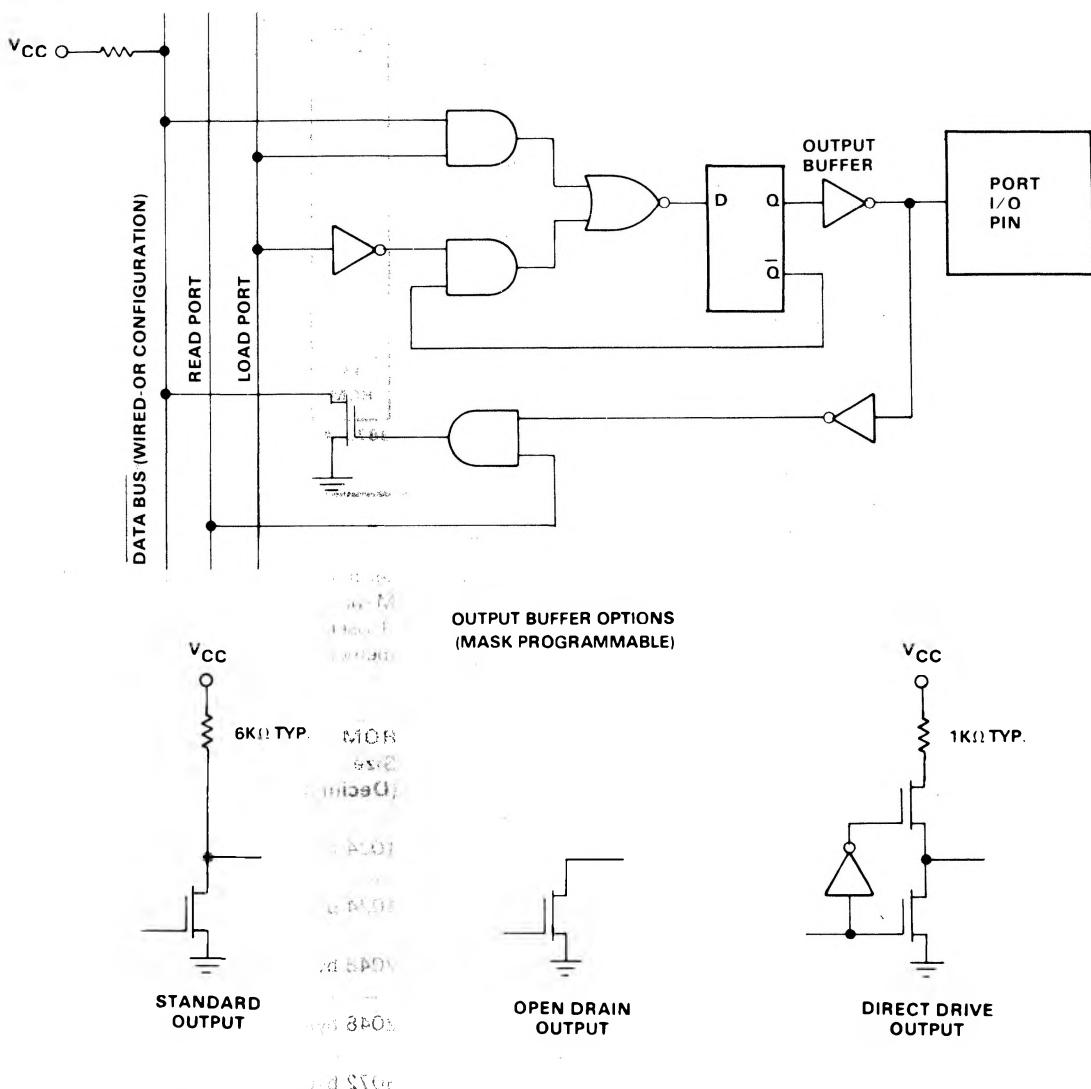
NOTE: Data derived from addressing any locations other than those within a part's specified ROM space or RAM space (if any) are not tested nor are the data guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK3870/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3870/12	64 bytes	12 bits	1024 bytes	64 bytes
MK3870/20*	64 bytes	12 bits	2048 bytes	0 bytes
MK3870/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3870/30	64 bytes	12 bits	3072 bytes	0 bytes
MK3870/32	64 bytes	12 bits	3072 bytes	64 bytes
MK3870/40	64 bytes	12 bits	4096 bytes	0 bytes
MK3870/42	64 bytes	12 bits	4032 bytes	64 bytes

*The MK3870/20 is equivalent to the original 3870 device in memory size; however, the original 3870 had an 11-bit Address Register. The original 3870 with 11-bit Address Register is available where required. Consult the section describing ROM Code Ordering Information for additional information.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT
BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The STROBE output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

RESET and EXT INT may have standard $6\text{ k}\Omega$ (typical) pull-up or may have no pull-up (mask programmable).

RESET and EXT INT do not have internal pull up on the MK38P70.

MK3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 3 shows the amounts of ROM and executable RAM for every available slash number in the MK3870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK3870 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and the DC address registers. The executable RAM may be addressed by all MK3870 instructions which address Main Memory. Additionally, the MK3870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe to Port 4 after completing the input operation.

MK38P70 GENERAL DESCRIPTION

The MK38P70 is the EPROM version of the MK3870. It retains an identical pinout with the MK3870, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P70 is housed in two packages which incorporate a 28-pin socket

located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P70 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P70 eliminates the need for emulator board products. In addition, several MK38P70s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3870s. The compact size of the MK38P70/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P70 can be used as the actual production device.

Most of the material which has been presented for the MK3870 in this document applies to the MK38P70. This includes the description of the pin configuration, architecture, programming model, and I/O ports. Additional information is presented in the following sections.

MK38P70 MAIN MEMORY

There are two basic versions of the MK38P70. These are the 97400 series and the 97500 series. The 97400 series parts have twelve bit address capability thus a total 4K memory map like the MK3870 ROM devices. The 97500 series has 16 bit address capability.

As can be seen from Figure 6, both the 97400 series and the 97500 series contain on-chip RAM in the upper portion of their memory maps and no on-chip ROM. Instead of on-chip ROM, address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package so that external memory devices (principally EPROMs) are addressed.

By using an external EPROM, the 38P70 may be used to emulate the 3870 ROM devices. The 97400 series can directly emulate the following devices.

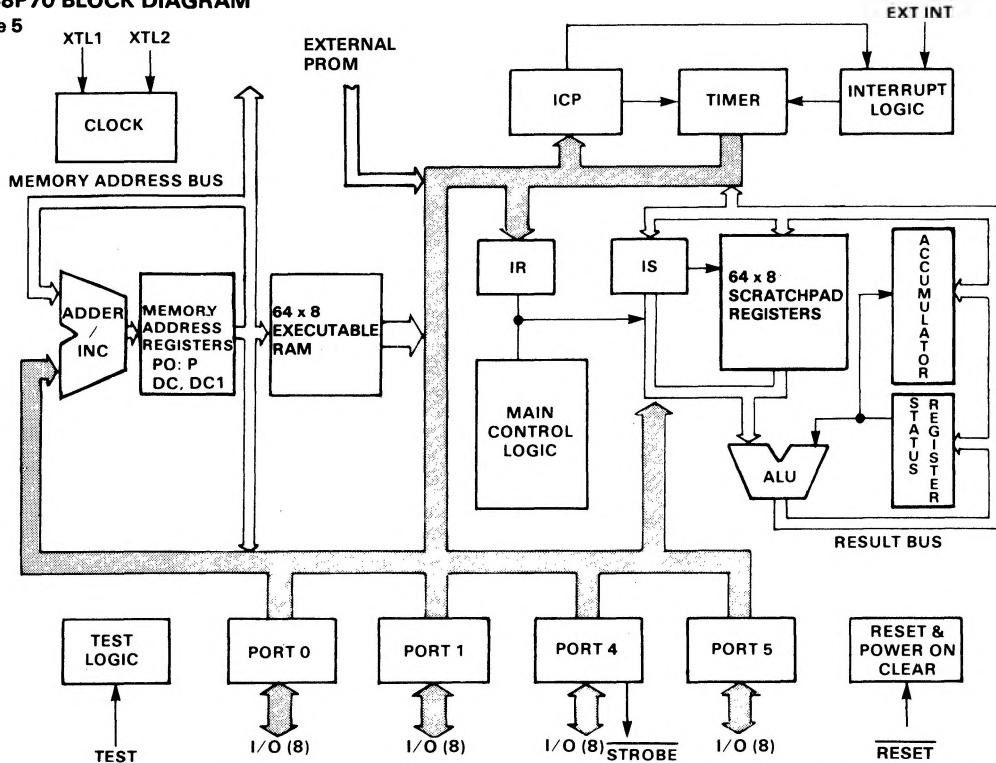
MK3870/10
MK3870/20
MK3870/22
MK3870/30
MK3870/42

The MK3870/40 cannot be emulated exactly by the 97400 series because the 97400 devices have the 64 bytes of RAM in the upper memory map while the 3870/40 provides ROM memory in this address space.

Besides the difference in the size of the address registers, 97500 series can also emulate many of the 3870 ROM devices. This difference in address capability should not cause any functional difference as long as normal programming practice is used. That is, as long as address roll-over or automatic truncation is not used. One such usage would be an end around branch (branching forward

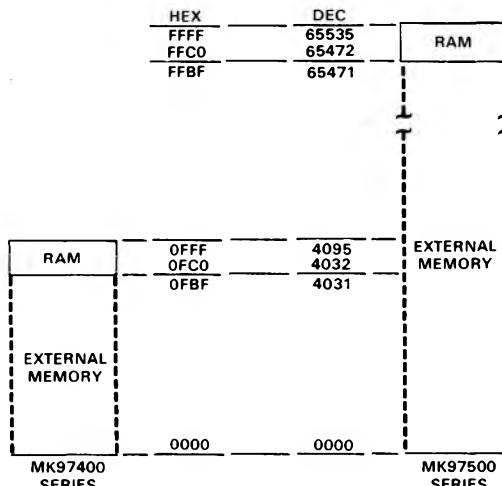
MK38P70 BLOCK DIAGRAM

Figure 5



MK38P70 MAIN MEMORY MAP

Figure 6



MK38P70 TYPE	SCRATCHPAD RAM SIZE (DECIMAL)	ADDRESS REGISTER SIZE	EXTERNALLY ADDRESSABLE MEMORY SIZE	INTERNAL EXECUTABLE RAM SIZE
97400 Series	64 bytes	12 bits	4032 bytes	64 bytes
97500 Series	64 bytes	16 bits	65472 bytes	64 bytes

MK38P70 devices have no internal ROM memory.

at upper memory to get to lower memory). Another case would be in using automatic truncation of data loaded into the 12 bit address registers on the ROM devices. For example, to access some particular location (03FF hex for example) via the data counter, one could load that address into DC using the DCI instruction. The instruction

DCI '73FF'

would cause 3FF to be loaded into the DC of the 3870 ROM device because the upper bits of the DC (bits 12-15) do not exist. If that instruction was followed by the LM instruction, the data stored at location 3FF would be obtained. The 97500 series devices would not truncate the 73FF address to 3FF. As previously stated, this type of programming is generally not done and thus the 97500 devices can be used to emulate the following devices directly.

MK3870/10
MK3870/20
MK3870/30
MK3870/40

The 97500 series can also be used to emulate the remainder of the 3870 devices as long as one accounts for the difference in the location of the RAM memory. In the 97500 devices, RAM is located at FFC0 through FFFF. While in 3870 devices this RAM (when it exists) is located at OFC0 through OFFF. When this minor difference is accounted for, the 97500 series will also emulate the following devices.

MK3870/22
MK3870/42

MK38P70 EPROM SOCKET

A 28 pin socket is located on top of the 40 pin package. When 24 pin memories are used, they are inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24 pin memory is lower justified in the 28 pin socket).

A 24 pin top socket was used so that the same package could be used for all 38P70 devices but could accommodate both 24 pin and 28 pin. Due to pin-out differences between various common memory devices, several different versions of the MK38P70 are provided with differing signals connected to particular pins on the 28 pin socket. Figure 7 shows the various options available.

MK38P70 I/O PORTS

For custom 3870 ROM codes, the user is given a bit by bit selection of I/O options on I/O ports 4 and 5. Additionally, the user has the option of selecting whether or not either RESET or EXT INT has an internal pull-up resistor. This flexibility allows about 172 million possible variations in I/O port and RESET and EXT INT configurations. Obviously, it is not practical to offer this variety in an "off the shelf" product

like the 38P70. Thus a few variations are offered which still give some flexibility to the designer. The available I/O options are also shown in Figure 7.

28 PIN SOCKET SIGNALS

The 40 package pins are the identical signals that are provided with the MK3870 ROM devices. In addition to these 40 inputs and outputs, various other signals are implemented on the 38P70 die which are available for connection to the top socket. Depending upon the particular version, some subset of these signals are connected to the 28 pin socket. These signals are described below.

A₀ - A₁₁ (97400 Series)

A₀ - A₁₅ (97500 Series)

These are the address buses. They are always outputs and a new address will appear on this bus during each machine cycle. Normally this is the address of op-codes or operands, but there are machine cycles wherein no op-code or operand is required by the CPU. During these cycles, an address is still provided but the data that may be read from that address is not used.

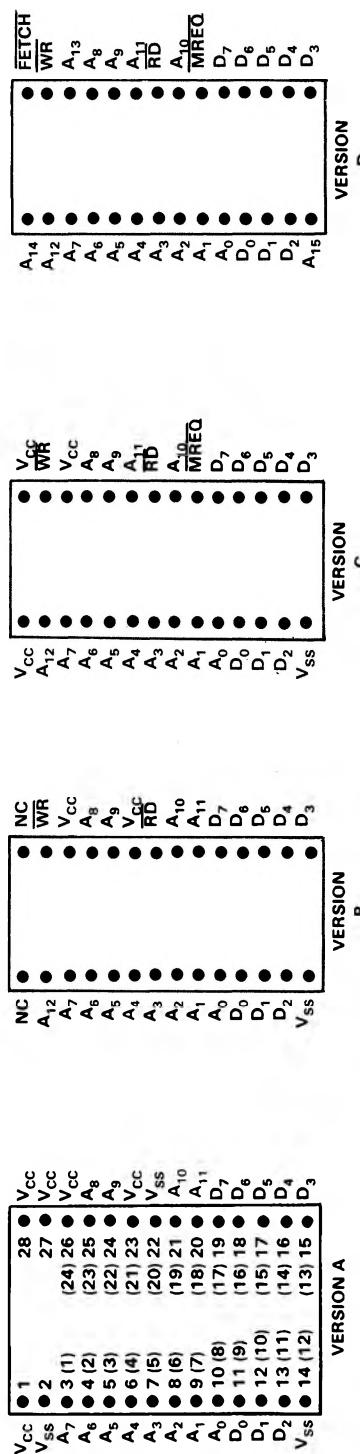
D₀ - D₇ (97400 and 97500 Series)

This is the bi-directional data bus for the external memory. Normally these lines are high impedance inputs. During op-code or operand reads, they receive data from the external memory and conduct it onto the internal 38P70 data bus. During those cycles wherein the operation is strictly internal to the 38P70, they remain hi-z inputs. Data may be presented to the 38P70 by an external memory device but it is not conducted onto the internal data bus. This includes machine cycles wherein op-codes or operands are read from the internal executable RAM. During the operand write machine cycle that occurs in the ST (store) instruction, they become push-pull outputs to conduct data to be written out to the external memory. However, if data is written to the internal executable RAM, this transaction is strictly internal and thus the data bus lines remain in their hi-z state. It, therefore, depends upon the address as to whether this bus becomes an active output bus or remains high impedance. If the address of the operand is not within the internal executable RAM space when a ST instruction is executed, D₀ - D₇ will become active outputs at the appropriate time, or else they will remain in the hi-z state. The 97400 devices do not provide a RD (read) control signal, nor is this signal provided on all versions of the 97500 series. Thus if a ST is executed with the operand address being that of external memory, that memory may access data and drive it onto D₀ - D₇ while the 38P70 is also driving data onto D₀ - D₇ and a bus conflict will result. This condition should be avoided; thus the user should note whether or not his external memory will drive D₀ - D₇ in this event. If it will drive D₀ - D₇, an ST with that operand address should be avoided. In general, one would not normally execute a write to a memory location where there is ROM or EPROM memory instead of RAM. However, some 3870 users have

MK38P70 VERSIONS

Figure 7

DEVICE	PORT 4 I/O TYPE	PORT 5 I/O TYPE	SUPPORTS THESE MEMORY DEVICES	TOP 28 PIN VERSION
MK97400	TTL	TTL	2716, 2516, 2532, 2758 MK3400 ROM	A
MK97410	Open Drain	Open Drain	2716, 2516, 2532, 2758 MK3400 ROM	A
MK97500	TTL	Open Drain	2716, 2516, 2532, 2758 MK3400 ROM	B
MK97501	TTL	Open Drain	2764, 2732, MK37000 ROM MK3400 ROM	C
MK97503	TTL	Open Drain	Use connector from 28 pin socket to memory bus	D



found the ST instruction useful even in devices like the 3870/20 which have no executable RAM. In this case it causes the data counter to increment (to perhaps totalize some event) but otherwise does nothing as one cannot write the internal ROM. No internal conflicts will occur if one attempts to write a 3870 ROM location. Most 97500 versions place a \overline{RD} (read, active low) signal on the top socket pin which matches the \overline{OE} (output enable, active low) input on most memories. Since \overline{RD} will remain high during an operand write, the external memory would not have its data outputs enabled and no conflict will occur.

MREQ (97500 Series Only)

This is an active low output which occurs during each machine cycle. It goes high at the start of each cycle then goes low for the remainder of the cycle.

\overline{RD} (97500 Series Only)

This is the active low read output which goes high at the start of each cycle then goes low if data (op-codes or operands) are to be read from external memory. During cycles wherein a strictly internal operation occurs, \overline{RD} will

remain high. It will also remain high during an operand write cycle.

\overline{WR} (97500 Series Only)

This is the active low write control output. It is normally high but will go low then return high during an operand write if the address is not that of internal executable RAM.

FETCH (97500 Series Only)

This is the active low fetch status signal which signals that an op-code fetch occurred during that cycle. It is generated for use of the 97500 as a development system component.

It will go low during all op-code fetches whether from internal or external memory.

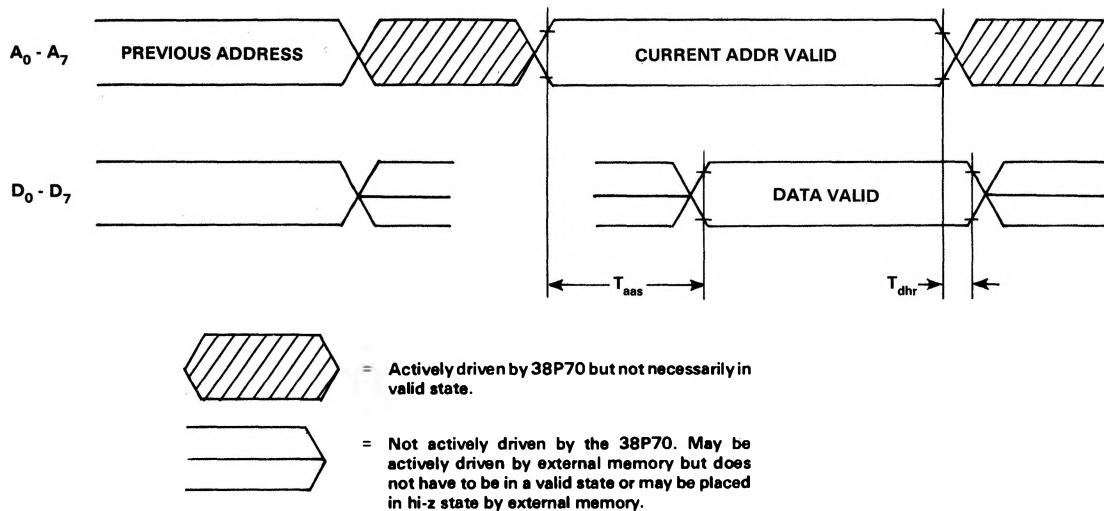
38P70 EXTERNAL MEMORY TIMING

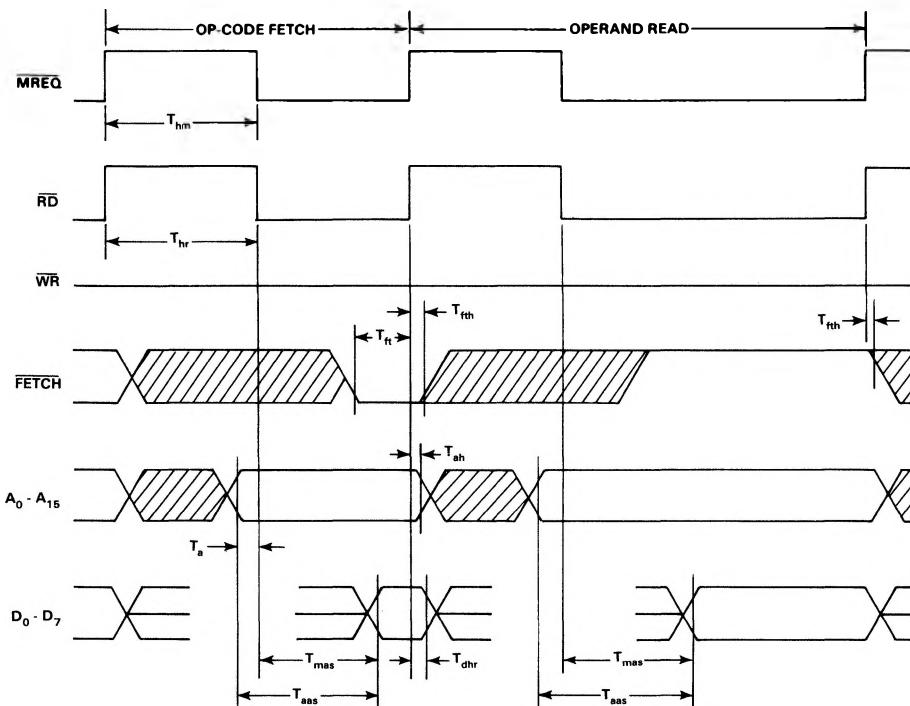
The following Figures show the relative waveforms for the signals used to interface with external memory. The timing parameters are labeled. Their values are given in the A.C. Characteristics section of the Electrical Specifications.

97400 SERIES TIMING

Read Cycle

Figure 8

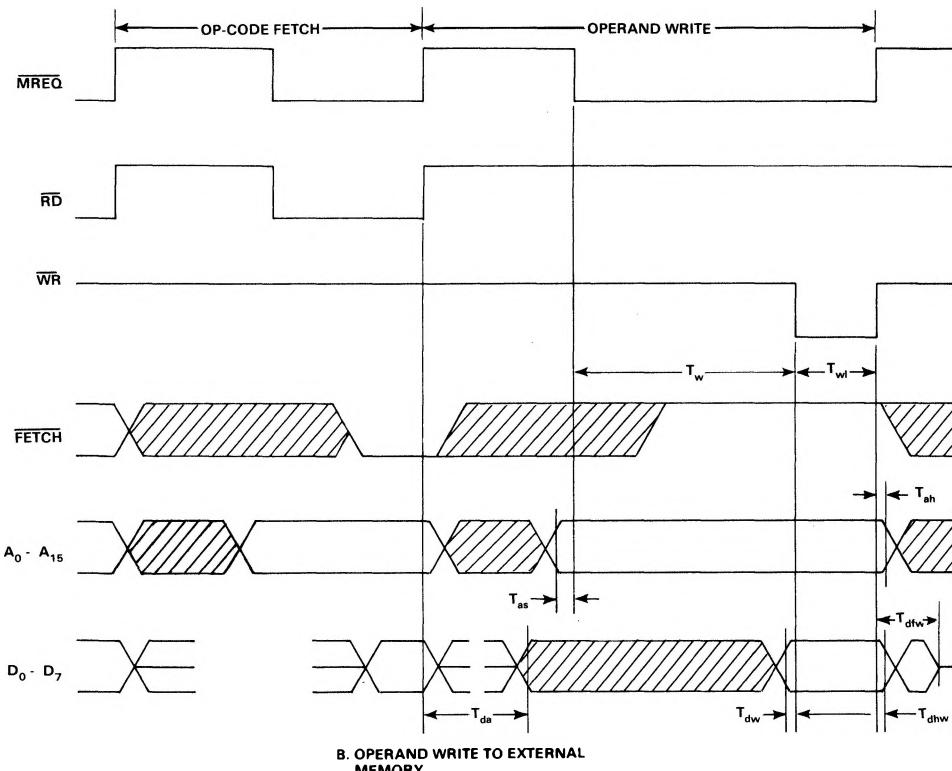


97500 SERIES TIMING**Figure 9**

A. OP CODE AND OPERAND READ
FROM EXTERNAL MEMORY

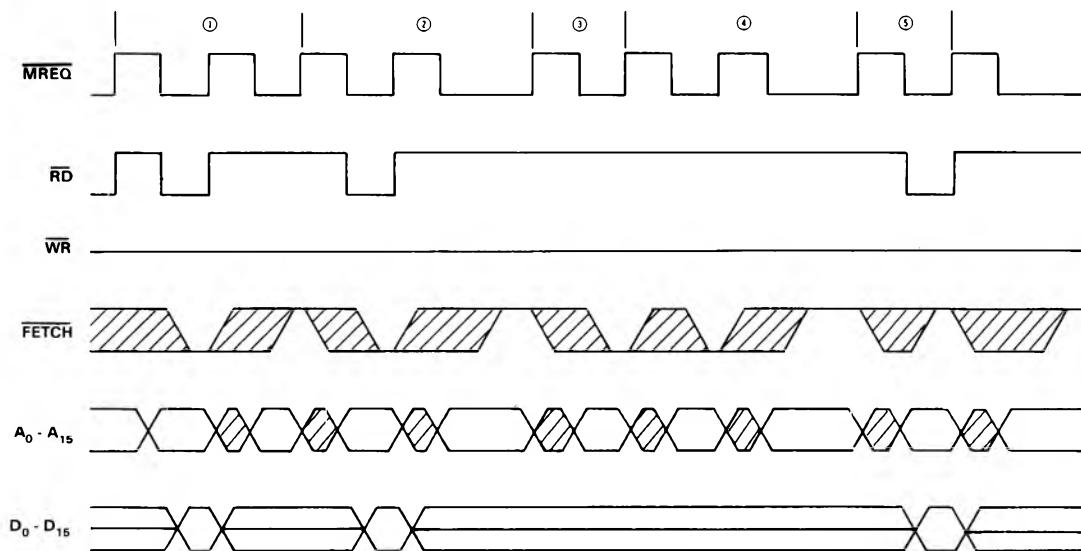
97500 SERIES TIMING (Continued)

Figure 9



97500 SERIES TIMING (Continued)

Figure 9



C. EXAMPLES OF VARIOUS CYCLES

- ① Op-code fetch from external memory followed by an internal cycle (short cycle).
- ② Op-code fetch from external memory followed by an internal cycle (long cycle) such as an operand read or write internal executable RAM.
- ③ Op-code fetch from internal executable RAM.
- ④ Op-code fetch from internal executable RAM followed by a internal cycle (long cycle) such as an operand read or write of internal executable RAM.
- ⑤ First cycle of an interrupt acknowledge. Had an interrupt not occurred, this would have been an op-code fetch. If it would have been an external op-code fetch, RD will still go low but FETCH will not indicate a fetch cycle. Externally this would appear to be an operand read except that it occurs in a short cycle and all real operand reads occur in a long cycle.

3870 TIME BASE OPTIONS

The 3870 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3870 may originate from one of four sources:

- 1) Crystal
- 2) LC Network
- 3) RC Network
- 4) External Clock

The type of network which is to be used with the mask ROM MK3870 must be specified at the time when mask ROM devices are ordered. However, the MK38P70 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproduction from system to system is unsurpassed. The 3870 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 11 lists the required crystal parameters for use with the 3870. The Crystal Mode time base configuration is shown in Figure 10.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3870, if a single crystal is to provide the time base for more than just a single 3870.

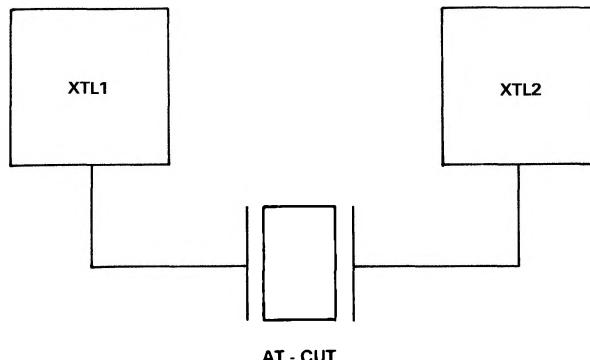
While a ceramic resonator may work with the 3870 crystal oscillator, it was designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3870 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 12. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C_{external} , the internal capacitance of the 3870, C_{XTL} , and the stray

CRYSTAL MODE CONNECTION

Figure 10



CRYSTAL PARAMETERS

Figure 11

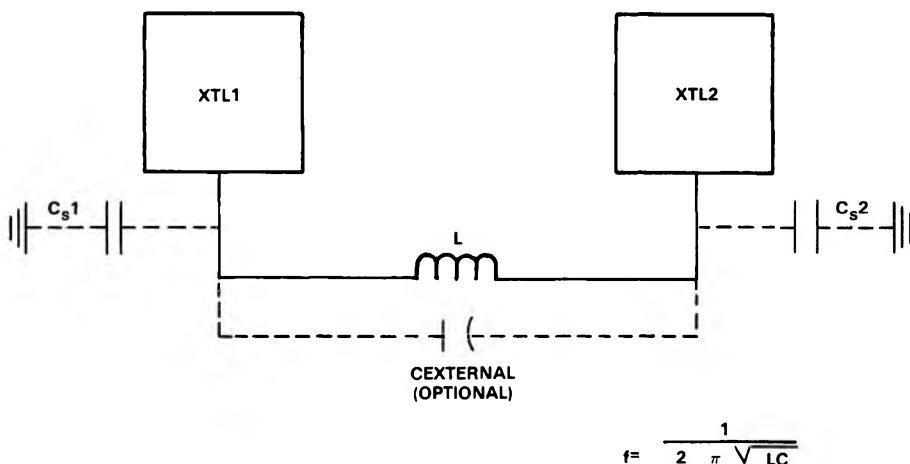
- a) Parallel resonance, fundamental mode AT-Cut
- b) Shunt capacitance (C_0) = 7 pf max.
- c) Series resistance (R_s) = See table
- d) Holder = See table below.

Frequency	Series Resistance	Holder
$f = 2-2.7 \text{ MHz}$	$R_s = 300 \text{ ohms max}$	HC-6 HC-33
$f = 2.8-4 \text{ MHz}$	$R_s = 150 \text{ ohms max}$	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

LC MODE CONNECTION

Figure 12



capacitances, C_{S1} and C_{S2} . C_{XTL} is the capacitance looking into the internal two port network at XTL1 and XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. $C_{EXTERNAL}$ should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3870 at XTL1 and XTL2 and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3870.

RC CLOCK CONFIGURATION

The time base for the 3870 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 13. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy, Mostek recommends the use of the

Crystal or LC time base configuration. Figure 14 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3870 devices are also shown in the diagram.

The designer must select the RC product such that a frequency of less than 2 MHz is not possible, taking into account the maximum possible RC product and using the minimum curve shown in Figure 14 below. Also, the RC product must not allow a frequency of more than 4 MHz, taking into account the minimum possible R and C and using the Maximum curve shown below. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit owing to switching speed and level at constant temperature and $V_{CC} = +$ or -5 percent.

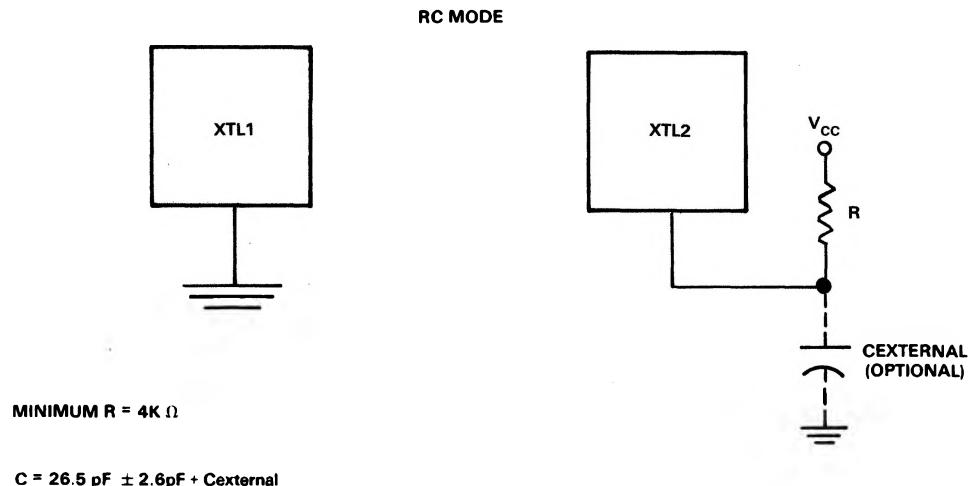
Frequency variation due to V_{CC} with all other parameters constant with respect to $+5V = +7$ percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

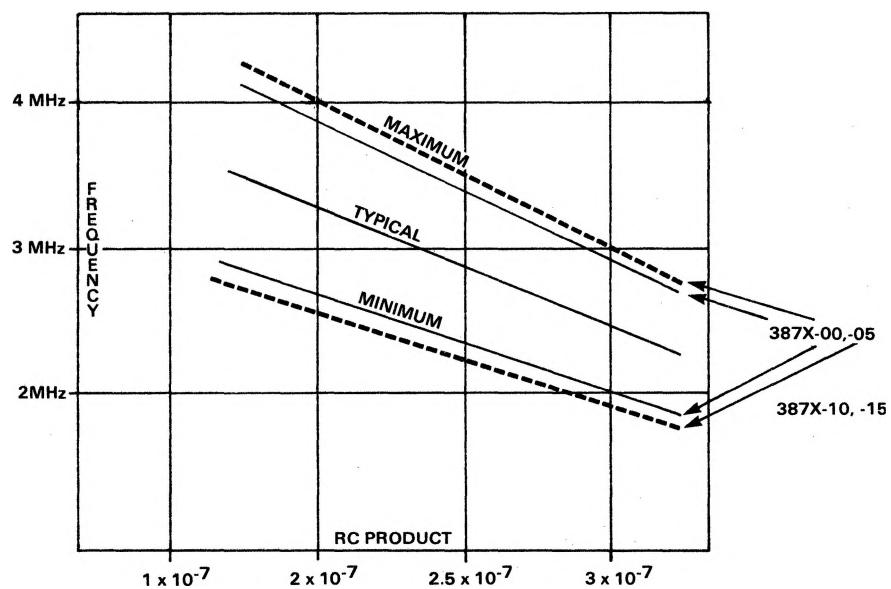
RC MODE CONNECTION

Figure 13



FREQUENCY VS. RC

Figure 14



Variations in frequency due to variations in RC components may be calculated as follows:

$$\text{Maximum RC} = (\text{R max})(\text{C external max} + \text{C}_{\text{XTL}} \text{ max})$$

$$\text{Minimum RC} = (\text{R min})(\text{C external min} + \text{C}_{\text{XTL}} \text{ min})$$

$$\text{Typical RC} = (\text{R typ})(\text{C external typ} +$$

$$\frac{\{\text{C}_{\text{XTL}} \text{ max} + \text{C}_{\text{XTL}} \text{ min}\}}{2}$$

$$\text{Positive Freq. Variation} = \text{RC typical} - \text{RC minimum} \\ \text{RC typical}$$

$$\text{Negative Freq. Variation} = \text{RC maximum} - \text{RC typical} \\ \text{due to RC Components} \quad \quad \quad \text{RC typical}$$

$$= -18 \text{ percent minus negative} \\ \text{frequency variation due to} \\ \text{RC components}$$

$$= -21 \text{ percent minus} \\ \text{negative frequency} \\ \text{variation due to RC} \\ \text{components}$$

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC} , 25 C

$$387X-00, -05$$

$$= +13 \text{ percent}$$

$$387X-10, -15$$

$$= +16 \text{ percent}$$

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 15. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3870 Family device data sheet for input capacitance.

Total frequency variation due to all factors:

$$387X-00, -05$$

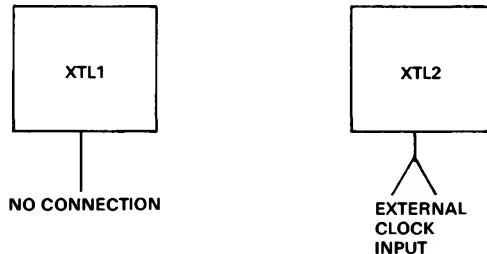
= +18 percent plus positive
frequency variation due
to RC components

$$387X-10, -15$$

= +21 percent plus positive
frequency variation due
to RC components

EXTERNAL MODE CONNECTION

Figure 15



ELECTRICAL SPECIFICATIONS
MK3870, MK38P70

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V _{CC}	Operating Temperature T _A
-00	+5V ± 10%	0°C - 70°C
-05	+5V ± 5%	0°C - 70°C
-10	+5V ± 10%	-40°C - +85°C
-15	+5V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature.....	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05		-10,-15		UNIT	NOTES
			MIN	MAX	MIN	MAX		
XTL1 XTL2	t ₀	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	t _{ex(H)} t _{ex(L)}	External clock pulse width high External clock pulse width low	90 100	400 400	100 110	390 390	ns ns	
Φ	t _Φ	Internal Φ clock	2t ₀		2t ₀			
WRITE	t _w	Internal WRITE Clock period	4t _Φ 6t _Φ		4t _Φ 6t _Φ			Short Cycle Long Cycle
I/O	t _{dI/O}	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	t _{slI/O}	Input setup time to internal WRITE clock	1000		1200		ns	
STROBE	t _{I/O-s}	Output valid to STROBE delay	3t _Φ -1000	3t _Φ +250	3t _Φ -1200	3t _Φ +300	ns	I/O load = 50pF + 1 TTL load
	t _{sL}	STROBE low time	8t _Φ -250	12t _Φ +250	8t _Φ -300	12t _Φ +300	ns	STROBE load = 50pF + 3 TTL loads
RESET	t _{RH}	RESET hold time, low	6t _Φ +750		6t _Φ +1000		ns	
	t _{RPOC}	RESET hold time, low for power clear	power supply rise time - 0.1		power supply rise time + 1.5		ms	
EXT INT	t _{EH}	EXT INT hold time in active and inactive state	6t _Φ +750		6t _Φ +1000		ns	To trigger interrupt
			2t _Φ		2t _Φ		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P70 Signals brought to top 28 pin socket.

T_A , V_{CC} within specified operating range.

I/O Power Dissipation ≤ 100 mW (Note 2)

97400 Series (See Note 3)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}	External memory required access time from A_0 - A_{11} stable	3t Φ -850		3t Φ -850		ns	$C_L A_0$ - $A_{11} = 50$ pF

97500 Series (See Note 3)

SIGNAL	SYMBOL	PARAMETER	-00, -05		-10, -15		UNITS	CONDITION
			MIN	MAX	MIN	MAX		
MREQ	T_{hm}	MREQ high time	2t Φ -100		2t Φ -100		ns	Load = 50 pF + 1 TTL load
RD	T_{hr}	RD high time	2t Φ -100		2t Φ -100		ns	Load = 50 pF + 1 TTL load
WR	T_w	WR low from MREQ low	3t Φ -200	3t Φ +100	3t Φ -200	3t Φ +100	ns	Load = 50 pF + 1 TTL load
	T_{wl}	WR low time	t Φ -100	t Φ +100	t Φ -100	t Φ +100	ns	
FETCH	T_{ft}	FETCH stable prior to rising MREQ	650	650	650	650	ns	Load = 50 pF + 1 TTL Load
	T_{fh}	FETCH hold time after MREQ high	20		20		ns	Load = 20 pF
A_0 - A_{15}	T_a	Address stable prior to RD or MREQ falling	t Φ -400		t Φ -400		ns	Load = 50 pF + 1 TTL load
	T_{ah}	Address hold time after MREQ, RD, or WR high	15		15		ns	Load = 20 pF
D ₀ - D ₇	T_{aas}	External memory required access time from	3t Φ -850		3t Φ -850		ns	
	T_{mas}	External memory required access time from MREQ or RD low	2t Φ -450		2t Φ -450		ns	
	T_{dhr}	Required data hold time after MREQ rising	0		0		ns	
	T_{da}	Data bus active after MREQ or RD high	t Φ		t Φ			
	T_{dw}	Data stable prior to WR falling	5t Φ -2250		5t Φ -2250		ns	Load = 50 pF + 1 TTL load
	T_{dhr}	Data hold after WR high	15		15		ns	Load = 20 pF
	T_{dfw}	Data bus delay to float after MREQ rising		200		200	ns	

CAPACITANCE $T_A = 25^\circ C$

All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS T_A, V_{CC} within specified operating rangeI/O power dissipation ≤ 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/10 Outputs Open
			94		125	mA	MK3870/12 Outputs Open
			85		110	mA	MK3870/20 Outputs Open
			94		125	mA	MK3870/22 Outputs Open
			100		130	mA	MK3870/30 Outputs Open
			100		130	mA	MK3870/32 Outputs Open
			100		130	mA	MK3870/40 Outputs Open
			100		130	mA	MK3870/42 Outputs Open
			125		150	mA	MK38P70/X2 No EPROM, Outputs Open

DC CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
P_D	Power Dissipation		400		525	mW	MK3870/10 Outputs Open
			440		575	mW	MK3870/12 Outputs Open
			400		525	mW	MK3870/20 Outputs Open
			440		575	mW	MK3870/22 Outputs Open
			475		620	mW	MK3870/30 Outputs Open
			475		620	mW	MK3870/32 Outputs Open
			475		620	mW	MK3870/40 Outputs Open
			475		620	mW	MK3870/42 Outputs Open
			600		750	mW	MK38P70/X2 No EPROM, Outputs Open

DC CHARACTERISTICS (cont.)

 TA, V_{CC} within specified operating range, I/O power dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V _{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V _{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I _{IHEX}	External Clock input high current		100		130	μA	V _{IHEX} =V _{CC}
I _{ILEX}	External Clock input low current		-100		-130	μA	V _{ILEX} =V _{SS}
V _{IHI/O}	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V _{IHR}	Input high level, <u>RESET</u>	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V _{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V _{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I _{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	V _{IN} =0.4V
I _L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	V _{IN} =13.2V V _{IN} =0.0V
I _{OH}	Output high current pins with standard pull-up resistor	-100		-89		μA	V _{OH} =2.4V
		-30		-25		μA	V _{OH} =3.9V
I _{OHDD}	Output high current, direct drive pins	-100 -1.5		-80 -1.3		μA mA mA	V _{OH} =2.4V V _{OH} =1.5V V _{OH} =0.7V
		-8.5		-8.5			
I _{OHS}	<u>STROBE</u> Output High current	-300		-270		μA	V _{OH} = 2.4V
I _{OL}	Output low current	1.8		1.65		mA	V _{OL} =0.4V
I _{OLS}	<u>STROBE</u> Output Low current	5.0		4.5		mA	V _{OL} =0.4V

DC CHARACTERISTICS FOR MK38P70

Signals brought to top 25 pin socket

T_A, V_{CC} within specified range

I/O Power Dissipation ≤ 100 mW (Note 2)

97400, 97500 Series

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
V_{IH}	Input high level ($D_0 - D_7$)	2.0	$V_{CC} + .3$	2.1	$V_{CC} + .3$	V	$D_0 - D_7$ in Hi-z input mode
	Input low level ($D_0 - D_7$)	$V_{SS} -.3$.8	$V_{SS} -.3$.7	V	
						μA	
V_{OH}	Output high level (all outputs and $D_0 - D_7$ in output mode)	2.4		2.4		V	
V_{OL}	Output low level (all outputs and $D_0 - D_7$ in output mode)		.4		.4	V	
I_{OH}	Output source current (all outputs and $D_0 - D_7$ in output mode)	-100		-90		μA	$V_{OH} = 2.4$ V
I_{OL}	Output sink current (all outputs and $D_0 - D_7$ in output mode)	1.8		1.65		mA	$V_{OL} = .4$ V
R_{CC}	Package resistance from device pin 40 to top socket V_{CC} pin(s)					Ω	Pin 28, 27, or 26 when V_{CC}
						Ω	Pin 1 if V_{CC}
						Ω	Pin 23 if V_{CC}
R_{SS}	Package resistance from device pin 20 to top socket V_{SS} pin(s)					Ω	Pin 14 when V_{SS}
						Ω	Pin 2 or 22 when V_{SS}
I_{CC}	Supply current available from top socket V_{CC} pin(s)		-185		-185	mA	Σ pin 28, 27, 26 when V_{CC}
			-20		-20	mA	Pin 1 if V_{CC}
			-10		-10	mA	Pin 23 if V_{CC}
I_{SS}	Supply current available from top socket V_{SS} pin(s)		190		190	mA	Pin 14 if V_{SS}
			2		2	mA	Pin 2 if V_{SS}
			2		2	mA	Pin 22 if V_{SS}

NOTES:

- RESET and EXT INT have internal Schmitt triggers giving minimum .2 V hysteresis.
 - Power dissipation for I/O pins is calculated by $\Sigma(V_{CC} - V_{IL})(|I_{IL}|) = \Sigma(V_{CC} - V_{OH})(|I_{OH}|) = \Sigma(V_{OH})(|I_{OL}|)$
 - AC timing for external memory signals on 38P70 are measured from either the .8 or 2.0 volt points as applicable. High means at or above 2.0 volts. Low
- means at or below .8 volts. Stable means high or low as appropriate. Rising means signal is no longer below .8 volts. Falling means signal is no longer above 2.0 volts. Hold times on outputs assume full rated load on reference signal and 20 pF load on specified signal. For 97400 series, only applicable specification is TAas as no other signals are available to reference to other than A0-A11.

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

$t_{psc} = t\Phi \times$ Prescale Value

Interval Timer Mode:

- Single interval error, free running (Note 3) $\pm 6t\Phi$
 Cumulative interval error, free running (Note 3) 0

Error between two Timer reads (Note 2)	$\pm (tpsc + t\Phi)$
Start Timer to stop Timer error (Notes 1, 4)	$+ t\Phi \text{ to } - (tpsc + t\Phi)$
Start Timer to read Timer error (Notes 1, 2)	$-5t\Phi \text{ to } - (tpsc + 7t\Phi)$
Start Timer to interrupt request error (Notes 1, 3)	$-2t\Phi \text{ to } -8t\Phi$
Load Timer to stop Timer error (Note 1)	$+ t\Phi \text{ to } - (tpsc + 2t\Phi)$
Load Timer to read Timer error (Notes 1, 2)	$-5t \pm \text{ to } - (tpsc + 8t \pm)$
Load Timer to interrupt request error (Notes 1, 3)	$-2t\Phi \text{ to } -9t\Phi$

Pulse Width Measurement Mode:

Measurement accuracy (Note 4)	$+ t\Phi \text{ to } - (tpsc + 2t\Phi)$
Minimum pulse width of EXT INT pin	$2t\Phi$

Event Counter Mode:

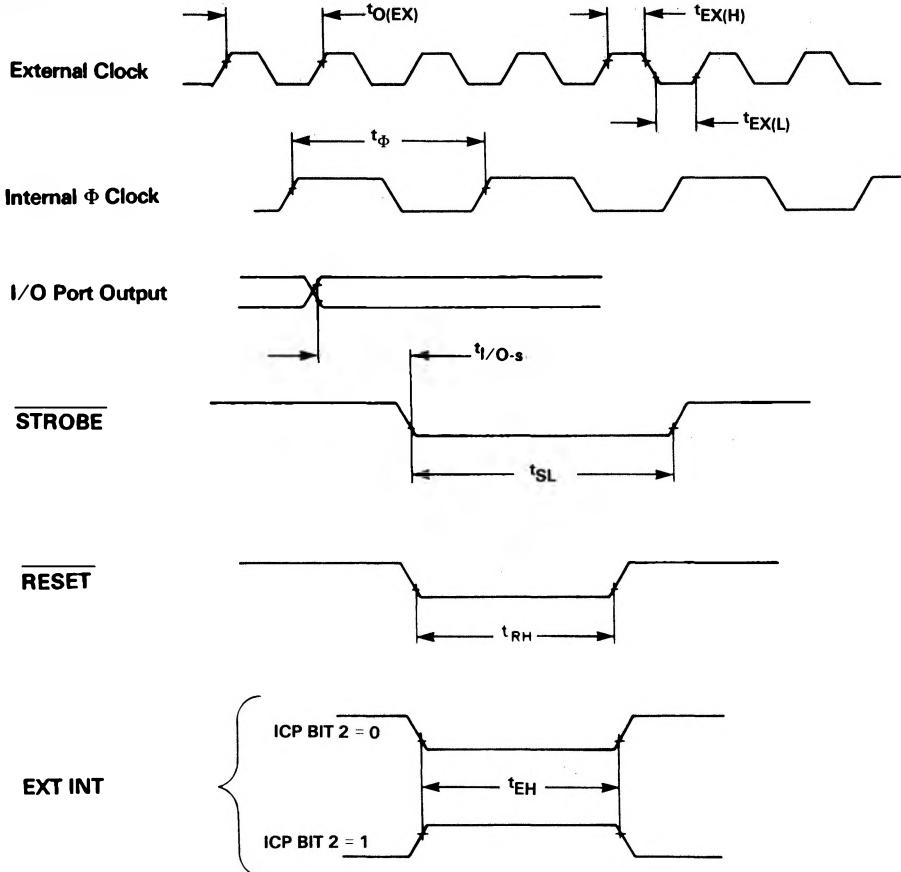
Minimum active time of EXT INT pin	$2t\Phi$
Minimum inactive time of EXT INT pin	$2t\Phi$

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

AC TIMING DIAGRAM

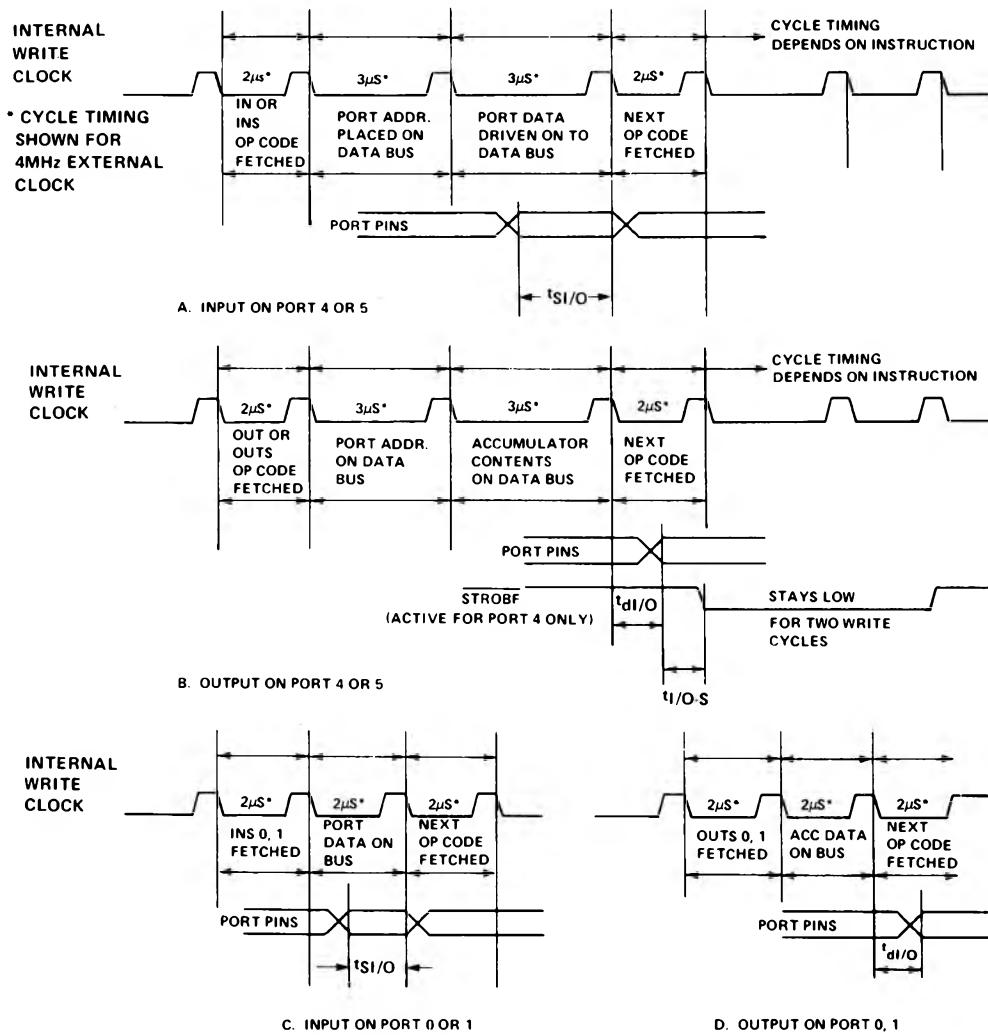
Figure 16



Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

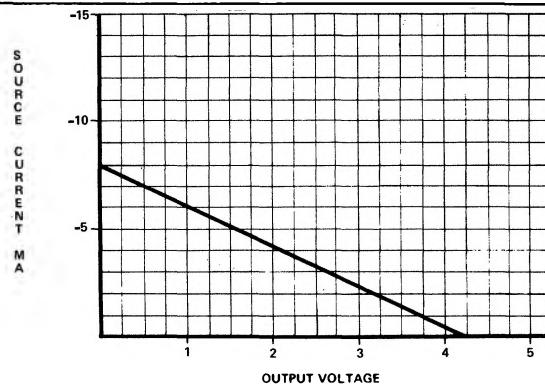
INPUT/OUTPUT AC TIMING

Figure 17



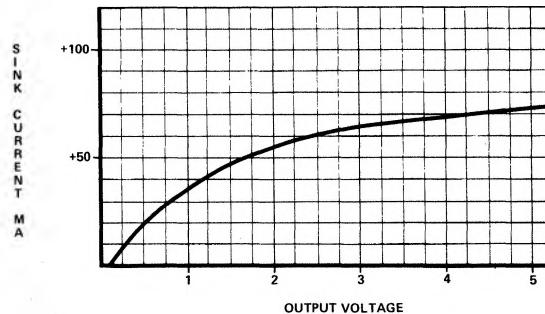
STROBE SOURCE CAPABILITY
(TYPICAL AT $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$)

Figure 18



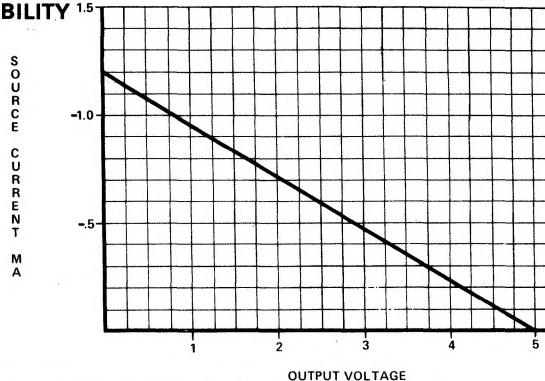
STROBE SINK CAPABILITY
(TYPICAL AT $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$)

Figure 19



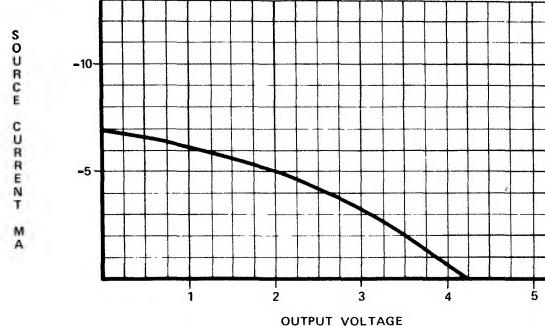
STANDARD I/O PORT SOURCE CAPABILITY^{1.5}
(TYPICAL AT $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$)

Figure 20



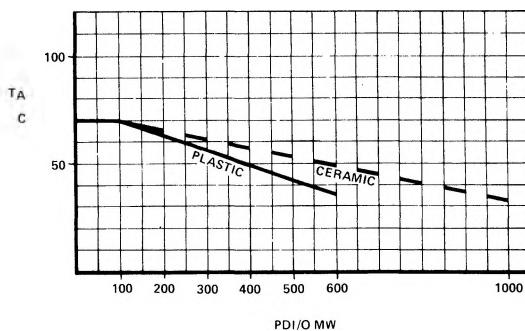
DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$)

Figure 21



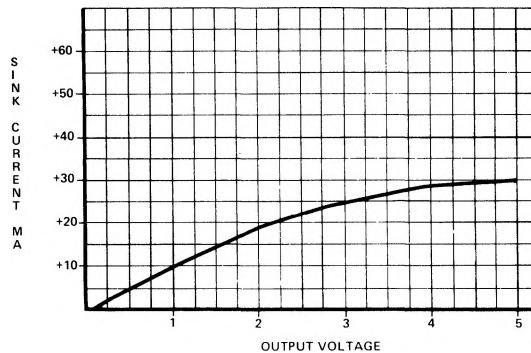
I/O PORT SINK CAPABILITY
(TYPICAL AT $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$)

Figure 22



**MAXIMUM OPERATING TEMPERATURE VS.
I/O POWER DISSIPATION**

Figure 23



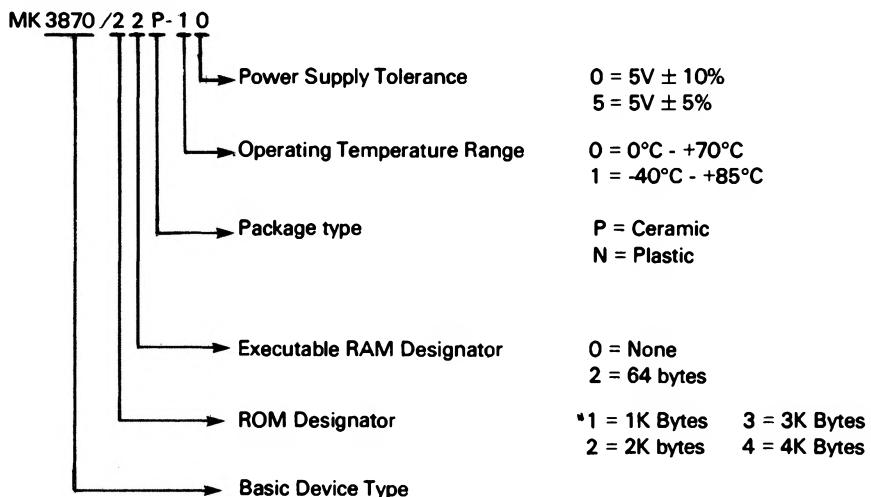
ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional

information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number. Note: the specific device order number will be used to differentiate between the MK3870/20 with 12-bit Address Registers and the original 3870 with 11-bit Address Register, as mentioned in an earlier section.

GENERIC PART NUMBER

An example of the generic part number is shown below.

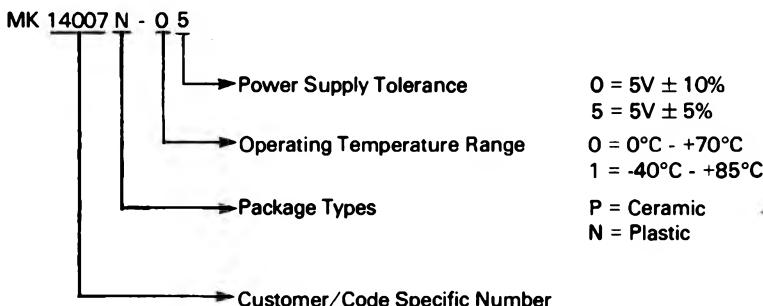


An example of the generic part number for the EPROM device is shown below.

MK38P70/02 R-05

DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.