PURDUE
UNIVERSITY

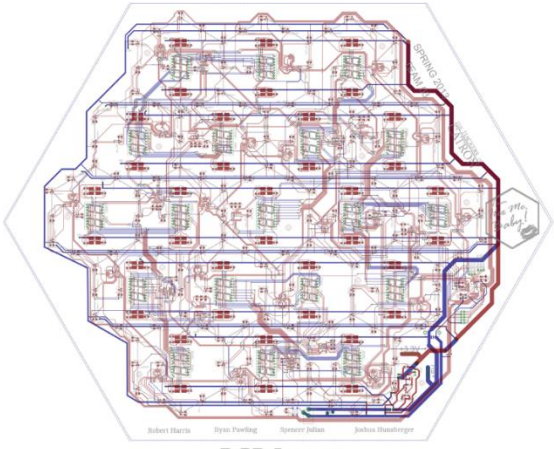
Elmore Family School of Electrical & Computer Engineering

ECE 47700 – Digital Systems Senior Design Project

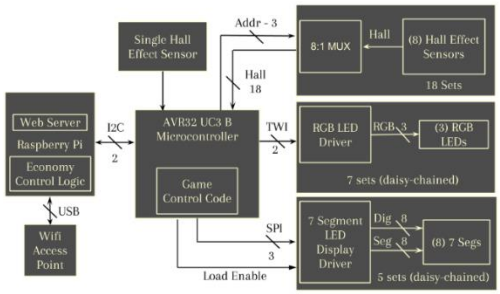
Fall 2022 Course Syllabus

A Game in Progress

Web Application



PCB Layout



Block Diagram

1.0 Course Description

Digital Systems Senior Design Project (ECE 477) is a structured approach to the development and integration of embedded microcontroller hardware and software that provides senior-level students with significant design experience applying microcontrollers to a wide range of embedded systems (e.g., instrumentation, process control, telecommunications, intelligent devices, etc.). The primary objective is to provide practical experience developing integrated hardware and software for embedded microcontroller systems in an environment that models one which students will most likely encounter in industry.

One of the unique features of this senior design option is that each team gets to choose their own specific project (subject to some general constraints) and define specific success criteria germane to that project. In general, this approach to senior design provides students with a sense of project ownership as well as heightened motivation to achieve functionality.

1.1 Course Staff

Name	*Title / Role*	*E-mail Address*
Dr. Phil Walter	Instructor / Project Advisor	philwalter@purdue.edu
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1.2 Lecture Outline

Week(s)	*Lecture Topics*
1	Course introduction, defining requirements
2	Hardware interfacing
3	Discrete components
4	Power considerations
5	Embedded software, hardware design fundamentals
6	Hardware design techniques, assembly and soldering
7	Assembly and soldering, design review guidelines
8	Formal design reviews
9	PCB verification and ordering, hardware debugging
10	Professional component overview case study, legal and regulatory
11	Reliability and safety
12	Ethical and environmental considerations
13-14	Case studies
15	Next steps, final presentation guidelines
16	Final presentations

2.0 Summary of Design Project Specifications / General Requirements

Work on the design project is to be completed in teams of four students. The design project topic is flexible, and each group is encouraged to pick a project that uses the strengths and interest areas of their group members. The design must have the following components:

- **Microcontroller:** To help make the project tractable, recommended microcontroller choices include STM, PIC, and Atmel variants. Development tools are readily available in lab to support these devices. Further, the devices themselves are relatively low cost and readily available. Optionally, auxiliary processing can be accomplished using a "motherboard". Examples of these directly supported are Intel Atom and ARM-based platforms.
- **Interface to Something:** The embedded system designed must interface to some other device or devices. It could be a computer, smart phone, tablet, or some other embedded device. Interface standards that can be used include: asynchronous or synchronous serial, parallel, Universal Serial Bus (USB), Bluetooth, Bluetooth Low Energy, Zigbee, Ethernet, Infrared (IR), Radio Frequency (RF), etc. This requirement has a large amount of freedom. To help with some of the more complex interfaces such as Ethernet and USB, dedicated chips which encapsulate the lowest layers of the interface can be utilized. This makes using these interfaces easier to handle but not necessarily trivial. (NOTE: *Interfaces involving A.C. line current require special permission – see the instructor for details.*)
- **Custom printed circuit board:** Through the process of the design, each group will be required to draw a detailed schematic. From the schematic, a two-layer printed circuit board will be created. Teams are responsible for ordering circuit boards, assembly (soldering parts on the board), and completing the final stages of debugging and testing on their custom boards.
- **Be of personal interest to at least two team members:** It is very difficult to devote the time and energy required to successfully complete a major design project in which you and/or your team members have no personal interest. There are *lots* of possibilities, ranging from toys and games to "useful and socially redeeming" household items, like audio signal processors and security systems.
- **Be tractable:** You should have a "basic idea" of how to implement your project, and the relative hardware/software complexity involved. For example, you should not design an "internet appliance" if you have no idea how TCP/IP works. Also, plan to use parts that are reasonably priced, have reasonable footprints, and are *readily available*. Be cognizant of the prototyping limitations associated with surface mount components.
- **Be neatly packaged:** The finished project should be packaged in a reasonably neat, physical sound, environmentally safe fashion. Complete specification and CAD layout of the packaging represents one of the project design components.
- **Not involve a significant amount of "physical" construction:** The primary objective of the project is to learn more about *digital system* design, not mechanical engineering! Therefore, most of the design work for this project should involve digital hardware and software.

2.1 Project Proposal

Each group should submit a proposal outlining their design project idea. This proposal should be efficient and concise. It should include your design objectives, design/functionality overview, and project success criteria. The five success criteria common to all projects include the following:

- Create a bill of materials and order/sample all parts needed for the design
- Develop a complete, accurate, readable schematic of the design
- Complete a layout and etch a printed circuit board
- Populate and debug the design on a custom printed circuit board
- Package the finished product and demonstrate its functionality

In addition to the success criteria listed above, a set of **five significant** *project-specific* success criteria should be specified. The degree to which these success criteria are achieved will constitute one component of your team's grade.

Forms for the preliminary and final versions of your team's project proposal are available on the course web site. Use these skeleton files to create your own proposal. Note that the proposal should also include assignment of each team member to one of the design components as well as to one of the professional components of the project.

2.2 Group Account and Team Webpage

Each team will be assigned an ECN group account to use as a repository for all their project documentation and for hosting a password-protected team web page. The team web page should contain datasheets for all components utilized, the schematic, board layout, software listings, interim reports, presentation slides, etc. It should also contain the progress reports (prepared in advance of the weekly progress briefings) for each team member. At the end of the semester, each team website will be archived on the course website.

2.3 Design Review

Part way through the design process, there will be a formal design review. This is a critical part of the design process. In industry, this phase of the design process can often make or break your project. A good design review is one where a design is actively discussed and consensus is reached. The design review is often the last chance to catch errors before the design is "frozen", boards are etched, and hardware is purchased. *A friend is not someone who rubber-stamps a design, but rather one who actively challenges the design to confirm the design is correct.*

Approach the design review from a top-down, bottom-up perspective. First, present a block diagram of your design and explain the functional units. Then drop to the bottom level and explain your design at a schematic level. Be prepared to justify every piece of the design; a perfectly valid answer, however, is applying the recommended circuit from an application note. If you do use a circuit from an application note, have the documentation on hand and be able to produce it. *Your grade for the design review will not be based on the number of errors identified in your design.* The best engineers make mistakes, and the purpose of the design review is to *catch them* rather than spend *hours of debugging later* to find them. The design review will be graded primarily on how well the group understands their design and the professionalism with which they present it.

3.0 Design Project Milestones

Each group is responsible for setting and adhering to their own schedule; however, there are several important milestones, as listed in the table below. Note, the preliminary project proposals are submitted before the semester begins as part of the enrolment process. As such, students were expected to submit a final proposal in week 1. (See Course Calendar for due dates.)

Week	*Milestone*	*Deliverables*
1	Devise a project budget, schedule, and determine project specific success criteria.	Final Project Proposal
2	Research and select major components, including the family of microcontroller (e.g. PIC32, STM32, etc.) and power supply components (switching regulator, battery management).	Functional Specification
3	Check out a microcontroller development board and write code that exercises various on-chip peripherals (e.g., blink an LED at variable rate specified by analog input voltage, debug via RS 232). Order some parts for prototyping purposes. Formulate PSSC and initial block diagram.	Software Overview and Component Analysis
4	Finalize and order major components. Order motherboard (Atom, ARM, etc.) if applicable. Begin prototyping microcontroller interfaces (work on parts of circuit most complex first). Start prototyping power supply circuitry. Begin selecting secondary components (e.g., voltage level translators, specialty diodes, capacitors, resistors, etc.) – note that an RS 232 level translator chip is required for the microcontroller to communicate with a host PC via RS 232).	Bill of Materials and Electrical Overview
5	Create packaging CAD drawings. Continue prototyping interface and support circuitry.	Mechanical Overview
6	Begin schematic and begin PCB layout. Check footprints created for PCB library against actual components. Start developing schematics and create footprints needed for PCB parts library. Start testing motherboard (if applicable).	Preliminary Schematic/ PCB footprint/component development
7	Finalize PCB layout for Design Review. Continue software development and testing. Prepare for Design Review.	Preliminary PCB Layout and Software Formalization
8	Practice presentation. Continue software development.	Design Review Presentation
9	Incorporate changes/comments from Design Review.	Proof-of-Parts, Final Schematic, and Final PCB Layout
10	Continue software development and testing.	Legal Analysis
11	Begin populating/testing PCB. Test PCB section-by-section as parts are added, porting software as you go – ***add functions one-by-one so you know what it was that "broke" your code or your board when things stop working.***	Reliability and Safety Analysis Report
12		Ethical/ Environmental Impact Analysis Report
13		User Manual
14	Finalize packaging and system integration. Start assembling and editing Final Report.	No deliverables (Thanksgiving)
15	Create Poster and Senior Design Report. Finish editing Final Report. Prepare for Final Presentation.	ECE Educational Report
16	Submit project deliverables. Create PSSC demo video. Practice Final Presentation.	Prepare for Final Presentation in week 17

4.0 Policies Regarding Project Hardware

ECE 477 is a senior design course that is designed to motivate and challenge students, as well as simulate the electronic design process in a professional setting. In order to provide sufficient challenge and maintain professionalism, only approved hardware is allowed to be used in final project deliverables. This course policy document serves to inform students about acceptable and unacceptable final hardware for use in their ECE 477 senior design projects. Final hardware and prototyping hardware are defined below.

4.1 Prototyping Hardware and Final Hardware

For the purposes of this course, prototyping hardware shall refer to any hardware used to test devices, software, concepts, or functions in a preliminary state. No restrictions are placed on hardware used to prototype for ECE 477; students may use whatever development hardware and tools they desire.

Final hardware refers to the hardware that is used in the final senior design project, and refers to any hardware used to satisfy preliminary or final PSSCs for the course. Final hardware is subject to the rules described in this document. PSSCs can only be satisfied by projects utilizing valid final hardware; projects utilizing prototyping hardware for a particular function will be unable to satisfy PSSCs and will be insufficient for passing course outcomes.

4.2 Rules Concerning Final Hardware

The rules concerning valid final hardware for ECE 477 are listed below:

1. The ECE 477 staff shall have the sole determination of what is and what is not valid final hardware for an ECE 477 project.
2. In order to pass preliminary or final project-specific success criteria (PSSCs), a student team must use final hardware to realize the functions being tested in their PSSC (in the case of preliminary PSSCs) or their complete system (in the case of final PSSCs). Prototyping hardware will not be acceptable for realizing a given PSSC and will be insufficient to satisfy a given course outcome.
3. Student teams are required to adhere to final hardware rules concerning development boards and prototyping microcontrollers. These rules are elaborated on in section 4.3.
4. Student teams are required to adhere to final hardware rules concerning breakout boards and electronic shortcuts. These rules are elaborated on in section 4.4.
5. Student teams are required to adhere to final hardware rules concerning development IDEs. These rules are elaborated on in section 4.5.
6. Exceptions and modifications to these rules can be made at the sole discretion of the ECE 477 course staff. Students wishing to make such exceptions to policy must have written permission from the ECE 477 course staff to do so.

4.3 Course Policy Concerning Development Boards and Prototyping Microcontrollers

At the time of this writing, there are a number of development systems and prototyping devices created and sold by third parties, often catering to the hobbyist market. Popular contemporary examples of such devices include the Basic Stamp, the Arduino and its many variants, the Chipkit, the Flora development system sold by Adafruit, and many others. A general common feature of these devices is that they feature a printed circuit board, a microcontroller, microprocessor, or FPGA, passive components and/or ICs, and optionally a programming interface, such as JTAG, USB, or a breakout ICSP programming header. These prototyping systems may additionally include add-on daughterboard or mezzanine cards to expand their functionality (Arduino shields are a popular example of this, though other examples exist).

As these systems feature significant overhead to a microcontroller and/or printed circuit board performing the same functionality, these development systems may be appropriate for the purposes of prototyping but are inappropriate for use in final products on the market. In addition, students are expected to design, create, and assemble their own printed circuit boards, featuring a microcontroller in this class (a function which development boards fulfill). **As such, development and prototyping systems are banned for the purposes of final project hardware.** There are exceptions to this rule, and these are described below.

There are certain situations where the use of development and prototyping systems may be acceptable for final hardware. One such exception is made for motherboards and systems running embedded operating systems. Examples of such systems include the Raspberry Pi, BeagleBoard/BeagleBone, Pandaboard, Intel Atom Motherboards, and others. Another possible exception is made for systems that perform operations that are deemed to be computationally complex. An example of a computationally complex system that is generally allowed to be used as final hardware is an inertial measurement unit (IMU) or flight controller used in UAVs and other projects. Yet another exception is made for boards in which the functionality necessary for the student project is only available in a device with very difficult soldering or layout requirements. The primary area where this exception comes into play is in projects involving FPGAs, which often come in BGA or other packages that are not hand-solderable, and often require multilayer boards. If a student team believes their hardware qualifies for any of these exceptions, they must contact course staff to receive approval.

4.4 Course Policy Concerning Breakout Boards and Electronic Shortcuts

At the time of this writing, a number of third-party vendors exist that provide breakout boards and electronic shortcuts, primarily to hobbyists. Examples of such vendors include Sparkfun, Adafruit, and Seeed Studio, among many others. These devices generally consist of a relatively small and simple printed circuit board, containing a small number of integrated circuits and passive components, and often feature headers or plated holes to make the parts easy to solder or otherwise integrate into a system.

As these systems constitute significant overhead to the basic parts laid out on a custom circuit board, these electronic shortcuts may be appropriate for purposes of prototyping but are inappropriate for use in final products on the market. Additionally, students are expected to design and build custom circuit boards that are motivating and challenging to them. **As such, breakout boards and electronic shortcuts are banned for the purposes of final project hardware.** There are exceptions to this rule, and these are described below.

Under certain situations, the use of raw components may be unreasonable or unfeasible in the time constraints of ECE 477. In these instances, the use of breakout boards and electronic shortcuts may be acceptable. One such instance is when the functionality being performed by the breakout board or shortcut is deemed electromagnetically or procedurally complex. Common examples of where this shortcut applies include breakout boards that handle the functionality of a wireless interface (Bluetooth, Zigbee, RF, Wifi, GPS receivers, and others), a complex power regulator (some switching power supplies), or USB-to-serial interface ICs used in conjunction with certain microcontrollers. In these instances, the use of a drop-in module is generally allowed and even recommended. Another situation where breakout boards and electronic shortcuts are allowed are situations where the functionality necessary for the student project is not otherwise readily available in a component or components that are hand-solderable. Examples of this exception include certain ICs that are only available in ball grid array (BGA) packages, and many times certain sensors such as accelerometers, magnetometers, and pressure sensors are only available in packages which are extremely difficult or impossible to solder by hand. If a student team believes their hardware qualifies for an exception, they must contact course staff to receive approval.

4.5 Course Policy Concerning Development IDEs

In addition to the development systems featured in section 4.3, a number of third-party IDEs have been developed that accompany these systems. These IDEs often free the developer from having to write low-level code in languages like C and instead allow the creation of code in more abstracted languages such as Python, Perl, custom third-party languages, or even graphical GUIs. One of the best contemporary examples of such an IDE is the Arduino IDE, which can be used to develop “sketches” on certain Atmel chips in place of the lower-level, more general purpose AVRStudio IDE.

As the languages used by these tools are often highly abstracted, the code produced by development IDEs of this nature often contains excessive overhead and performs poorly when compared to comparable code written in a lower level language and compiled. Additionally, IDEs of this nature are considered low-effort and don't adequately simulate the software tools and tool-related challenges electrical engineering graduates are expected to use and deal with in the vast majority of professional settings. **As such, the use of development IDEs of this nature are banned for the purposes of final senior design projects.** If a student team believes their software development tools qualify for an exception to this rule, they must contact course staff to receive approval.

5.0 Policies Regarding Project Specific Success Criteria

ECE 477 is a student-led design class in which projects are chosen by student teams and proposed to ECE 477 course staff. Every project is different, but there still needs to be a method of determining whether a group of students has succeeded or failed in their project endeavor. To judge a team's success (or lack thereof), students must fulfill and demonstrate a series of project-specific success criteria (PSSCs).

A PSSC is a project-based objective that a senior design team wishes to accomplish during the course of the semester. For the purposes of the course, a senior design team must develop 5 distinct PSSCs and demonstrate them to the course staff. Successful demonstration of at least 3 PSSCs during the semester is necessary to pass ECE 477. Due to the nature of the course, there are some hard rules, as well as some general guidelines, when it comes to selecting PSSCs. These rules and guidelines are detailed below.

5.1 Course Rules Concerning PSSCs

There are a few hard rules regarding PSSCs. They are as follows:

1. Course staff shall have the final determination on the validity and successful demonstration of any and all PSSCs. NO EXCEPTIONS.
2. All student teams must select 5 project-specific success criteria (PSSCs) as part of their design process.
3. In order to pass ECE 477, all student teams must successfully demonstrate 3 of their 5 PSSCs. For purposes of satisfying the course outcome, students may demonstrate preliminary PSSCs in lieu of final PSSCs. Final and preliminary PSSCs are explained in section 5.2, below.
4. Project-specific success criteria (PSSCs) based on the default functionality of a component are prohibited. This rule is further elaborated upon in section 5.3, below.
5. All project-specific success criteria (PSSCs) must be focused on the student-implemented embedded hardware. This is explained in section 5.4, below. An exception to this rule is made for projects deemed by the course staff to be motherboard-based projects. Motherboard projects are described in section 5.4, below.
6. All project-specific success criteria should be phrased in terms of capabilities to perform a specified function (“An ability to...”)

For more details on the rules concerning PSSCs see the PSSCs policy on the course website

5.2 Preliminary and Final PSSCs

In order to fulfill one of the ABET outcomes for this course, and thereby pass ECE 477, students must demonstrate 3 of the 5 PSSCs they choose. To assist students in fulfilling this course requirement, PSSCs have been delineated by preliminary and final PSSCs.

Preliminary PSSCs are PSSCs that have been demonstrated on the final hardware, but not necessarily in final packaging or in a fully system-integrated project. The final hardware distinction is important; no prototyping or development hardware will be accepted for passing a PSSC. Successfully demonstrating a preliminary PSSC will provide the team with

acknowledgement of passing the PSSC for the purposes of the course outcome. No points towards a student's grade are awarded for the demonstration of a preliminary PSSC.

Final PSSCs are PSSCs that are successfully demonstrated on the packaged, fully-integrated final hardware. Successful demonstration of a final PSSC satisfies that PSSC from the perspective of the course outcome and additionally provides the student team with points towards their course grade. Final PSSCs can be demonstrated directly; it is recommended though not necessary to first demonstrate a preliminary version of the PSSC.

5.3 The Default Functionality of a Component Rule

In choosing PSSCs for a project, it is necessary that students choose criteria that will challenge and push them. As such, PSSCs that are based upon the default functionality of a component are prohibited.

One of the most common violations of this rule involves PSSCs focused around the use of a particular interface. At the time of this writing, projects utilizing wireless interfaces are extremely common, and many students write a PSSC of the general form “An ability to send/receive data via a *wireless interface*” (where the *wireless interfa*ce might be RF, Bluetooth, WiFi, Zigbee, etc.). If a team is using an off-the-shelf solution for said interface, this is not an acceptable PSSC, as it largely comes down to hooking up the interface and configuring it.

Examples exist beyond interfacing. If a team has onboard memory, then a PSSC about storing data in memory would not be acceptable as a PSSC. If a team has been allowed to use a filter IC, a PSSC about filtering data, as done automatically by the filter IC, is not an acceptable PSSC.

A primary shortcoming of the violating PSSCs described above is a lack of detail in the PSSC. To improve the PSSCs and make them valid, one of the most common methods is to add detail to the PSSC in question. Instead of writing “An ability to send and receive data over a wireless interface” (an invalid PSSC), a valid PSSC could detail the types of data a team expects their system to collect and send over such an interface (an improved and probably valid PSSC).

Far more examples exist than can be reasonably listed here. If in doubt, follow the two golden rules when it comes to PSSCs. First, if a team thinks a PSSC is too easy, and is being done entirely by a component, it is likely that that PSSC will be invalid under this rule. Second, if a team has any doubts about a PSSC, ask course staff for further clarification.

5.4 Embedded Hardware Focus of PSSCs

ECE 477 is embedded systems senior design. As such, the course is developed around embedded hardware, and the ABET outcomes for the course reflect this fact. Therefore, in order to be eligible for satisfying the educational outcomes of ECE 477, at least 3 of the 5 PSSCs are required to be based upon the embedded hardware implemented by the senior design teams.

A common issue students encounter related to this rule is to have PSSCs that are performed on a general-purpose computer. PSSCs related to software written for a general purpose software, such as GUIs, web-interfaces, etc. can be the focus of up to 2 PSSCs, but not more.

6.0 Policies Regarding Progress Reports

Over the course of the semester, all students are expected to maintain an electronic progress report detailing their individual progress and contributions towards their senior design projects. Progress reports are to be written on a weekly basis, and are evaluated by the ECE 477 course staff frequently over the semester. Progress reports are one of the primary resources available to any individual attempting to reproduce a particular project or a given ECE 477 student's work.

Progress reports constitute a course outcome that must be individually satisfied in order to receive a passing grade for the course. In the event that a team member's contribution to a project is contested, well-written and thorough progress reports can assist the student in defending his or her effort on a senior design project. Therefore, doing well on progress reports will have a significant positive impact on a student's experience in ECE 477.

Progress reports are individual efforts designed to capture the development activities of a particular student, and as such are written and graded individually. Use of progress report entries to detail the efforts of team member development efforts that the author had no part in is not allowed. Copying portions of progress report entries from other team members is similarly prohibited; violation of this rule could subject the student or students in question to grade penalties or academic dishonesty citations.

6.1 Progress Report Templates

Students will be provided with a standard template to use for their personal project notebooks. For ease of grading and evaluating progress reports, all students are expected to use the templates provided.

6.2 Progress Report Evaluation

As referenced in the notebook evaluation rubrics in the homework section of the ECE 477 course website, there are 3 categories used for grading progress reports. These categories are:

1. Level of Technical Detail
2. Pictures, Drawings, and Diagrams
3. Technical Writing Style and Clarity

6.2.1 Level of Technical Detail

This is the “meat” of a progress report, and as such is weighted the most heavily of the project notebook grading criterion. With a thorough, detailed report, a student's work can be readily reproduced by others, and helps to result in a high-quality overall project. Sloppy, poorly-written, and incomplete reports are of little or no help to an end user who is attempting to reproduce a student's work from his or her notes.

A technically detailed project report entry answers the following questions (where applicable) clearly and concisely:

- What did the student work on?
- How did the student work on it? (Tools? Programs? Test rig? Etc.)
- What was the result, and how does this affect the project?
- What did the student learn?
- What are the next steps that must be taken?

6.2.2 Pictures, Drawings, and Diagrams

Large, endless blocks of text can be very formidable to a reader, and sometimes the content of a student's report can be improved considerably through the inclusion of pictures (or other visual content). This is where the pictures, drawings, and diagrams portion of the report score comes in. Getting a good score on this is as simple as including a number (3 or more each week) of relevant, unique pictures and diagrams related to your project. Pictures could include but aren't limited to: screenshots/images of schematics or PCB designs generated in software, photographs of your project and/or prototyping setups you have created to test features of your project, MATLAB graphs, and screenshots from oscilloscopes or other laboratory measurement equipment. Even students whose primary responsibility is coding can include relevant pictures of their work on a project in the form of screenshots of pseudo-code, GUI screenshots, flowcharts, graphical representations of algorithms, or useful graphical output produced by one's code.

It is important that the pictures a student chooses to include in his or her progress report be relevant to the work he or she, as opposed to the other team members, is performing. If, for example, a student's progress report entries detail their efforts on a project's firmware but the pictures for those entries are of hardware being assembled, this may reflect negatively on that student's “pictures” score. In addition, pictures utilized in student progress reports should be unique; several images of an object taken from different angles will only be counted as a single image. Pictures instantiated in progress reports should be small, in terms of physical size as well as in terms of file size. This will ensure that the reports loads quickly and is simultaneously easy to read. However, the course staff would like to see actual images in the content of student progress reports, so please do not simply use hyperlinks to external photos.

The recommended best practice for progress report images is to create a small (600x450 px or less) image, insert that into the progress report, and then modify that image to include a hyperlink to the larger source image. Gimp and ImageMagick are two excellent programs that students may find useful for resizing images and converting between file formats.

A student's progress report should contain at least one image each week. Progress reports containing zero images will receive a score of zero for the Pictures, Drawings, and Diagrams section of their report grade.

6.2.3 Technical Writing Style and Clarity

Along with technical detail, this section of your notebook forms the “core” of your progress report, and is thus weighted heavily in the evaluation grade. To receive a high score in this section, a student must write professionally. Proper spelling and good grammar are essential for high quality technical writing, and are thus necessary for full points. A useful method for improving one's score in this section is to copy and paste the contents of one's progress report into a text editor that features a spell checker. Spelling and grammar mistakes can then be identified and corrected prior to evaluation.

6.3 Maintaining Progress Reports in the Event of Student Absences

Over the course of the semester, circumstances may arise in which a student is unable to maintain his or her ECE 477 progress report for some period of time. Examples of such circumstances include job interviews, conferences, unexpected illness or accident, or family bereavement. In the event that such circumstances arise, please contact course staff so that they are aware of the absence and can handle it accordingly. No activity is required in the event of holidays and official university student breaks and holidays (such as fall break, spring break, etc.).

7.0 Policies Regarding Online Collaboration Tools

A veritable plethora of online collaboration tools have been developed that allow easy access, sharing, and collaboration of source code and other documents online. Popular examples at the time of this writing include Google Code, Google Docs, github, bitbucket, and SourceForge, though many others exist. While the use of revision control in student projects is strongly recommended, there are certain guidelines and rules students should be aware of when working with online collaboration tools. These guidelines and rules are listed below.

7.1 Rules Concerning Online Collaboration Tools

There are several rules pertaining to the use of online collaboration tools. These are fairly straightforward, and listed below:

1. Student teams are allowed to use online collaboration tools at the sole discretion of the ECE 477 course staff. This right may be amended or revoked at any time.
2. Online collaboration tools are not an acceptable alternative to the provided student websites and laboratory notebooks. If an online collaboration tool is used, students are still expected to host all relevant project information on their team website and keep laboratory notebooks subject to the course guidelines on laboratory notebooks. Use of automated scripts to populate course websites and notebooks is acceptable, but it is the responsibility of the student team members to ensure that the scripts work correctly and transfer the necessary data to the course website.
3. Student teams are expected to perform their own work over the course of ECE 477. Therefore, all code contributions to an ECE 477 team's student-written code should come from team members. Code improvements and merges from third parties while a team is enrolled in ECE 477 are not allowed. Students or teams in violation of this rule may be subject to academic dishonesty actions and disciplinary measures.

7.2 Guidelines Concerning Online Collaboration Tools

In addition to rules concerning online collaboration tools, the course staff has a few recommendations concerning such tools. These are:

1. If any aspect of the online collaboration course policy is unclear, students are encouraged to contact course staff for further clarification
2. It is suggested that students utilize an organized, consistent directory structure in their repositories. Doing so is professional and makes files easy to find and can simplify commits to a repository.

8.0 Policies Regarding Laboratory Facilities and Equipment

ECE 477 is a project-based senior design course in which students are expected to design and construct a functional hardware prototype of an embedded design project. To assist students in this endeavor, laboratory facilities and equipment are provided for student use. This course policy document serves to inform students of rules and guidelines related to the usage of laboratory facilities and equipment.

8.1 Laboratory Facilities

The Purdue School of Electrical Engineering provides Digital Systems Senior Design (ECE 477) with exclusive use of designated facilities for laboratory activities related to senior design. Access to these laboratories is regulated through the use of electronic passcode door locks. The laboratories include workbench space assigned to student teams, student team lockers for senior design materials, cabinets for materials related to senior design, and shared stations for soldering and other electronics assembly activities. The ECE 477 laboratory facilities are managed by the Digital Systems Laboratory Engineer.

For details on lab access and guidelines see the lab facilities section within the policies. Failure to follow rules that are contained within the laboratory policies could result in the removal of lab privileges or other disciplinary action for the student in question or the entire student team.

Failure to follow the rules contained in this document could result in the removal of lab privileges or other disciplinary action for the student in question or the entire student team.

8.2 Use of the Course Laboratory Facilities

The following rules govern student use of the ECE 477 laboratory facilities.

1. Use of the ECE 477 labs is authorized for staff, students officially enrolled in ECE 477, and those with written consent from the ECE 477 staff. Use of the lab facilities by other individuals is strictly prohibited.
2. Electronic passcodes to the lab facility door locks are provided to students enrolled in ECE 477. These passcodes are confidential and may not be shared with any other individual.
3. For liability and safety reasons, use of any electrical and mechanical assembly tools (drill presses, soldering irons, etc.) require two team members to be present. This rule does not apply to computer usage and other design-related activities.
4. Smoking, food, and drink within the ECE 477 labs are strictly prohibited.
5. Students are responsible for maintaining clean and orderly laboratory facilities. In particular, the shared soldering stations are cleaned on a weekly basis. Students are highly discouraged from leaving team items or personal belongings at the shared soldering stations.
6. When a team member is not present, student team valuables should be locked in the provided team lockers. The ECE 477 staff is not responsible for lost or stolen items.

8.3 Course Laboratory Equipment

The ECE 477 lab contains course laboratory equipment to assist students with their senior design projects. For the purposes of this policy document, course laboratory equipment refers to any equipment in the senior design lab which is provided for student use that does not require a student to sign out the equipment with the Digital Systems Laboratory Engineer.

Examples of course laboratory equipment include:

- Laboratory desktop computers, monitors, peripherals, printers, and other computing equipment
- Workbenches, chairs, shelves, and other laboratory furnishings
- Oscilloscopes, power supplies, digital multi-meters, spectrum analyzers, waveform generators, and other workbench test and measurement equipment
- Soldering irons, hot air rework tools, microscopes, and other shared fabrication tools
- Wire cutters, SMD tweezers, X-Acto knives, and other shared laboratory tools

8.4 Rules Concerning Course Laboratory Equipment

The following rules govern the use of ECE 477 course laboratory equipment.

- The laboratory equipment contained in the ECE 477 lab facilities is to be used for senior design activities or activities given written consent by the ECE 477 staff. Use of laboratory equipment for other activities is strictly prohibited.
- Laboratory equipment provided to students may not be rearranged or removed from the ECE 477 lab without the express written consent of the ECE 477 staff.
- Writing on, vandalizing, or otherwise defacing course laboratory equipment is strictly prohibited.
- Sitting on anything other than the chairs provided is prohibited, and placing feet on anything other than the floor is also strictly prohibited.
- Problems and malfunctions concerning course laboratory equipment should be promptly reported to ECE 477 course staff.

8.5 Student Laboratory Equipment

In addition to the course laboratory equipment provided to students, the ECE 477 staff are able to purchase or provide student laboratory equipment to assist ECE 477 senior design teams at no cost to the students. For the purposes of this policy document, student laboratory equipment refers to any special item or piece of equipment that requires student teams to sign out the equipment in order for the equipment to be used. Examples of student laboratory equipment include:

- Motherboards, development boards, breakout boards, or other electronic shortcuts used by a team for prototyping purposes
- Programming or debugging tools specific to a particular team's target microcontroller or other embedded processor

- Specific mechanical tools such as crimpers, specialty hand tools, or other such tools
- Any other item that the course staff deems valuable and reusable to assist current and future generations of ECE 477 students

8.6 Rules Concerning Student Laboratory Equipment

The following rules govern the use of ECE 477 student laboratory equipment.

1. Student laboratory equipment must be checked out by filling out a form provided by the Digital Systems Laboratory Engineer. Student lab equipment is the property of ECE 477, and must be checked back in to the ECE 477 course staff in good condition at the end of the semester. Failure to do so may result in academic penalties to the offending team.
2. Student laboratory equipment should be used for ECE 477 activities and activities receiving written approval from the ECE 477 course staff. Other uses of student laboratory equipment are prohibited.
3. In the event that a piece of student laboratory equipment is requested for purchase in ECE 477, course staff will have final determination over the purchase and whether or not that purchase request is reasonable and useful to ECE 477.

8.7 Classroom Guidance Regarding Protect Purdue

The Protect Purdue Plan, which includes the Protect Purdue Pledge, is campus policy and as such all members of the Purdue community must comply with the required health and safety guidelines. Required behaviors in this class include: staying home and contacting the Protect Purdue Health Center (496-INFO) if you feel ill or know you have been exposed to the virus, properly wearing a mask in classrooms and campus building, at all times (e.g., mask covers nose and mouth, no eating/drinking in the classroom), disinfecting desk/workspace prior to and after use, maintaining appropriate social distancing with peers and instructors (including when entering/exiting classrooms), refraining from moving furniture, avoiding shared use of personal items, maintaining robust hygiene (e.g., handwashing, disposal of tissues) prior to, during and after class, and following all safety directions from the instructor.

Students who are not engaging in these behaviors (e.g., wearing a mask) will be offered the opportunity to comply. If non-compliance continues, possible results include instructors asking the student to leave class and instructors dismissing the whole class. Students who do not comply with the required health behaviors are violating the University Code of Conduct and will be reported to the Dean of Students Office with sanctions ranging from educational requirements to dismissal from the university.

Any student who has substantial reason to believe that another person in a campus room (e.g., classroom) is threatening the safety of others by not complying (e.g., not wearing a mask) may leave the room without consequence. The student is encouraged to report the behavior to and discuss next steps with their instructor. Students also have the option of reporting the behavior to the Office of the Student Rights and Responsibilities. See also Purdue University Bill of Student Rights.

9.0 Course Grade Determination Policies and Procedures

ECE 477 is a course that requires both individual and team-based efforts in order for a given student and team to succeed. The ability of a student to pass ECE 477 and graduate from the Purdue University School of Electrical Engineering undergraduate degree program hinges on the student and team successfully satisfying the evaluation criteria for ECE 477. The method by which student grades are determined is detailed in this section.

Student grades are based upon individual and team grade components. For the purposes of the course, the individual component of a student's grade is based upon efforts undertaking specifically by the student in question. The team component of a student's grade is based upon efforts undertaken by both the student and other team members that impact the success of the team as a whole.

9.1 Grade Determination

Student course grades will be determined per the breakdown in Table 1, below:

Table 1. Determination of Student Grades

Team Components (40% of total)		**Individual Components (60% of total)**	
Project Success Criteria Satisfaction*	20.0%	Weekly Progress Update Reports*	20.0%
Design Review*	15.0%	Design Component Report*	15.0%
Final Presentation*	10.0%	Professional Component Report*	15.0%
Final Project Archive*	15.0%	Individual Contribution	20.0%
Concept Development Assignments	10.0%	Class Attendance and/or Participation	10.0%
System Integration and Packaging	20.0%	Mandatory Lab Session Attendance	10.0%
Educational (Senior Design) Report*	5.0%	Confidential Teammate Reviews (2)	5.0%
PCB Completion and Submission*	5.0%	Design Review and Final Presentation Peer Evals	5.0%
Bonus Components (added to grade total)			
Early completion		1.0% per week early (team)	
Design bonus contracts		(variable – negotiated with course staff before Week 6)	
Design Showcase participation		1.0% per individual	
Design Showcase poster		1.0% per team	
Purdue mycourseval Evaluation		0.5% per individual	
Instructor discretion (borderline resolution)		0.5% per individual	

* *items directly related to ABET course outcome assessment*

A description of each component of the grade determination is discussed in sections 9.4, 9.5, and 9.7. Note that some items are directly related to the course outcomes, as detailed in section 9.3.

Student performance on various elements of the course will be used to calculate a student's weighted percentage grade based on the weights in Table 1, above. Letter grades are then assigned on a 90-80-70-60 scale. Letter grades in the upper 30% of each range will receive a "+" designation, and those that fall in the lower 30% of each range will have a "-" designation.

9.1.1 Incompletes and Conditional Failures

A grade of "incomplete" (I) or "conditional failure" (E) will be given *only* for cases in which there

are ***documented*** medical or family emergencies that prevent a student from completing required course work by the end of the semester. University regulations stipulate that a student must be passing in order to ***qualify*** for a grade of "I" or "E".

9.1.2 Borderline Cases

A "borderline" is officially defined as a weighted percentage grade within 0.5% of a cutoff when the **final** grade calculation is performed. Before course grades are assigned, the instructor will carefully examine all such cases and determine if the next higher grade is warranted. Grade adjustments are made at the sole discretion of the course staff and are not guaranteed.

9.2 Professionalism and Academic Dishonesty

Unless otherwise noted, students are expected to do their own work, and not copy the work of any other individual, past or present. Any and all sources used in the completion of ECE 477 lab activities should be properly referenced, and where appropriate, the level of original work performed by the student should be noted. Any documented case of academic dishonesty will result in a failing grade for the course as well as possible disciplinary action. All cases of academic dishonesty will be reported to the ECE Associate Head as well as to the Dean of Students. ***A professional person does not take credit for the work of somebody else.***

9.3 Learning Outcome Assessment

In order to satisfy ABET course requirements, each student is expected to successfully demonstrate the set of learning outcomes approved by the ECE Senior Design Committee, listed in Table 2 along with the evaluation instruments used to assess their demonstration.

Table 2. Course Outcome Assessment Instruments

Outcome	*Course Outcome*	*Evaluation Instruments Used*
(i)	An ability to apply engineering design to create a product that meets the specified needs of this engineering design experience with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.	Design Component Homework
(ii)	An ability to develop and conduct experimentation, analyze and interpret data, and use engineering judgment to draw conclusions related to the development of the product of this engineering design experience.	Individual Progress Reports
(iii)	An ability to identify, formulate, and solve complex engineering problems arising from this engineering design experience by applying principles of engineering, science, and mathematics.	PCB Completion and Submission
(iv)	An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives associated with this design experience.	Project Specific Success Criteria Satisfaction (general ***and*** project-specific)
(v)	An ability to communicate effectively with a range of audiences appropriate to this design experience in both a written report and oral presentation.	Professional Component Homework
(vi)	An ability to acquire and apply new knowledge as needed, using appropriate learning strategies to complete the engineering design experience associated with this course.	Educational (Senior Design) Report
(vii)	An ability to recognize ethical and professional responsibilities associated with this engineering design experience and make informed judgments which must consider the impact of the product of this engineering design experience in global, economic, environmental, and societal contexts.	Midterm Design Review, Final Presentation, and Final Project Archive

In order for a student to successfully demonstrate a given course outcome, a minimum score of 60% shall be required on its associated evaluation instrument. An exception to this rule is made for success criteria satisfaction, for which 100% of the general success criteria must be passed *in addition to* 60% of the project-specific success criteria.

9.4 Description of Team Components

The team component of a student's grade is responsible for 40% of their overall grade. The elements of the team component score are listed out in detail in the subsections below.

9.4.1 Project Success Criteria Satisfaction

ECE477 requires teams to develop a set of 5 Project-Specific Success Criteria (PSSCs). These five PSSCs are the engineering requirements of the project in which the team will focus their engineering design efforts to meet the minimum ECE design criteria for the School and ABET. A team must successfully achieve at least three of these PSSCs in preliminary testing on the final project hardware in order to meet ABET requirements and pass the course. Please note that there are specific course policies that must be observed when selecting project specific success criteria and when demonstrating their achievement. More information on these course policies can be found in the "PSSC Policy" document, available on Brightspace and in Section 5, above.

9.4.2 System Integration and Packaging

In addition to a team's ability to satisfy project success criteria, the system integration score is a measure on the part of the course staff of how successfully the team was able to produce a refined final prototype of the proposed senior design project. This score includes things such as whether or not the senior design project was packaged, and how successfully and professionally it was done, as well as the extent to which electronic systems were combined together to produce a complete, working design. System integration and packaging is worth 20% of the student's team component grade, or 8% of the student's overall grade.

9.4.3 Midterm Design Review

During the middle of the semester, all ECE 477 teams are expected to present their projects in the form of a midterm design review. The midterm design review allows course staff to assess students' presentation skills as well as their preparation and progress at the middle of the semester. A score of 60% on the midterm design review is required to partially satisfy an ABET course outcome (this is further described in section 9.3). The midterm design review is worth 15% of the student's team component grade, or 6% of the student's overall grade.

9.4.4 Final Presentation

ECE 477 student teams are required to conduct a final presentation summarizing their development activities and progress on their senior design projects over the course of the semester. The final presentation allows course staff to assess students' presentation and communication skills. A score of 60% on the final presentation is required to partially satisfy an ABET course outcome (this is further described in section 9.3). The final presentation is worth 10% of the student's team component grade, or 4% of the student's overall grade.

9.4.5 Final Project Archive

At the end of the semester, student teams are required to compile revised assignments and source code and submit a final project archive for their respective senior design projects. The final archive provides the course staff with the opportunity to assess the student teams' abilities to communicate technical information in written form. A minimum score of 60% on the final archive is required to partially satisfy an ABET course outcome (this is further described in section 9.3). The final archive is subject to the late assignment policy defined in section 9.6. The archive is

worth 15% of the student's team component grade, or 6% of the student's overall grade.

9.4.6 Concept Development Assignments

During the earlier stages of the design process, ECE 477 student teams are expected to complete a number of concept development assignments. These assignments are listed below:

- Functional Specification (#2)
- Component Analysis (#5)
- Bill of Materials (#7)

The purpose of these assignments is to help the team determine global design aspects and requirements of their projects, and these assignments are to be completed by and with input from the entire team. Assignments 5 and 6, though separate items, are graded as a single item. Completion of the functional specification is worth 5% of the student's team grade and completion of the component analysis and bill of materials is worth 5% of the student's team grade, for a total of 10% of the student's team grade or 4% of their overall grade.

9.4.7 Educational (“Senior Design”) Report

To satisfy educational requirements of ECE 477, student teams are expected to complete a senior design educational summary at the end of the senior design semester. This report is used to describe the educational development of student teams over the course of their ECE 477 senior design semester. The senior design educational summary is subject to the late assignment policy defined in section 9.6. The senior design educational summary is worth 5% of the student's team component grade, or 2% of the student's overall grade.

9.4.8 PCB Completion and Submission

ECE 477 requires the design and fabrication of a printed circuit board (PCB); students are responsible for ordering their own individual PCBs. PCB Submission and Completion is a gradable item which assesses the ability of student teams to submit their printed circuit board for fabrication in a timely manner, to ensure completion of hardware integration and course objectives. PCB completion and submission is worth 5% of the student's team component grade, or 2% of the student's overall grade.

9.5 Description of Individual Components

The individual component of a student's grade is responsible for 60% of their overall grade. The elements of the individual component score are listed out in detail in the subsections below.

9.5.1 Progress Reports

Students are expected to maintain a progress report over the course of their semester within ECE 477. Progress reports are brief (generally 1 page or less) reports which are evaluated by course staff frequently throughout the semester. A 60% or better average score on progress reports is required to satisfy an ABET outcome; this is described in further detail in section 9.3. Course policies regarding progress reports are detailed further in the Progress Report Policy, available on the ECE 477 course website. Performance on progress reports is worth 20% of the student's individual component grade, or 12% of the student's overall grade.

9.5.2 Individual Contribution

ECE 477 is a team-based course in which individual student efforts contribute to the overall success or failure of an ECE 477 student team. The individual contribution score is an assessment by the course staff of how much a student contributed and helped or hindered their ECE 477 team. Level of individual contribution is worth 20% of the student's individual component grade, or 12% of the student's overall grade.

9.5.3 Design Component Report

The following ECE 477 assignments are considered design component reports for the purposes of the class:

- Software Overview (#3)
- Electrical Overview (#4)
- Mechanical Overview (#6)
- Software Formalization (#8)

Each ECE 477 student team is required to complete one copy of each of these assignments, and each assignment is to be completed by a different member of the ECE 477 team. A score of 60% or better score on the design component report is required to satisfy an ABET outcome; this is described in further detail in section 9.3. The design component reports are subject to the late assignment policy defined in section 9.6. The design component report is worth 15% of the student's individual component grade, or 9% of the student's overall grade.

9.5.4 Professional Component Report

The following ECE 477 assignments are considered professional component reports for the purposes of this class:

- Legal Analysis (#9)
- Reliability and Safety Analysis (#10)
- Ethical/Environmental Impact Analysis (#11)
- User Manual (#12)

Each ECE 477 student team is required to complete one copy of each of these assignments, and each assignment is to be completed by a different member of the ECE 477 team. A score of 60% or better score on the professional component report is required to satisfy an ABET outcome; this is described in further detail in section 9.3. The design component reports are subject to the late assignment policy defined in section 9.6. The professional component report is worth 15% of the student's individual component grade, or 9% of the student's overall grade.

9.5.5 Class Attendance and/or Participation

Clicker quizzes will be routinely used to encourage attendance and attention in ECE 477 lectures. Students must be ***physically present*** to earn the associated class participation credit – no substitution will be allowed. ***It will be considered "cheating" for someone to use the iClicker of another student to "fake" that student's class participation.*** Class participation exercises are cumulatively worth 10% of the individual component grade, or 6% of the student's overall grade.

9.5.6 Mandatory Lab Session Attendance

In the interest of ensuring students are held accountable for project work and staff are up to date

on student project issues and progress, weekly mandatory lab sessions are held in which ECE 477 course staff meet with students. During these sessions, students are expected to detail their progress concerning their projects and homework assignments. Students are expected to attend their mandatory lab sessions and attendance is taken; failure to attend a minimum of 80% of these mandatory sessions may result in course failure **(i.e., Don't Miss More Than Two Labs!)**. Mandatory lab session attendance is worth 10% of a student's individual grade, or 6% of the student's overall grade.

9.5.7 Confidential Teammate Reviews

During the midterm and final portions of an ECE 477 semester, feedback on student performance is provided in the form of confidential teammate reviews filled out by student team members. The midterm and final confidential peer reviews are cumulatively worth 5% of the student's individual component grade, or 3% of the student's overall grade.

9.5.8 Design Review and Final Presentation Peer Evaluations

During the midterm design review and final presentations, feedback on student presentation performance is provided in the form of peer evaluations. The midterm design review and final presentation peer evaluations are cumulatively worth 5% of the student's individual component grade, or 3% of the student's overall grade.

9.6 Late Assignment Penalty

Homework assignments are due by the deadlines described in the course calendar (typically Fridays or Saturdays) at 11:59 PM (midnight). In the event of late assignments, the following penalties are assessed:

a) -10% for every day the assignment is submitted late (rounded up)

b) If an assignment is more than 3 days late, the ECE 477 course staff may grade it at their discretion.

Final project deliverables (assignments 13 and 14) are due the Monday of finals week for a given ECE 477 semester at 5:00 pm. Late penalties are assessed in accordance with the late policy outlined above. It should be noted that late materials WILL NOT be accepted after 5:00 pm on the Thursday of finals week.

9.7 Description of Bonus Components

In addition to the project and team components, opportunities exist for additional bonus credit. These bonus credit opportunities are elaborated on in the subsections below.

9.7.1 Early Completion Bonus Credit

Student teams who successfully complete their ECE 477 senior design project early may qualify for early completion bonus credit. This is to inspire student teams to work hard and be proactive by working ahead in their senior design course. For each week prior to the final week of the semester that a team completes their project, they will receive an additional +1% bonus credit to their overall grade. This bonus credit is subject to certain conditions, and is awarded at the sole discretion of the ECE 477 course staff.

In order to qualify for early completion bonus credit, a team must successfully demonstrate all of

their final PSSCs (preliminary PSSCs may not be used for this purpose). In addition, all homework assignments and project deliverables must be submitted, with the exception of the Poster, Educational (Senior Design) Report, Final Confidential Peer Review, and Final Project Archive.

9.7.2 Poster and Design Showcase Participation

At the end of the senior design semester, ECE 477 student teams may have the option of participating in a symposium known as the Spark Challenge. Student teams approved by course instructional staff will become eligible for bonus credit. If selected and agreed upon, the team is then required to produce a poster detailing their senior design projects. The senior design posters are used to present ECE 477 to the general public, as well as for promotional materials for ECE 477 used by the course staff and Purdue School of Electrical Engineering. Spark Challenge participation, along with a completed poster, is worth an additional 2% bonus credit to participating students' grades.

9.7.3 Design Bonus Contract Credit

ECE 477 requires students to design and build a preliminary hardware prototype of a project. Depending on the particulars of a student project, students may have the opportunity to receive bonus credit for going above and beyond standard hardware design requirements for ECE 477. Please contact course staff to see if a design bonus contract may be assessed.

9.8 Campus Emergencies

In the event of a major campus emergency, course requirements, deadlines, and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances beyond the instructor's control. Should such an emergency occur, information will be posted in the ECE 47700 Brightspace Course Announcements.

10.0 Additional Course Information and Policies

Course Title: ECE 47700 Digital Systems Senior Project
CRNs: 37776, 38075, 62147/68480/26019/28699/30958
Lecture: TR - 4:30-5:20 pm in MSEE B012
Labs: Section 4: T 8:30-10:20 am in BHEE 007
Section 5: W 3:30-5:20 pm in BHEE 007
Section 8: W 9:30-11:20 am in BHEE 007
Section 9: T 11:30-1:20 pm in BHEE 007
Section 10: T 2:30-4:20 pm in BHEE 007
Lecture and Lab: Face-to-Face
4 Credit Hours

Course Website: www.engineering.purdue.edu/ece477

Prerequisites:

A minimum grade of D- is required in the following courses.
ECE 20100, 20200, 20700, 20800, 25500, 27000, 30100, 30200, 31100, 36200, 36400, 36800
These courses may not be taken concurrently with ECE 477.

10.1 Communication:

For questions, first ask your teammates on the Team communication app you have chosen (slack, WeChat, Team section in Piazza, etc.). Next ask your assigned TA if they are included in your Team communication group. Next post on the course Piazza. Finally, if you still do not have an acceptable answer, send an email to ECE477@ecn.purdue.edu. You also may attend any of the in person or virtual office hours offered for this course (calendar to be posted soon).

10.2 Additional Attendance Policies:

This course follows Purdue's academic regulations regarding attendance, which states that students are expected to be present for every meeting of the classes in which they are enrolled. When conflicts or absences can be anticipated, such as for many University-sponsored activities and religious observations, the student should inform the instructor of the situation as far in advance as possible. For unanticipated or emergency absences when advance notification to the instructor is not possible, the student should contact the instructor as soon as possible by email or phone. When the student is unable to make direct contact with the instructor and is unable to leave word with the instructor's department because of circumstances beyond the student's control, and in cases falling under excused absence regulations, the student or the student's representative should contact or go to the Office of the Dean of Students (ODOS) website to complete appropriate forms for instructor notification. Under academic regulations, excused absences may be granted **by ODOS** for cases of grief/bereavement, military service, jury duty, parenting leave, or emergent or urgent care medical care.
Guidance on class attendance related to COVID-19 are outlined in the Protect Purdue Pledge for Fall 2021 on the Protect Purdue website.

If you must miss class at any point in time during the semester, please reach out to course staff via email (ece477@ecn.purdeu.edu) so that we can communicate about how you can maintain your academic progress. For COVID-19 concerns, please see the **Fall 2022: What you need to know guidance published July 27**. If you find yourself too sick to progress in the course, notify your adviser and notify me via email or Brightspace. We will make arrangements based on your particular situation.

10.3 Academic Integrity:

Academic integrity is one of the highest values that Purdue University holds. Individuals are encouraged to alert university officials to potential breaches of this value by either emailing integrity@purdue.edu or by calling 765-494-8778. While information may be submitted anonymously, the more information is submitted the greater the opportunity for the university to investigate the concern. More details are available on our course Brightspace under University Policies.

10.4 Nondiscrimination:

Purdue University is committed to maintaining a community that recognizes and values the inherent worth and dignity of every person; fosters tolerance, sensitivity, understanding, and mutual respect among its members; and encourages each individual to strive to reach his or her potential. In pursuit of its goal of academic excellence, the University seeks to develop and nurture diversity. The University believes that diversity among its many members strengthens the institution, stimulates creativity, promotes the exchange of ideas, and enriches campus life. A hyperlink to Purdue's full Nondiscrimination Policy Statement is included in our course Brightspace under University Policies.

10.5 Accessibility:

Purdue University is committed to making learning experiences accessible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Disability Resource Center at: drc@purdue.edu or by phone: 765-494-1247.

10.6 Mental health / Wellness:

If you find yourself beginning to feel some stress, anxiety and/or feeling slightly overwhelmed, try WellTrack**.** Sign in and find information and tools at your fingertips, available to you at any time.

If you need support and information about options and resources, please contact or see the Office of the Dean of Students. Call 765-494-1747. Hours of operation are M-F, 8 am- 5 pm.

If you find yourself struggling to find a healthy balance between academics, social life, stress, etc., sign up for free one-on-one virtual or in-person sessions with a Purdue Wellness Coach at RecWell. Student coaches can help you navigate through barriers and challenges toward your goals throughout the semester. Sign up is free and can be done on BoilerConnect.

If you're struggling and need mental health services: Purdue University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of mental health support, services are available. For help, such individuals should contact Counseling and Psychological Services (CAPS) at 765-494-6995 during and after hours, on weekends and holidays, or by going to the CAPS office on the second floor of the Purdue University Student Health Center (PUSH) during business hours. The CAPS website also offers resources specific to situations such as COVID-19.

10.7 Basic needs:

Any student who faces challenges securing their food or housing and believes this may affect their performance in the course is urged to contact the Dean of Students for support. There is no appointment needed and Student Support Services is available to serve students 8 a.m.-5 p.m. Monday through Friday. Considering the significant disruptions caused by the current global crisis as it relates to COVID-19, students may submit requests for emergency assistance from the Critical Need Fund

Appendix A - Guidelines for Academic Integrity

In a society that increasingly questions the value of higher education, upholding academic integrity takes on added significance. The time and effort necessary to champion high expectations of academic integrity are well understood, and the University is in full support of faculty and instructors who uphold these standards. Please consider these five steps for your class.

1. *Define academic dishonesty for your class in your syllabus and emphasize it on the first day of class. The OSRR website offers a faculty guide on responding to academic dishonesty. Revisit your expectations at key junctures of the semester (e.g., before an exam or term project).*
2. *Provide greater clarity to students about what is acceptable and unacceptable. Some classes routinely use team assignments and encourage collaboration for projects, labs, or homework. Yet at other times of the term, students are expected to work independently. Be very clear about your expectations for each assignment.*
3. *Students should be told prior to – and as part of – the instructions on each test what is acceptable in terms of notes, phones, calculators, etc. From class to class our practices vary widely so, here again, it's important to be very clear in your expectations.*
4. *Define penalties that will be enforced for academic dishonesty. One example might be:*

   > Incidents of academic misconduct in this course will be addressed by the course instructor and referred to the Office of Student Rights and Responsibilities (OSRR) for review at the university level. Any violation of course policies as it relates to academic integrity will result minimally in a failing or zero grade for that particular assignment, and at the instructor's discretion may result in a failing grade for the course. In addition, all incidents of academic misconduct will be forwarded to OSRR, where university penalties, including removal from the university, may be considered.

5. *At a minimum, if you penalize a student's grade by deducting points, report the instance of scholastic dishonesty using the OSRR reporting form. Reporting all incidents helps to ensure consistent treatment both at the course level and across the institution. Staff members from OSRR are available to consult on an individual basis. Their phone is 765-494-1250.*
6. *While faculty and instructors have raised concerns about student academic integrity, students have indicated that some instructors appear reluctant to uphold academic standards. Be clear in your syllabus on the steps you will take in your class to uphold academic integrity. In addition, students should be made aware that they can report issues of academic integrity that they observe, and may do so anonymously, through the OSRR by calling 765-494-8778 or emailing integrity@purdue.edu.*

Appendix B: Emergency Preparedness face-to-face

1. Prior to the first day of class, obtain a copy of the building emergency plan for each building in which you will be teaching. Note the evacuation route and assembly area, as well as the shelter in place locations. BEPs are located on the Emergency Preparedness website.
2. On the first day of class, the following information is required to be presented to students:
   1) As we begin this semester, I want to take a few minutes and discuss emergency preparedness. While COVID-19 is currently a major focus of our campus health and safety preparations, we must also take time to be prepared for other possible emergencies as we would in any semester. Purdue University is a very safe campus and there is a low

probability that a serious incident will occur here at Purdue. However, just as we receive a "safety briefing" each time we get on an aircraft, we want to emphasize our emergency procedures for evacuation and shelter-in-place incidents. Our preparedness will be critical IF an unexpected event occurs!

2) Emergency preparedness is your personal responsibility. Purdue University is actively preparing for natural disasters or human-caused incidents with the ultimate goal of maintaining a safe and secure campus. Let's review the following procedure
    - For any emergency text or call 911.
    - There are more than 300 Emergency Telephones (aka blue lights) throughout campus that connect directly to the Purdue Police Department (PUPD). If you feel threatened or need help, push the button and you will be connected right away.
    - If we hear a fire alarm, we will immediately evacuate the building and proceed to__Paved area West of MSEE Building_ (location). Do not use the elevator. Go over the evacuation route (see specific Building Emergency Plan).
    - If we are notified of a Shelter in Place requirement for a tornado warning we will stop classroom or research activities and shelter in the lowest level of this building away from windows and doors. Our preferred location is _BHEE 007 (Stay in place)_.
    - If we are notified of a Shelter in Place requirement for a hazardous materials release, we will shelter in our classroom shutting any open doors and windows.
    - If we are notified of a Shelter in Place requirement for an active threat such as a shooting, we will shelter in a room that is securable preferably without windows. Our preferred location is _____.
    - **(NOTE: Each building will have different evacuation & shelter locations. The specific Building Emergency Plan will provide specific locations and procedures)**

Appendix C: Fall 2022 Course Calendar – Weeks 1 through 8

ECE 47700 - Fall 2022	Weeks 1-8	Tenative Schedule - Subject to Change			
Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Week 1					
August 22, 2022	August 23, 2022	August 24, 2022	August 25, 2022	August 26, 2022	August 27, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 1 Intro to ECE 47700		Lecture 2 Defining Requirements	Due at 11:59pm (I) Progress Report 1 (optional) (I) Participation Quiz 1	Reports Due at 11:59pm (T) A1 - Final Project Proposal
Week 2					
August 29, 2022	August 30, 2022	August 31, 2022	September 1, 2022	September 2, 2022	September 3, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 3A Hardware Interfacing		Lecture 3B Hardware Interfacing	Due at 11:59pm (I) Progress Report 2 (optional) (T) Create Team Website (I) Participation Quiz 2	Reports Due at 11:59pm (T) A2 - Functional Specification
Week 3					
September 5, 2022	September 6, 2022	September 7, 2022	September 8, 2022	September 9, 2022	September 10, 2022
Labor Day No Classes	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 4A Discrete Components		Lecture 4B Discrete Components	Due at 11:59pm (I) Progress Report 3 (I) Participation Quiz 3	Reports Due at 11:59pm (T) A0 - Revised Initial Project Prop. (I) A3 - Software Overview
Week 4					
September 12, 2022	September 13, 2022	September 14, 2022	September 15, 2022	September 16, 2022	September 17, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 5A Power Design		Lecture 5B Power Design	Due at 11:59pm (I) Progress Report 4 (I) Participation Quiz 4	Reports Due at 11:59pm (I) A4 - Electrical Overview (T) A5 - Component Analysis
Week 5					
September 19, 2022	September 20, 2022	September 21, 2022	September 22, 2022	September 23, 2022	September 24, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 6 Firmware Design		Lecture 7 Hardware Design 1	Due at 11:59pm (I) Progress Report 5 (T) "Locked Down" PSSCs (I) Participation Quiz 5	Reports Due at 11:59pm (I) A6 - Mechanical Overview (T) A7 - Bill of Materials
Week 6					
September 26, 2022	September 27, 2022	September 28, 2022	September 29, 2022	September 30, 2022	October 1, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 8 Hardware Design 2		Lecture 9A PCB Debugging	Due at 11:59pm (I) Progress Report 6 (T) Schematic & PCB Footprints (I) Participation Quiz 6	Reports Due at 11:59pm (I) A8 - Software Formalization
Week 7					
October 3, 2022	October 4, 2022	October 5, 2022	October 6, 2022	October 7, 2022	October 8, 2022
	Man Labs (8:30,11:30,2:30)	Man Labs (9:30,3:30)			
	Lecture 9B PCB Debugging		MDR Lecture Design Review Lecture	Due at 11:59pm (I) Progress Report 7 (T) PCB Layout (I) Participation Quiz 7	Work on Midterm Design Review Presentation
Week 8					
October 10, 2022	October 11, 2022	October 12, 2022	October 13, 2022	October 14, 2022	October 15, 2022
October Break No Classes	October Break No Classes	Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	Due at 11:59pm (I) Progress Report 8 (optional) (I) Midterm Teammate Reviews

Appendix D: Fall 2022 Course Calendar – Weeks 9 through End of Semester

ECE 47700 - Fall 2022	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Week 9	October 17, 2022	October 18, 2022 Man Labs (8:30,11:30,2:30) Lecture 10 PCB Verification & Ordering	October 19, 2022 Man Labs (9:30,3:30)	October 20, 2022 Lecture 11 Soldering Techniques	October 21, 2022 Due at 11:59pm (I) Progress Report 9 (I) Participation Quiz 9	October 22, 2022 Due at 11:59pm (T) PCB Verification & Order
Week 10	October 24, 2022	October 25, 2022 Man Labs (8:30,11:30,2:30) Lecture 12A Legal & Regulatory	October 26, 2022 Man Labs (9:30,3:30)	October 27, 2022 Lecture 12B Legal & Regulatory	October 28, 2022 Due at 11:59pm (I) Progress Report 10 (I) Participation Quiz 10	October 29, 2022 Reports Due at 11:59pm (I) A9 - Legal & Regulatory Analysis
Week 11	October 31, 2022	November 1, 2022 Man Labs (8:30,11:30,2:30) Lecture 13A Reliability & Safety	November 2, 2022 Man Labs (9:30,3:30)	November 3, 2022 Lecture 13B Reliability & Safety	November 4, 2022 Due at 11:59pm (I) Progress Report 11 (I) Participation Quiz 11	November 5, 2022 Reports Due at 11:59pm (I) A10 - Reliability & Safety Analysis
Week 12	November 7, 2022	November 8, 2022 Man Labs (8:30,11:30,2:30) Lecture 14 Ethical Considerations	November 9, 2022 Man Labs (9:30,3:30)	November 10, 2022 Lecture 15 Environmental Concerns	November 11, 2022 Due at 11:59pm (I) Progress Report 12 (I) Participation Quiz 12	November 12, 2022 Reports Due at 11:59pm (I) A11 - Ethical & Environ. Analysis
Week 13	November 14, 2022	November 15, 2022 Man Labs (8:30,11:30,2:30) Lecture 16 Final Steps	November 16, 2022 Man Labs (9:30,3:30)	November 17, 2022	November 18, 2022 Due at 11:59pm (I) Progress Report 13	November 19, 2022 Reports Due at 11:59pm (I) A12 - User Manual
Week 14	November 21, 2022	November 22, 2022	November 23, 2022 Thanksgiving Vacation	November 24, 2022 Thanksgiving Vacation	November 25, 2022 Thanksgiving Vacation	November 26, 2022 Due at 11:59pm (I) Progress Report 14 (optional)
Week 15	November 28, 2022	November 29, 2022	November 30, 2022	December 1, 2022	December 2, 2022 Due at 11:59pm (I) Progress Report 15 (T) A13a - Draft Sr. Des. Report	December 3, 2022
Week 16	December 5, 2022	December 6, 2022	December 7, 2022	December 8, 2022	December 9, 2022 Due before 5pm (T) Final PSSC Checkoffs Due at 11:59pm (I) Progress Report 16	December 10, 2022
Finals Week	December 12, 2022 Due at 11:59pm (T) A13b - Sr. Design Report	December 13, 2022 Final Design Presentations Due after Pres. (I) Pres. Peer Reviews	December 14, 2022 Final Design Presentations Due after Pres. (I) Pres. Peer Reviews	December 15, 2022 Due at 11:59pm (I) Final Teammate Reviews (T) A14 - Project Archive	December 16, 2022	December 17, 2022