Inputs:

- Memory Management Unit Output Address, 32 bits
- Controller_enable_read, Controller_enable_write, 1 bit
- Page_lookup_needed, 1 bit
- MM_page_found, 1 bit
- Clock, 1 bit
- L2_read_complete, L2_write_complete, 1 bit
- MM_read_complete, MM_write_complete, 1 bit
- IOBuf_read_complete, IOBuf_write_complete, 1 bit
- Disk_read_complete, Disk_write_complete, 1 bit

Outputs:

- Address out to CPU, 32 bits
- Reset_N, 1 bit
- MMU_enable, 1 bit
- MM_page_query, 1 bit
- TLB_read, TLB_read, 1 bit
- L2_read_mm, L2_write_mm, 1 bit
- L2_read_cpu, L2_write_cpu, 1 bit
- MM_read_io, MM_write_io, 1 bit
- MM_read_cache, MM_write_cache, 1 bit
- IOBuf_read_mm, IOBuf_write_mm, 1 bit
- IOBuf_read_disk, IOBuf_write_disk, 1 bit
- Disk_read, Disk_write, 1 bit

Mechanism:

1. The memory controller initiates a global reset to all modules in the memory hierarchy.

2. The memory controller waits for an enable signal, either read or write, from the CPU controller.

3. The memory controller uses the TLB and MMU to resolve the physical address from the virtual address supplied by the CPU.
    a. If necessary, the memory controller will look up the physical address in the page table in Main memory, writing the result to the TLB.

4. Depending on the operation required (writing to the memory hierarchy or reading from the memory hierarchy), the FSM for the memory controller moves into the read section (specified in the — — - block) or the write section (specified in the ····· block).

5. Once the read or write operation has completed, the FSM returns to the wait state (step two).