

EE105 MiniProject: AM Radio

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December 2013

1 Introduction

2 Circuit Diagram

3 Topology

We used a total of 6 stages in our amplifier. Five common sources and one source follower. Our first decision was to choose topologies to use for amplification. We first considered using a cascode stage because of its characteristically high gain and good frequency response (high bandwidth). However, due to the high gain of the cascode it was very difficult to bias it correctly such that it would not rail. The possible cascode configuration is shown in Figure 2, We need to choose R1 and R2 carefully such that the current being forced by both PMOS and NMOS current mirrors are the same. Otherwise, the small difference in current will reflect as a voltage drop in one of the r_{os} and the high gain of the cascode will amplify and rail this difference.

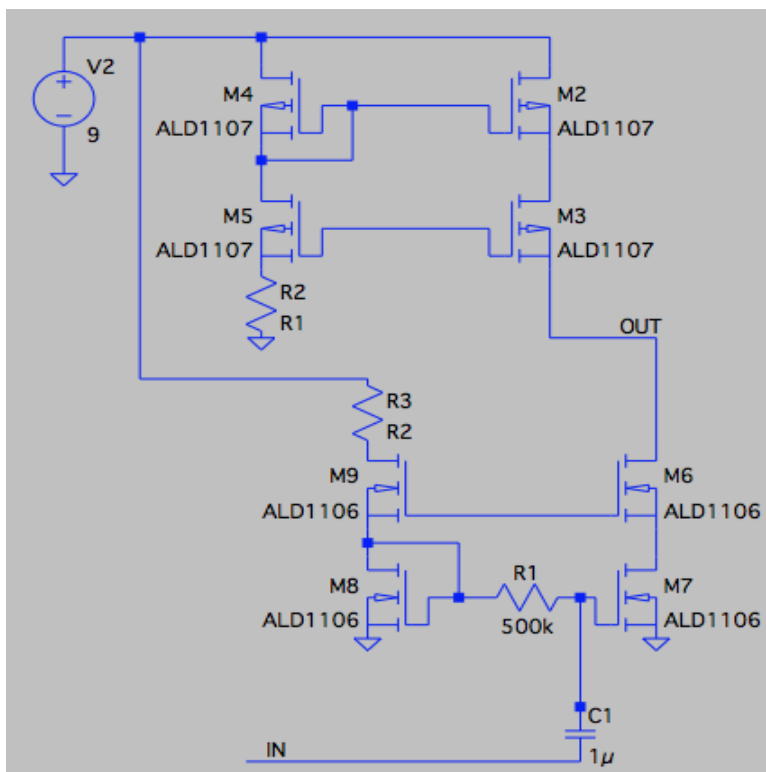


Figure 1: Cascode topology

After some more consideration, we decided to use multiple stages of common source topologies because they

would be much easier to bias than cascode stage. We also decided to use MOSFETs rather than BJTs because while they had lower gain than BJTs (the g_m of MOSFETs is in the order of 10^{-3} compared to the BJT's 0.038), the large gate impedance of MOS proved more attractive since we don't have to worry much about impedance loading between stages. As for the specific MOS, we used the BS170 N-channel MOSFETs because they had high saturation current capacity and, thus, a higher g_m and gain.

Going back to the biasing of the common sources. Our first decision was to choose a desired drain current so that the gain and the $V_{outBIAS}$ would depend on this current. We will go through this calculations in a later section, but it is easy to see that both drain current and $V_{outBIAS}$ are straight forward to bias. Drain current is set by using a current mirror, as shown in Figure 3. Then we choose our drain resistance such that we get a well centered $V_{outBIAS}$. In our case, we chose $R_D = 1000k\Omega$, so the voltage drop on the resistor would be 6V and leave a $V_{outBIAS} \approx 4V$. The gain per common source stage turned out to be low and inconsistent across different BS170, probably due to their mismatch in $\frac{W}{L}$, in fact, it was a gain ranging from 5 to 10. However, since we did not have inter-stage loading gain loss, cascading multiple of this common sources would increase our gain exponentially with a base in the range of 5 to 10. So five stages were enough to reach a gain of over 12500.

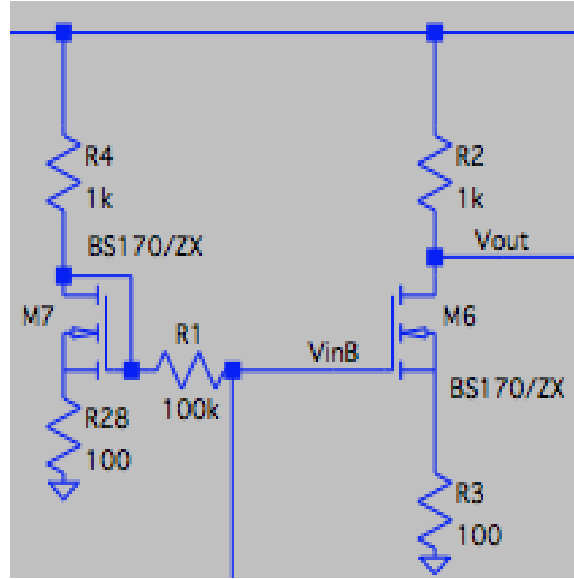


Figure 2: Current Mirror Biasing a common source

Stage	Gate Voltage Bias	Drain Current
Stage 1		
Stage 2		
Stage 3		
Stage 4		
Stage 5		
Stage 6		

4 Hand Calculations and Measurements

Magnitude/Phase Bode Plot

Output Impedance

Bias Voltages/Currents

Power Consumption