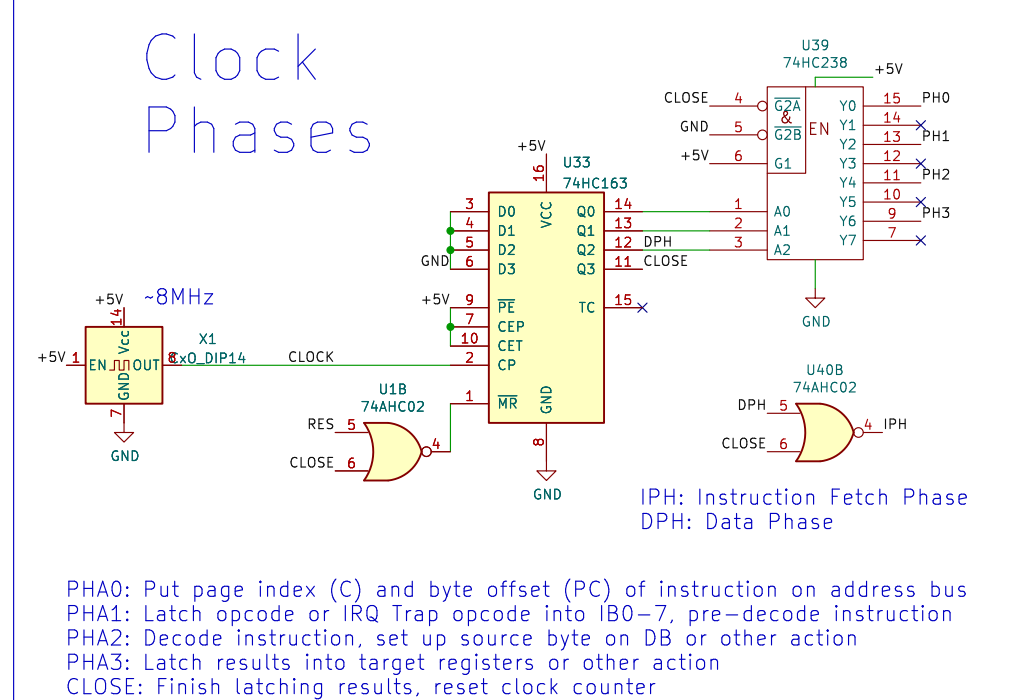


Clock Phases



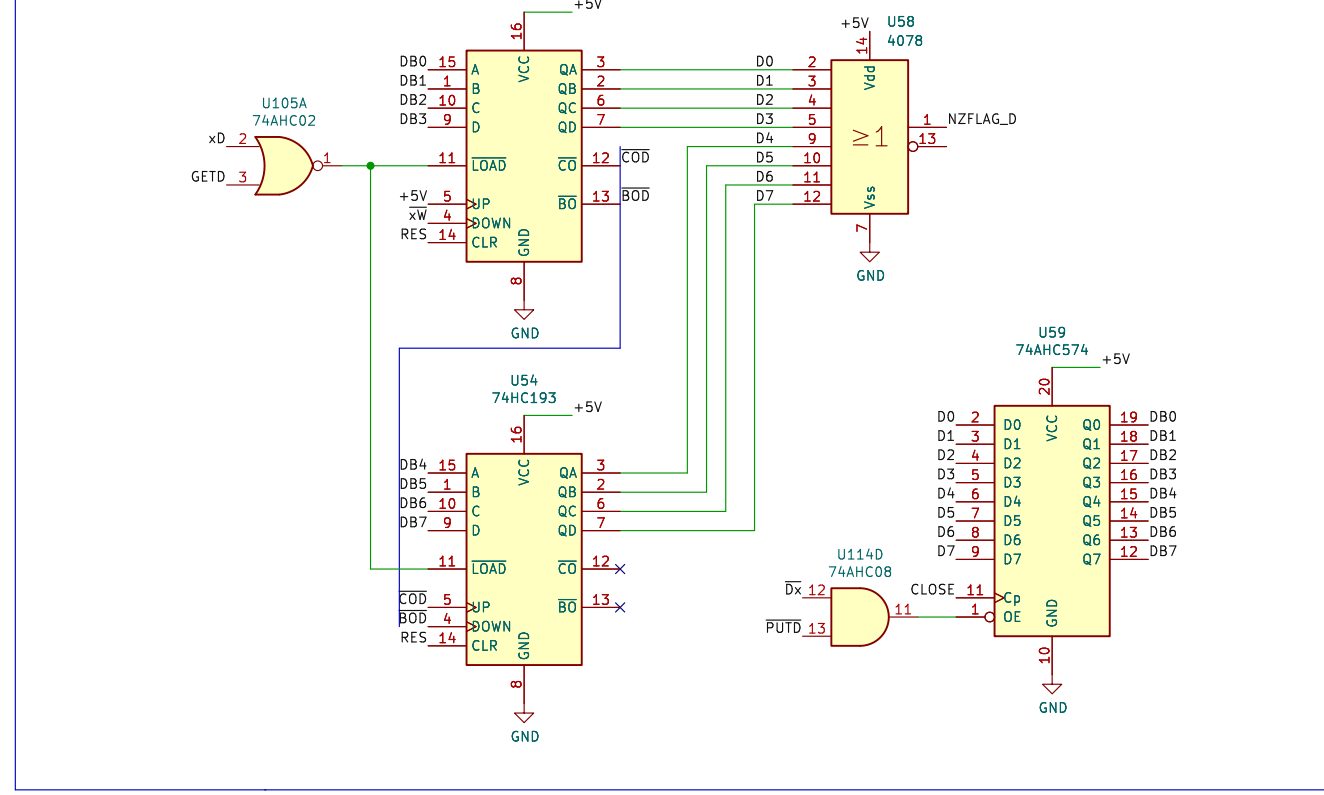
Sonne-8 Microcontroller

Reference Schematics

Rev. Myth

D(OWN) COUNTER

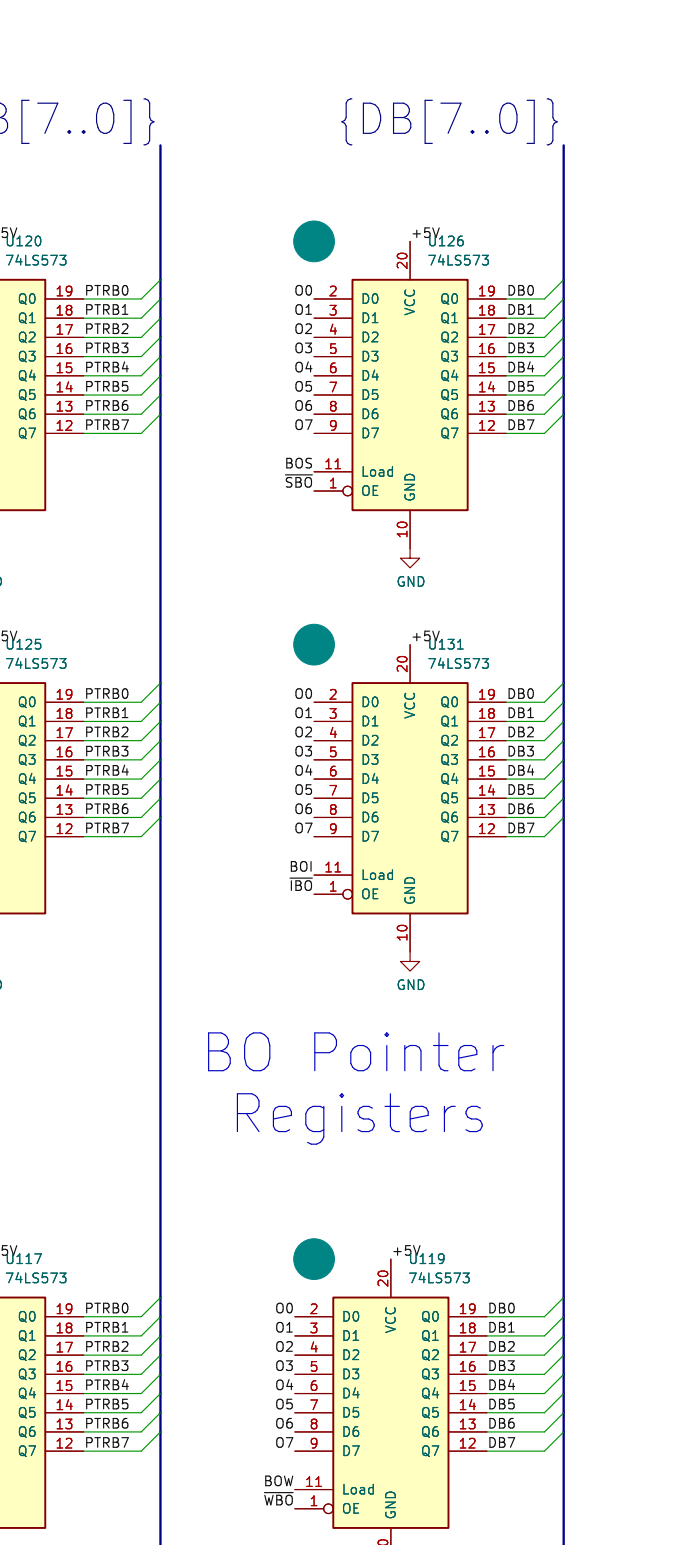
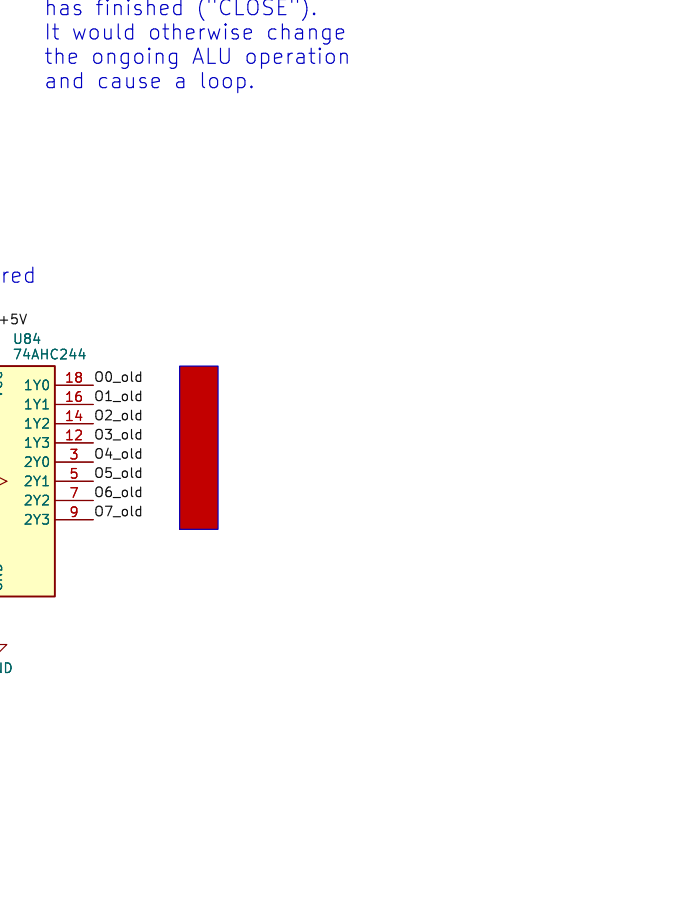
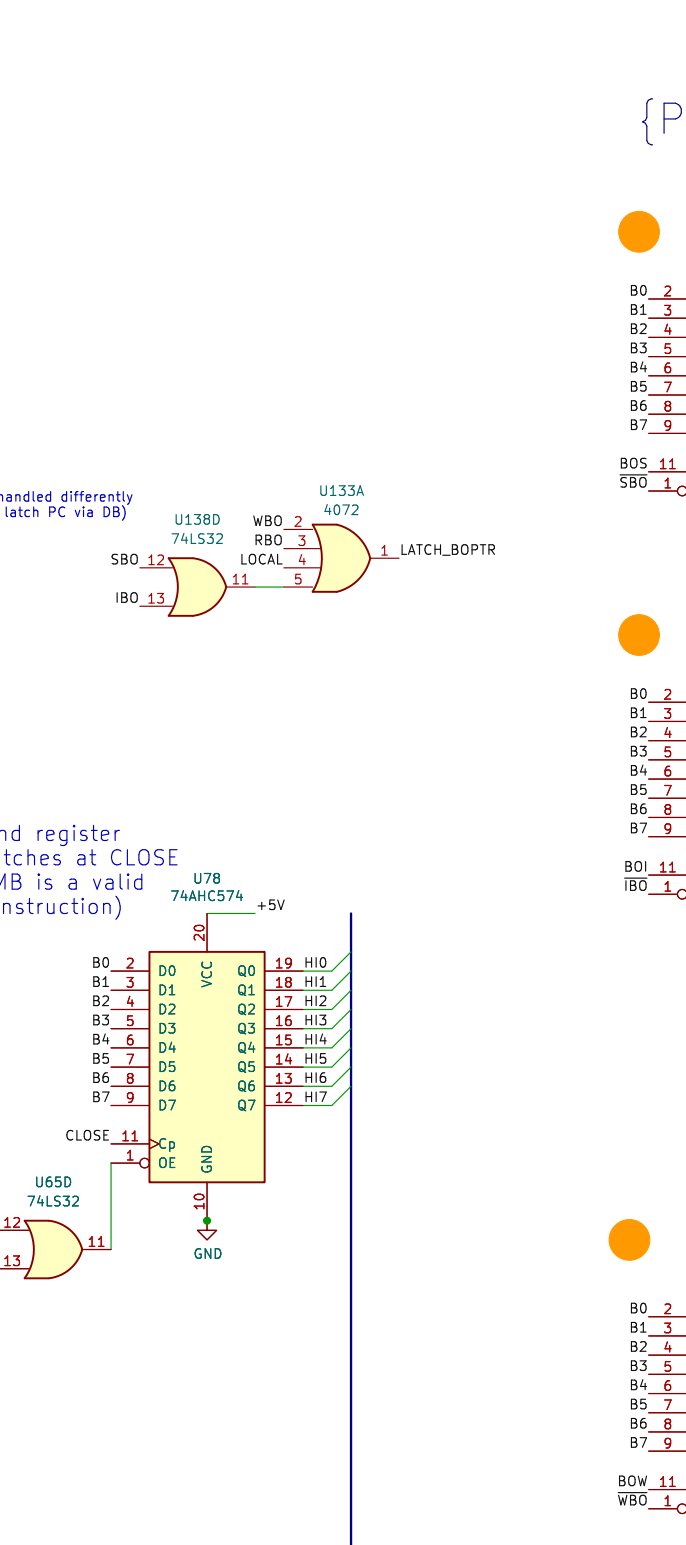
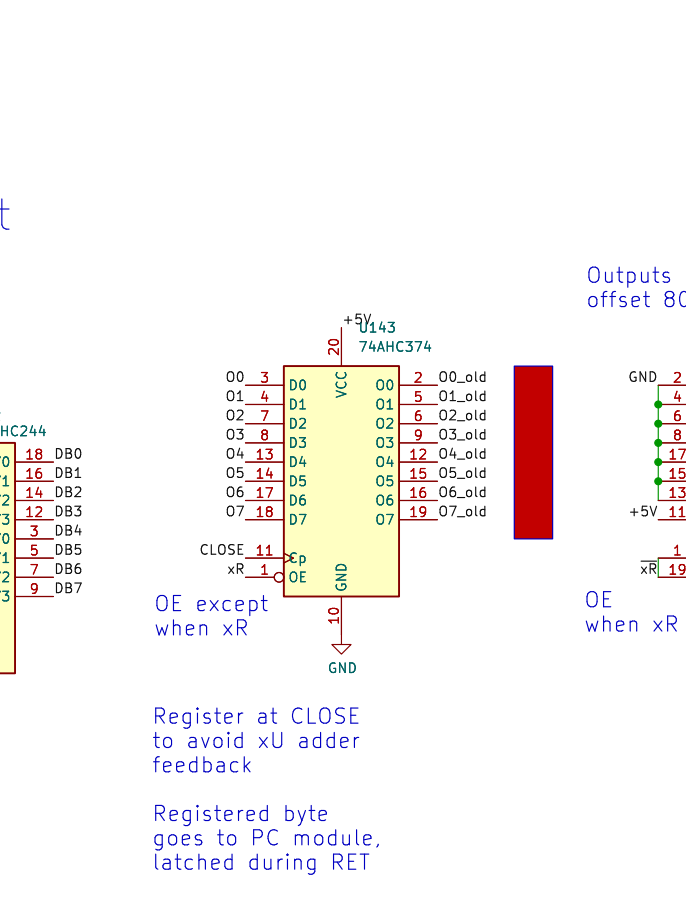
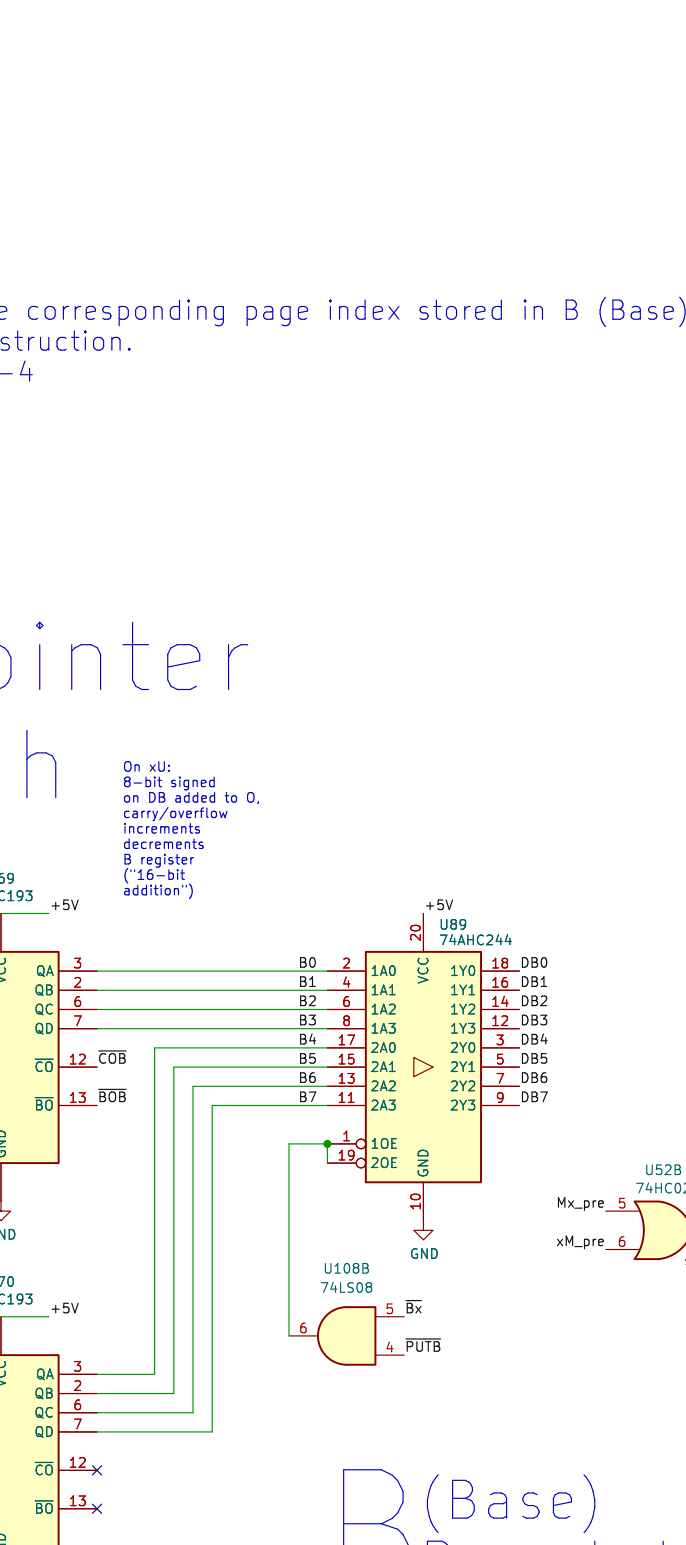
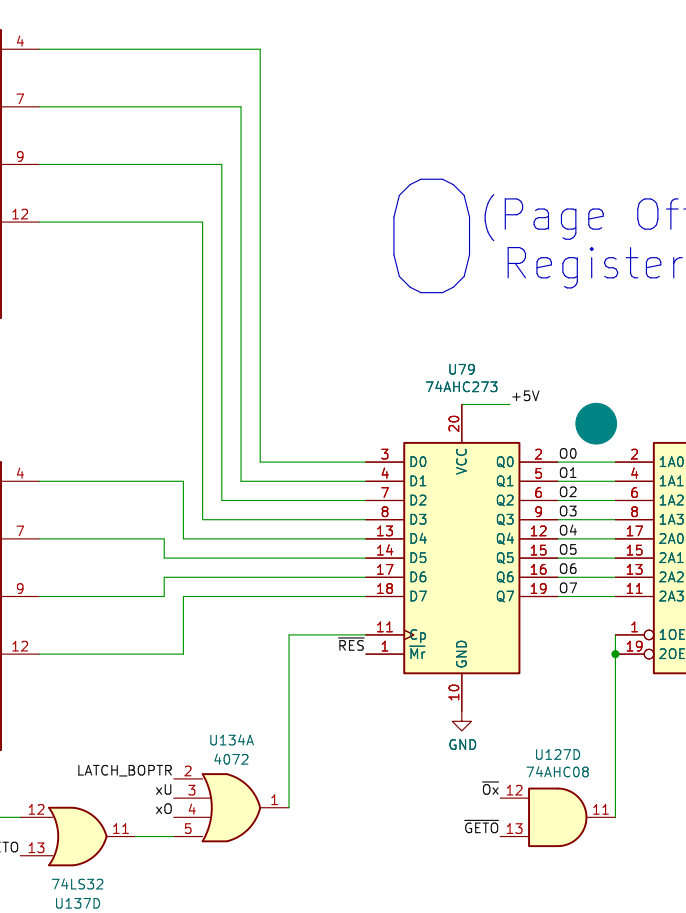
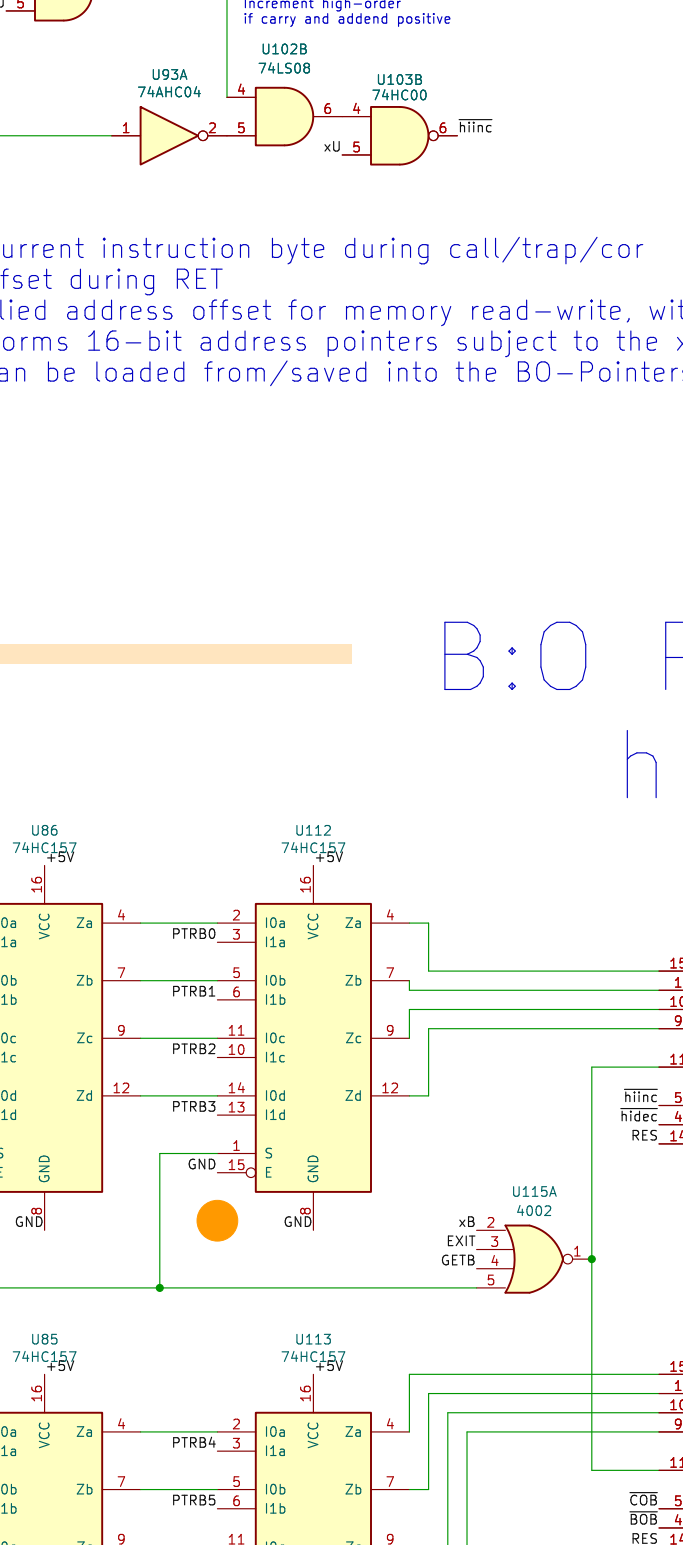
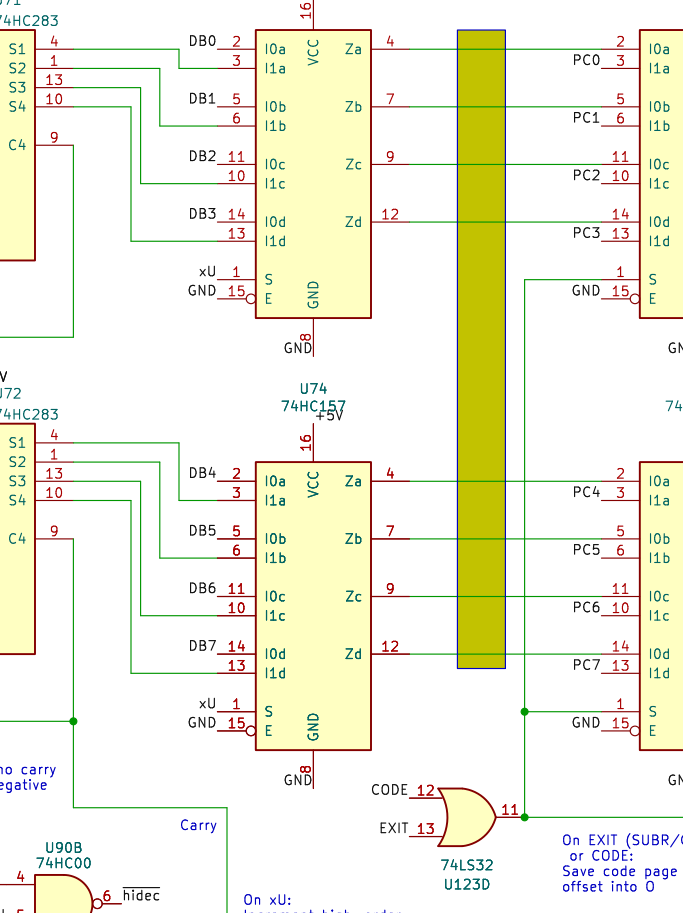
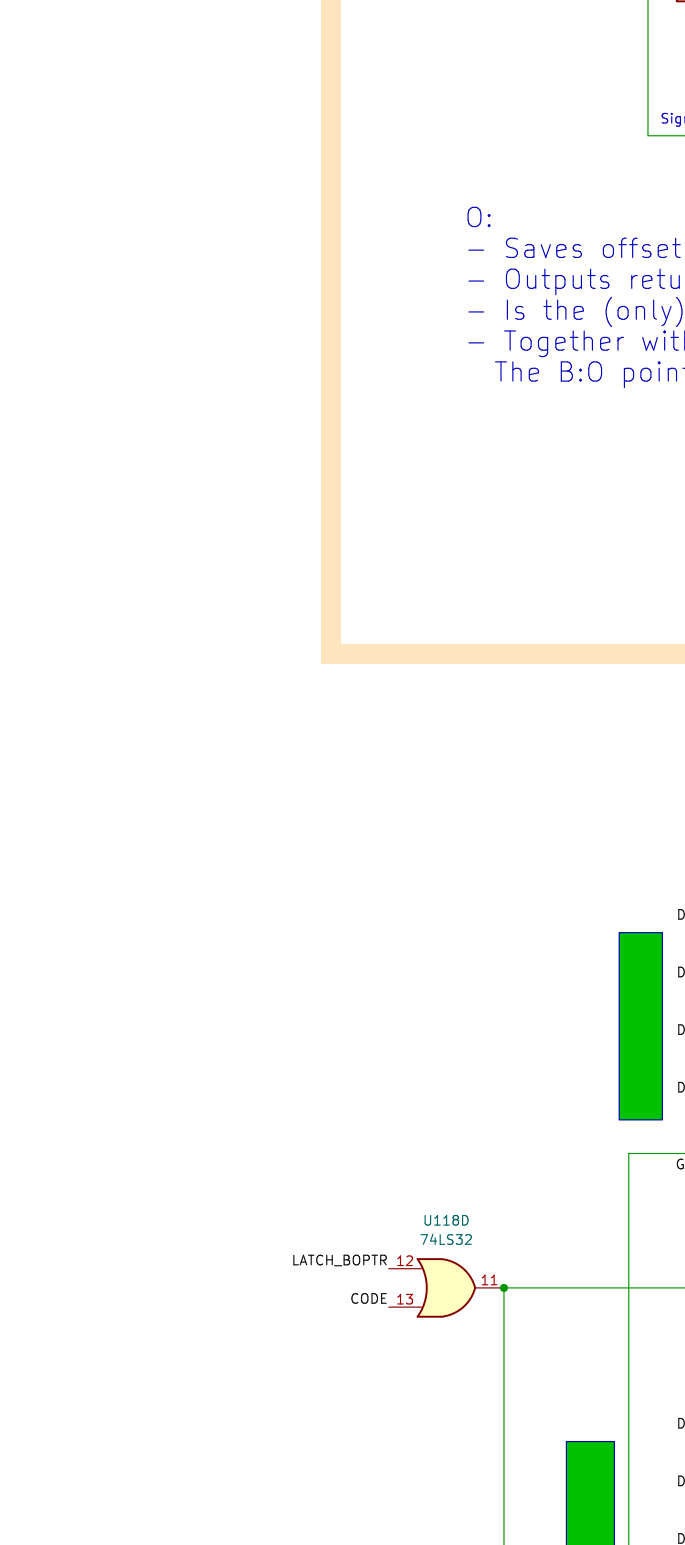
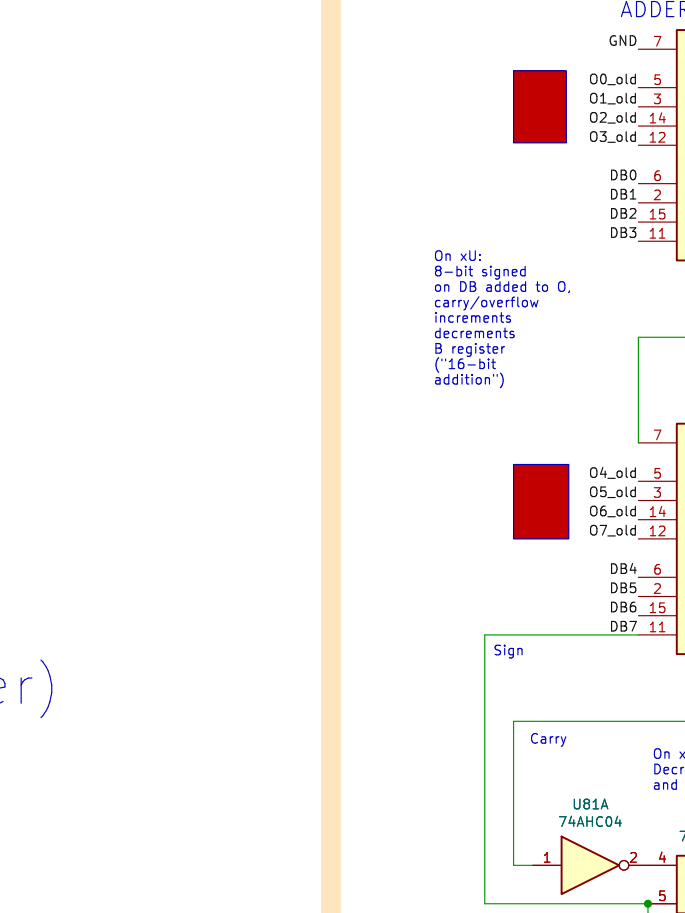
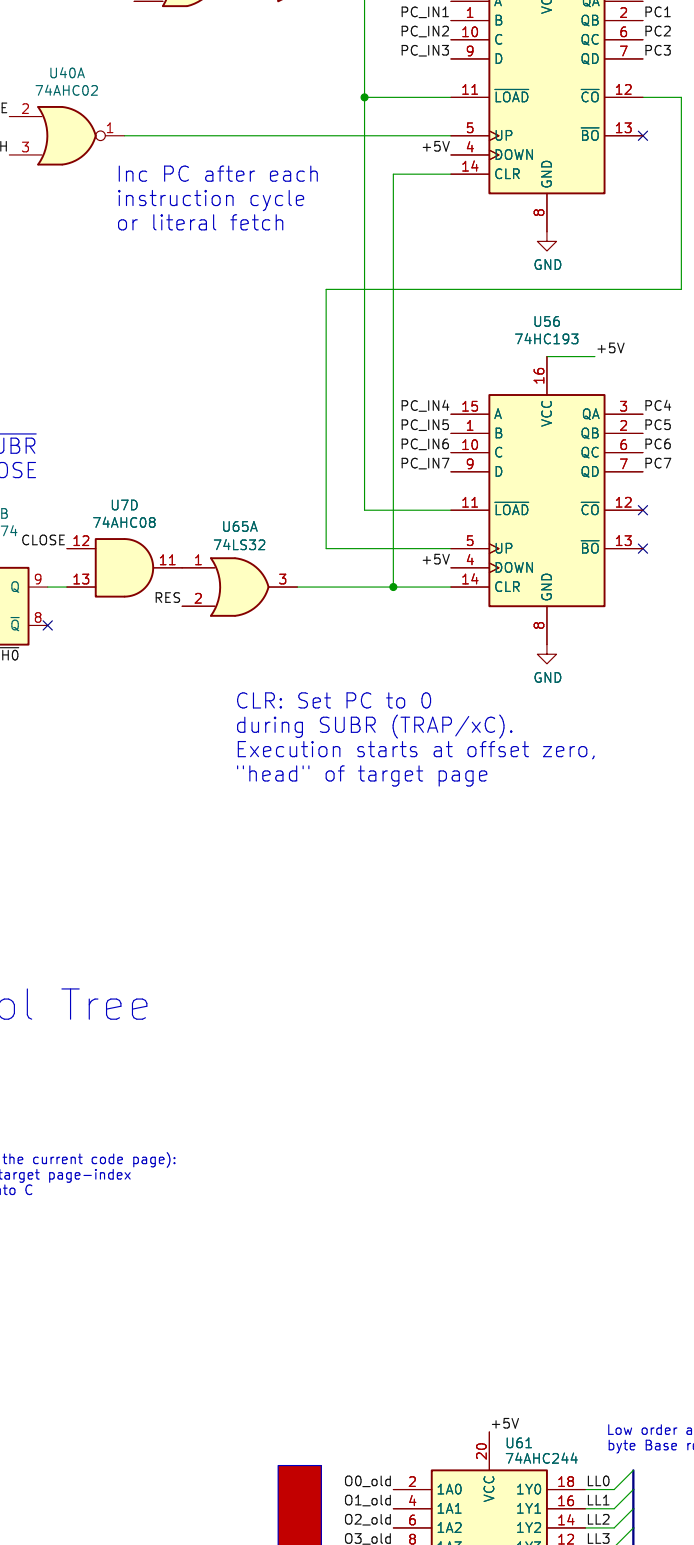
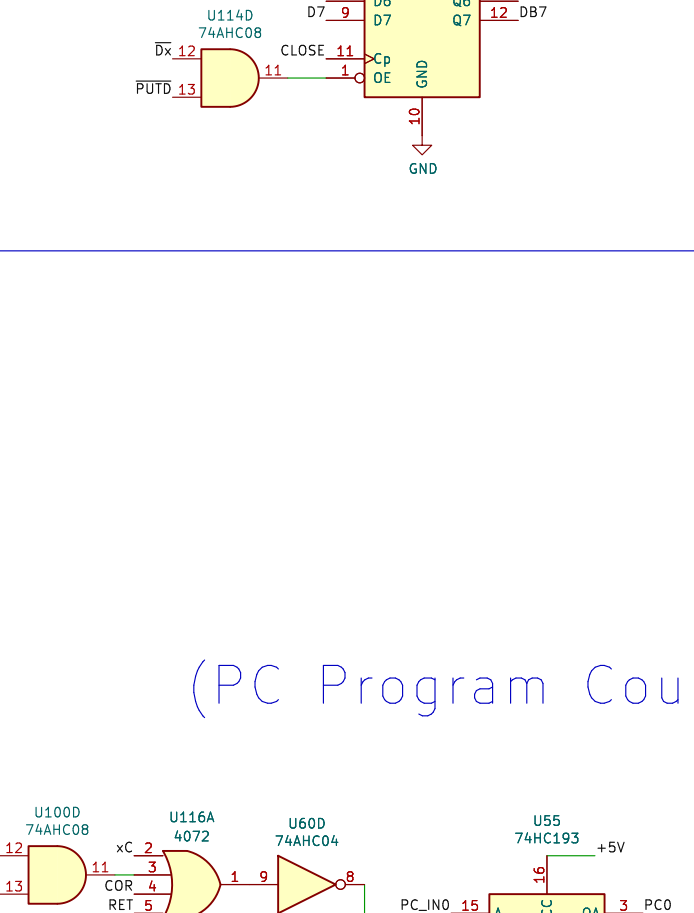
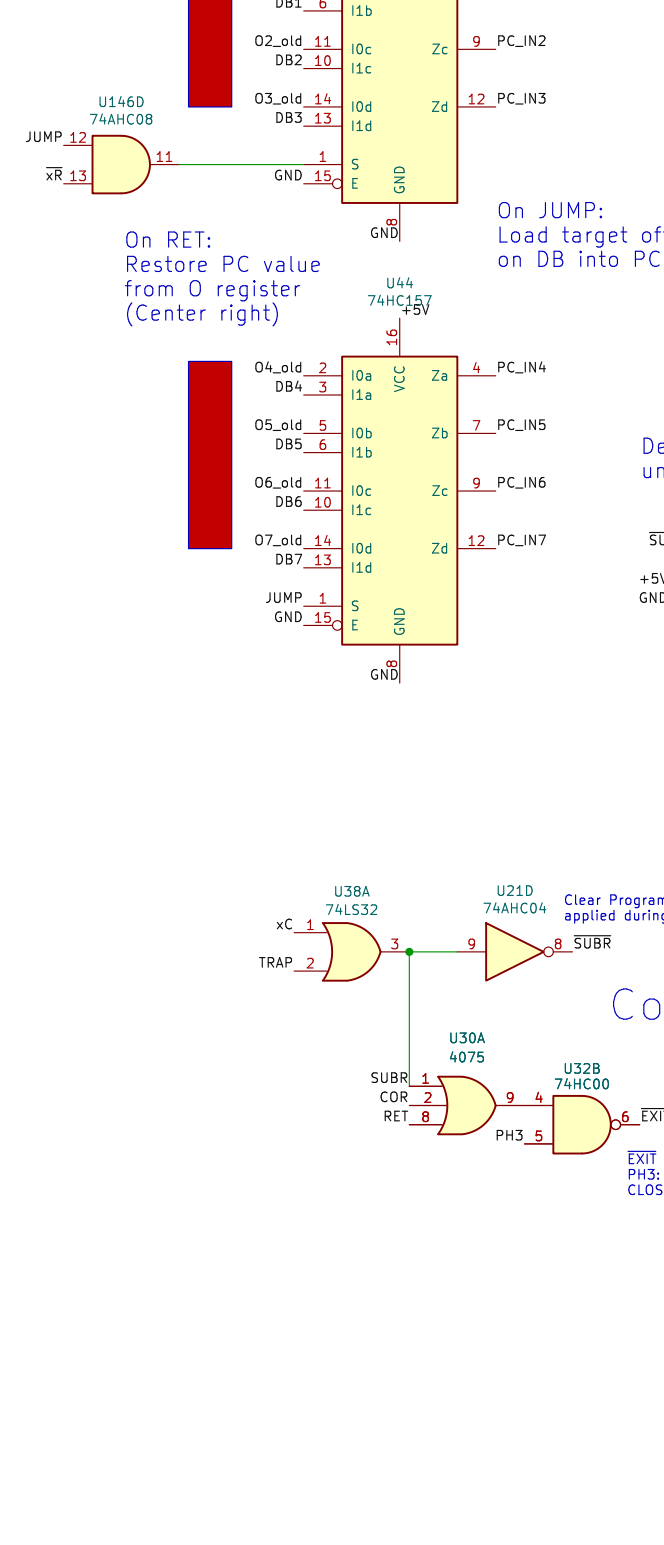
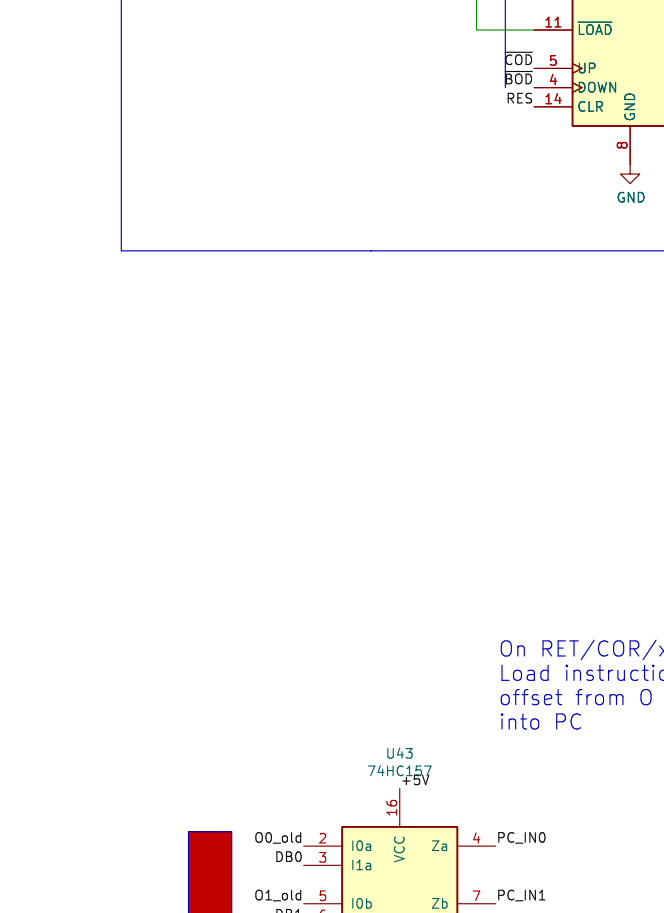
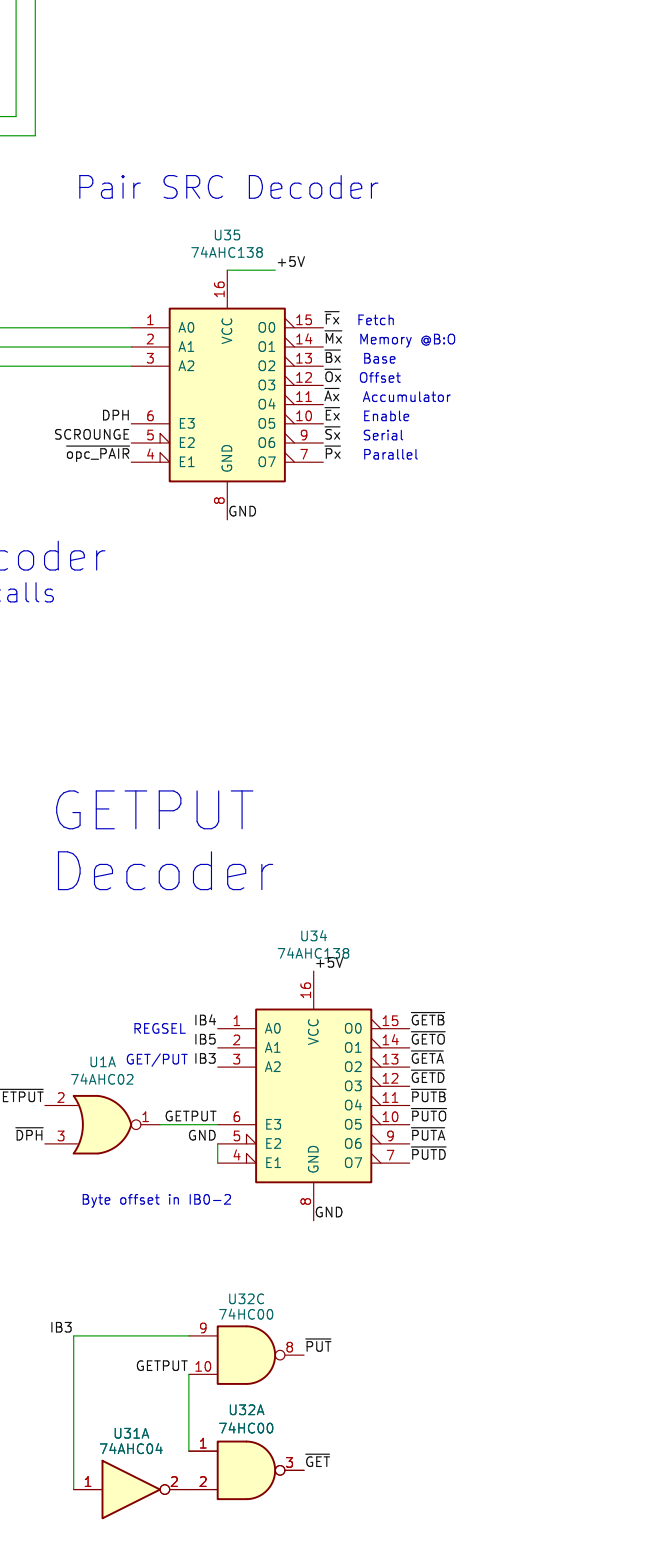
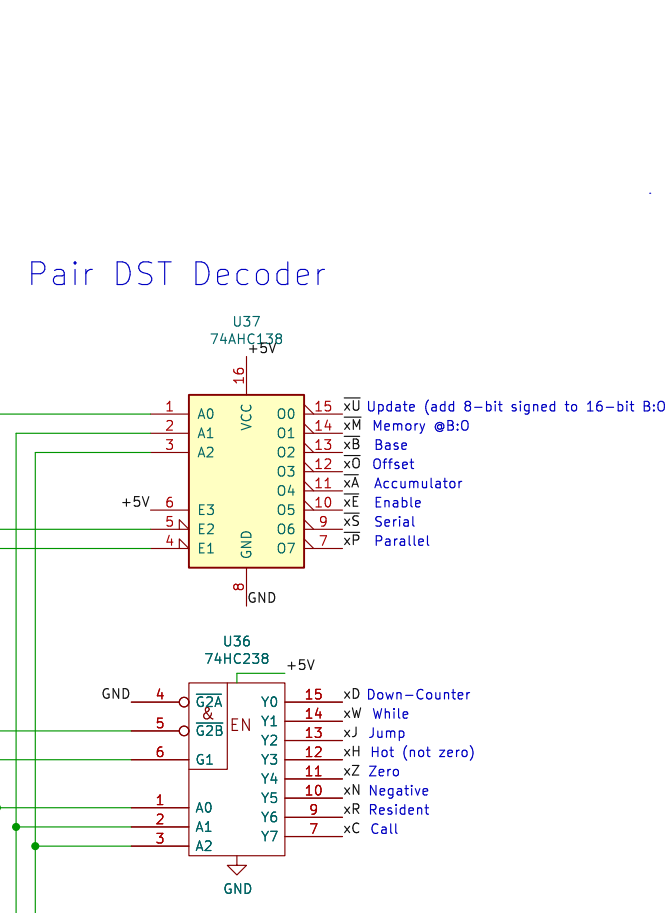
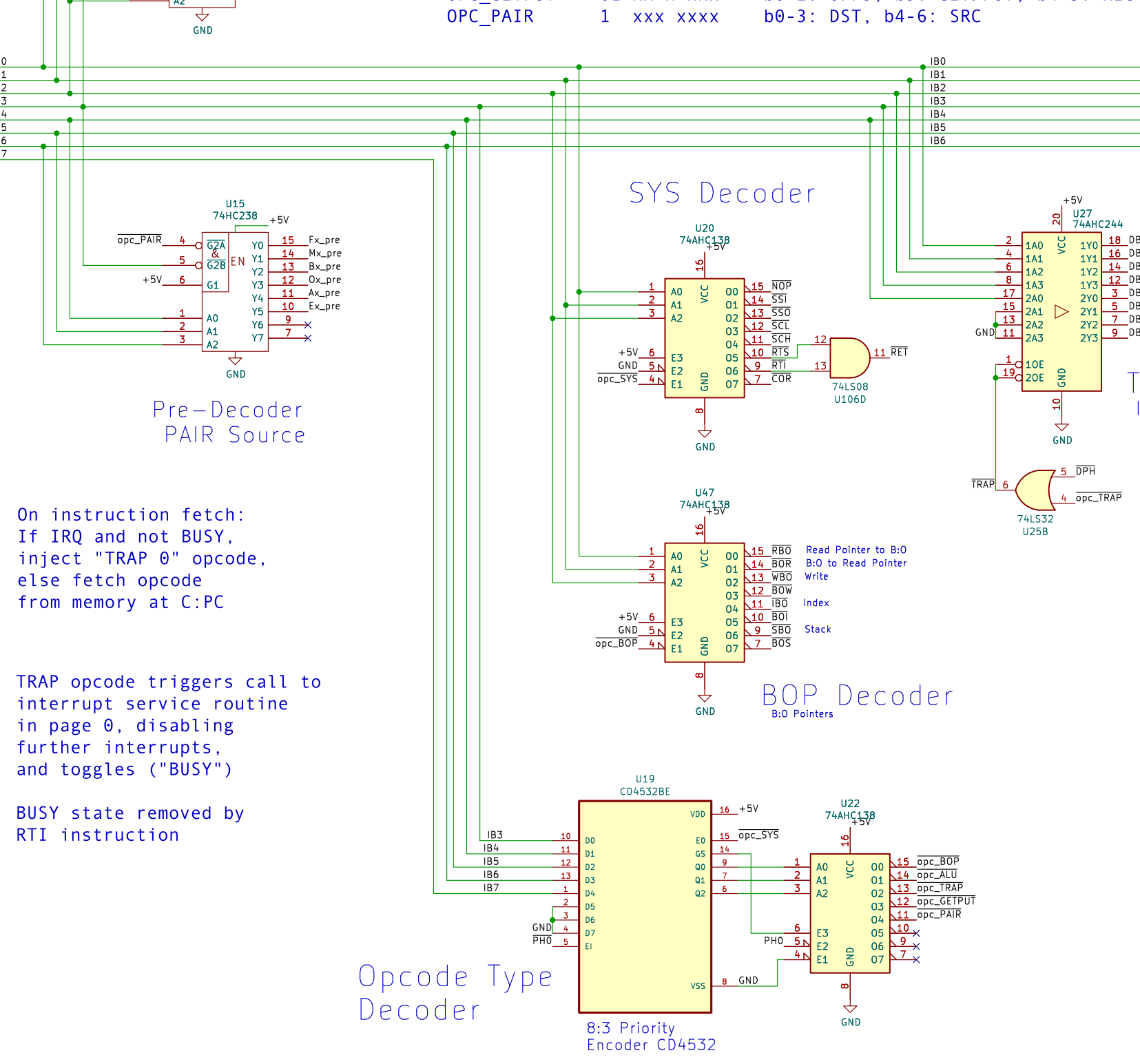
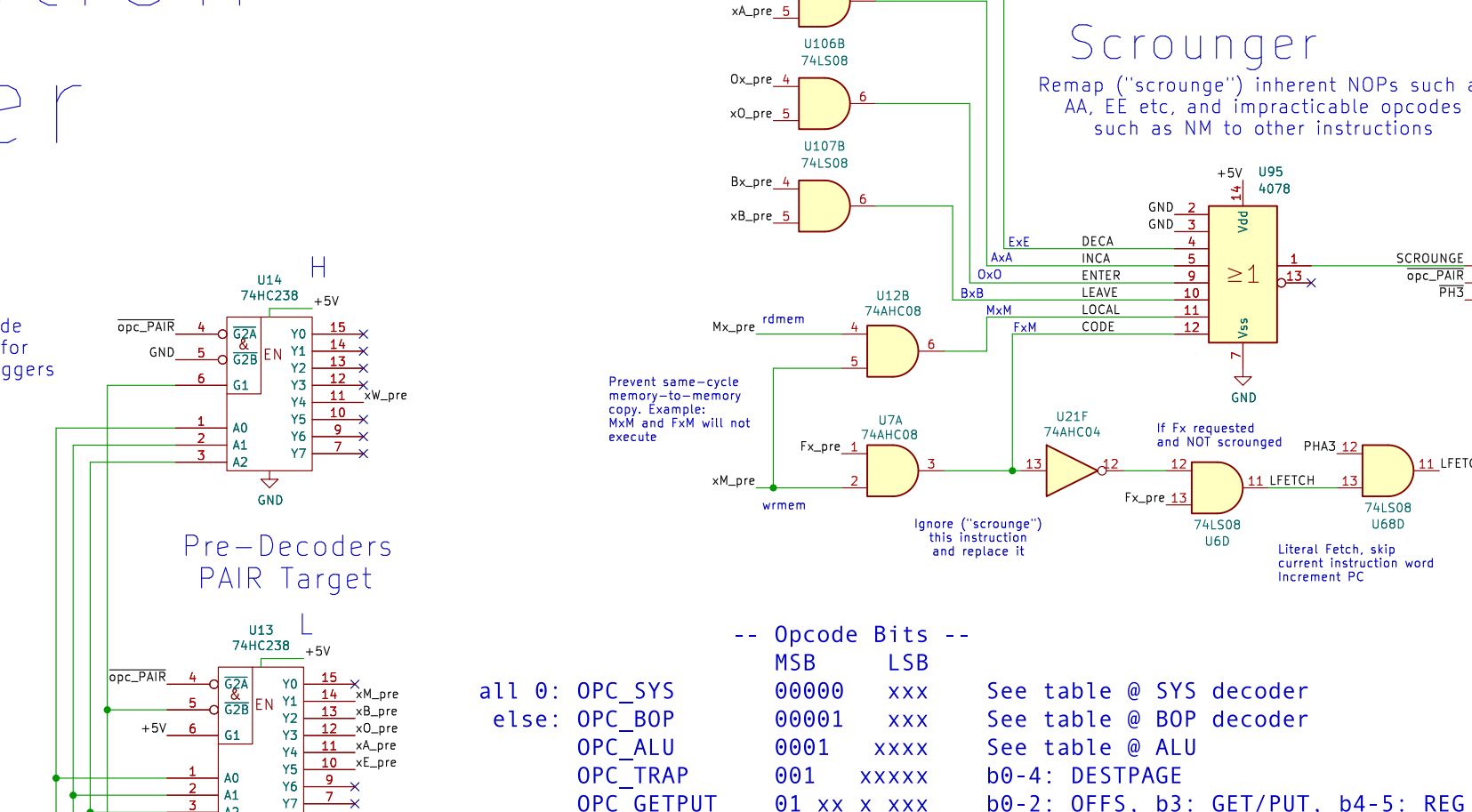
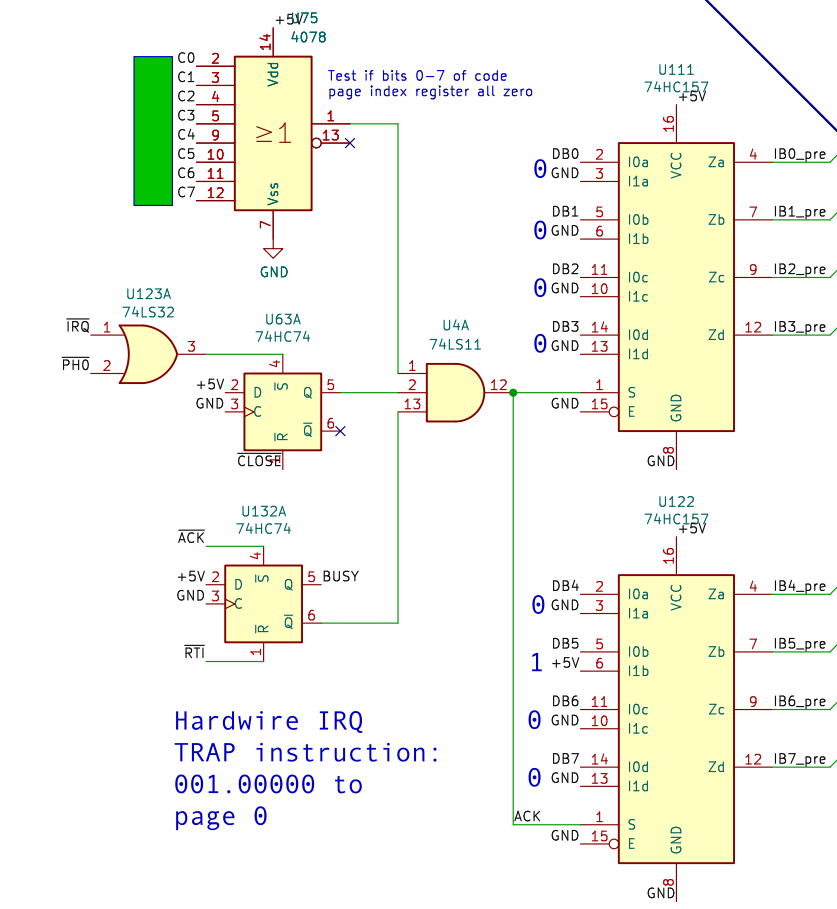
Inner-loops



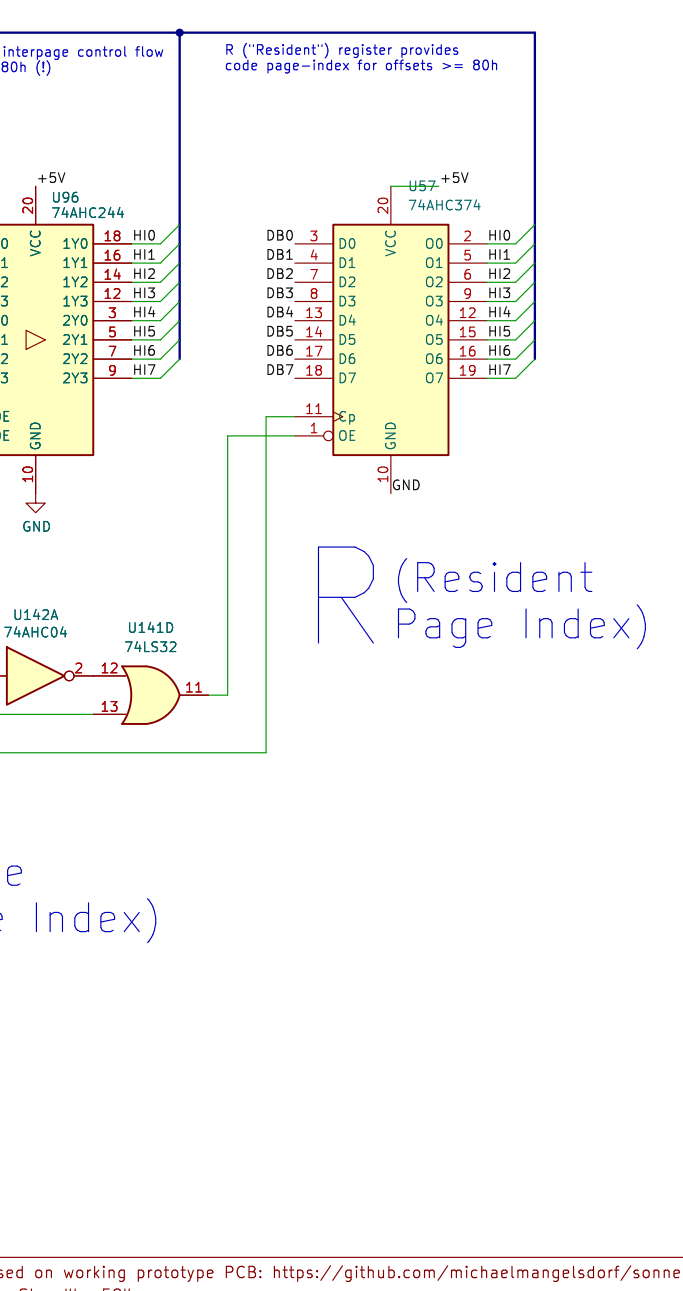
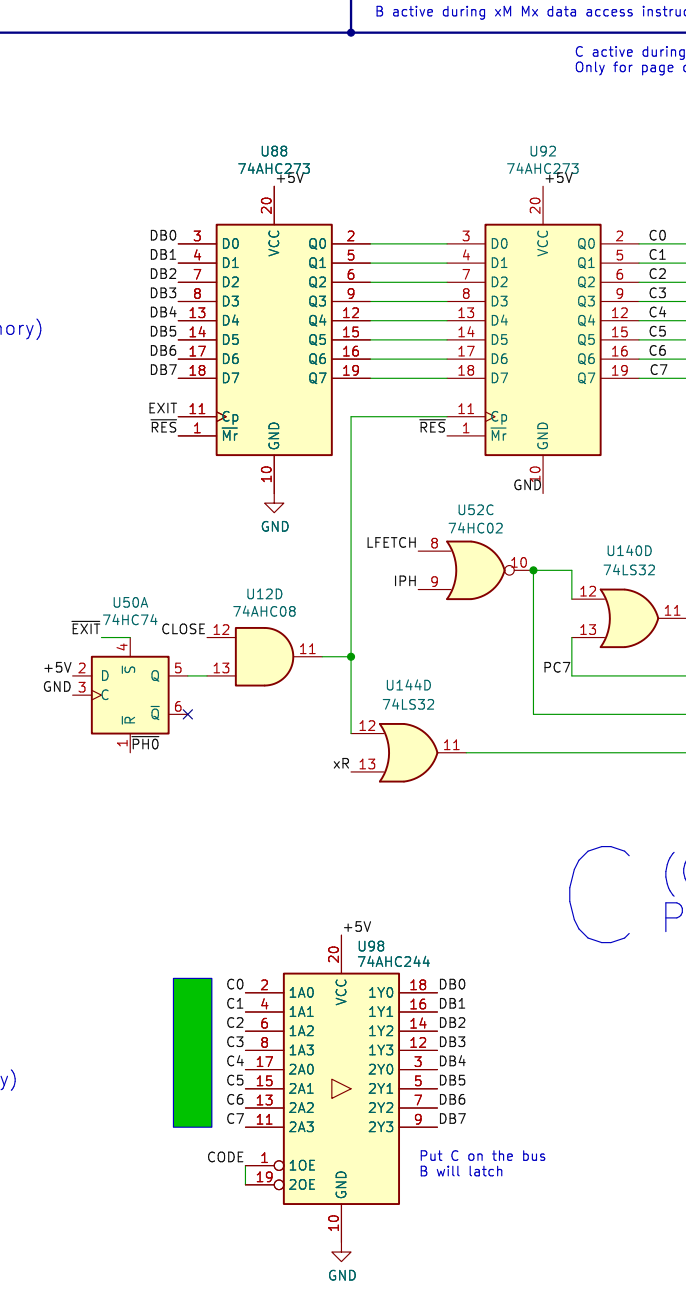
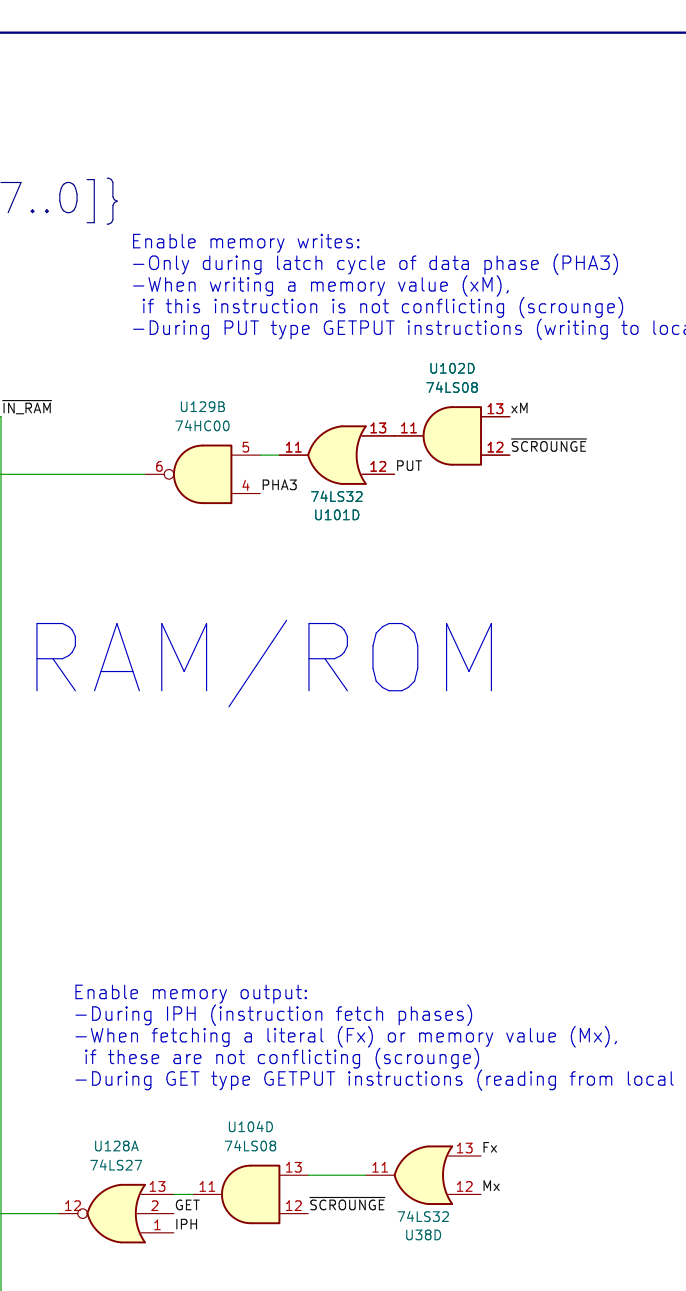
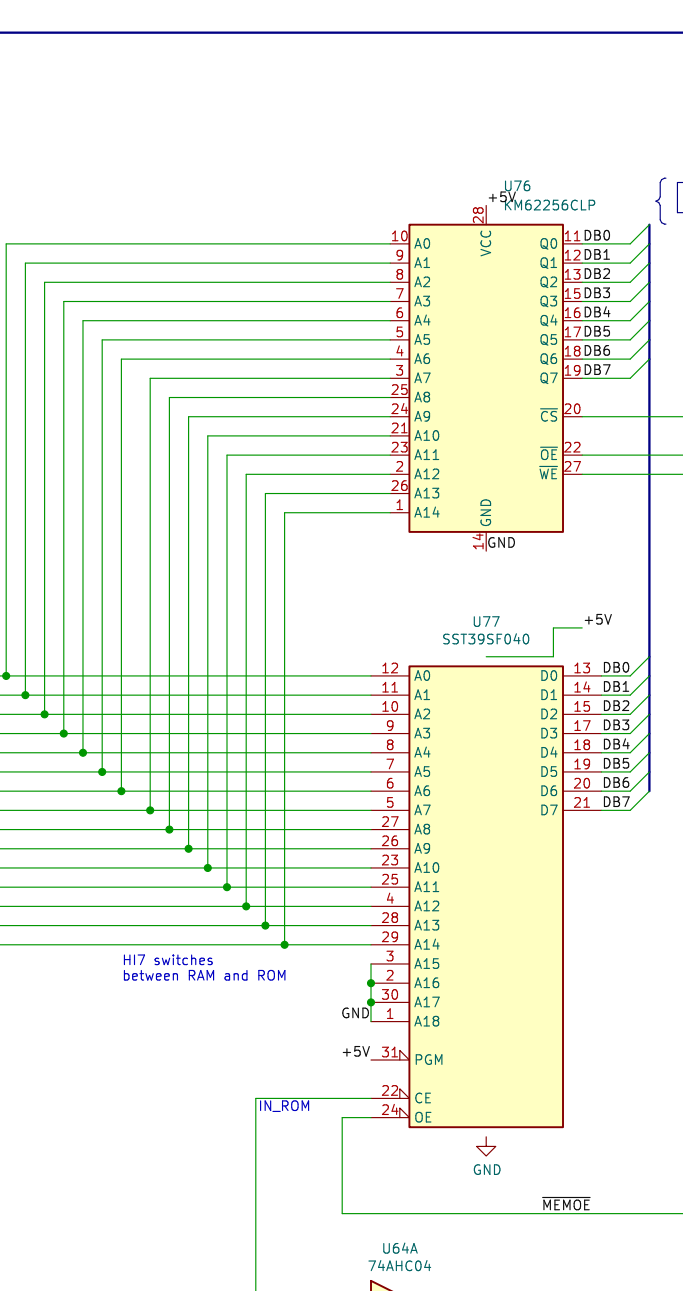
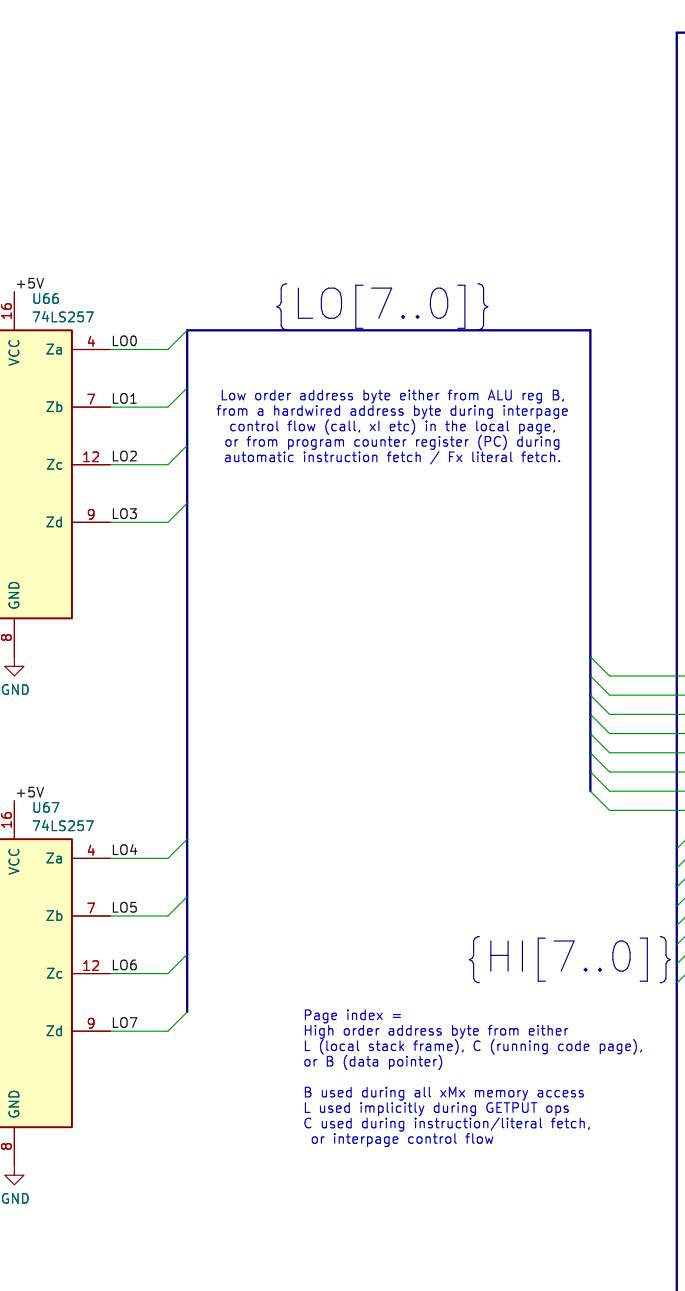
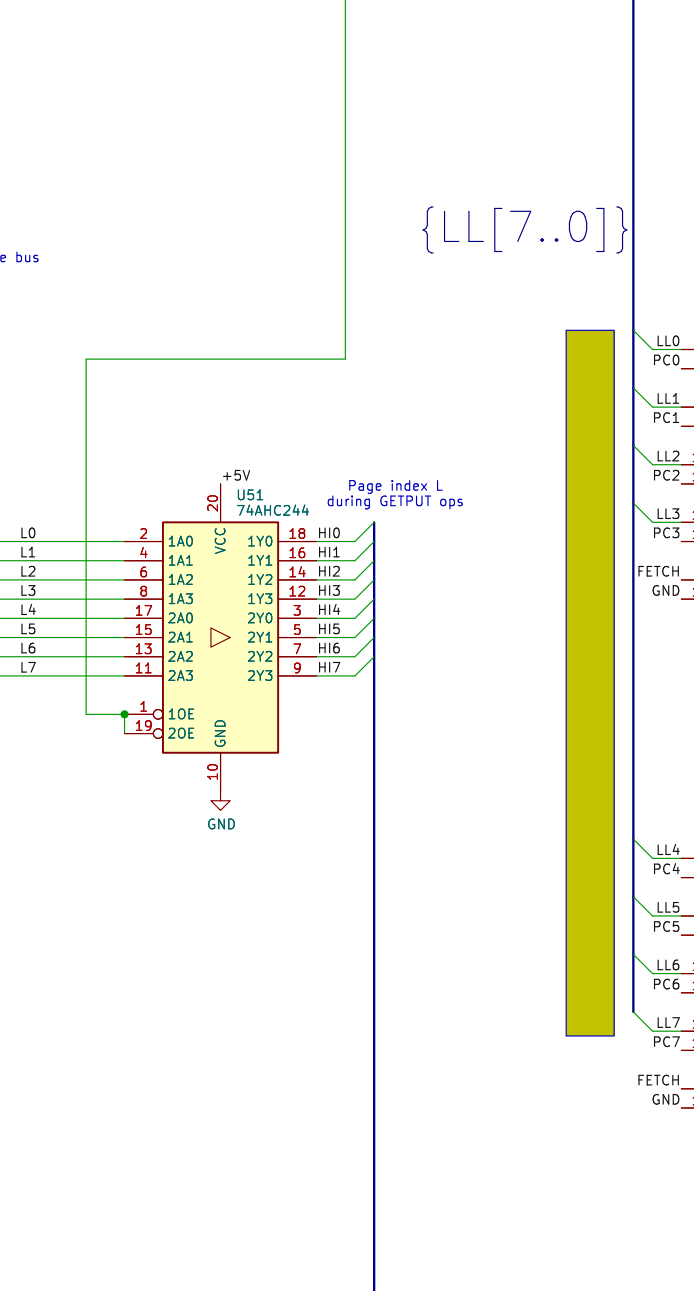
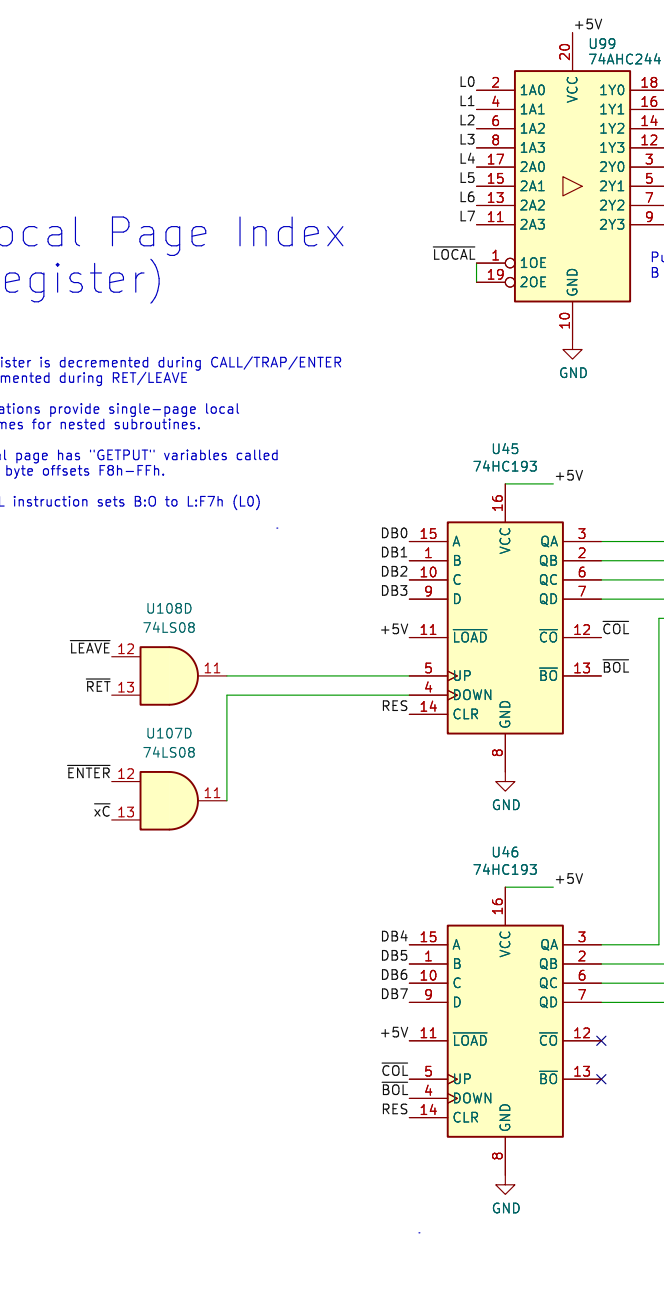
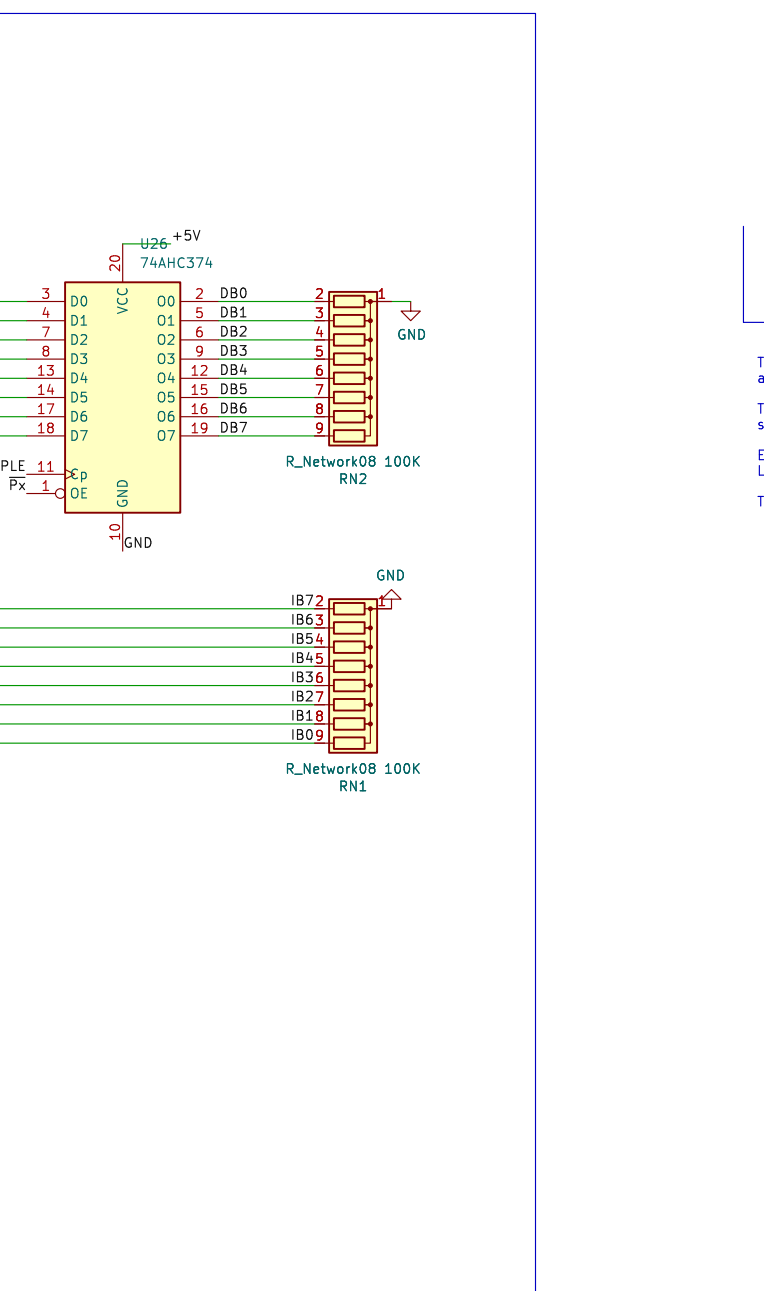
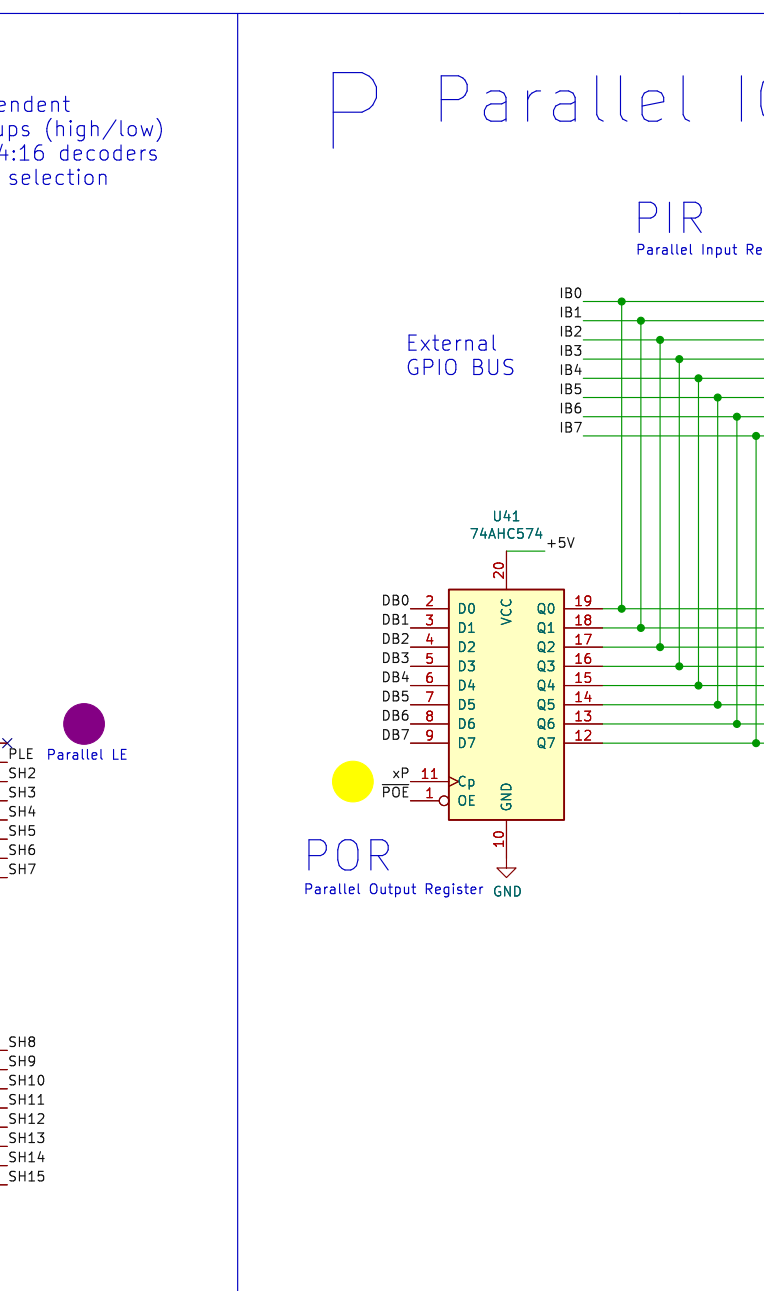
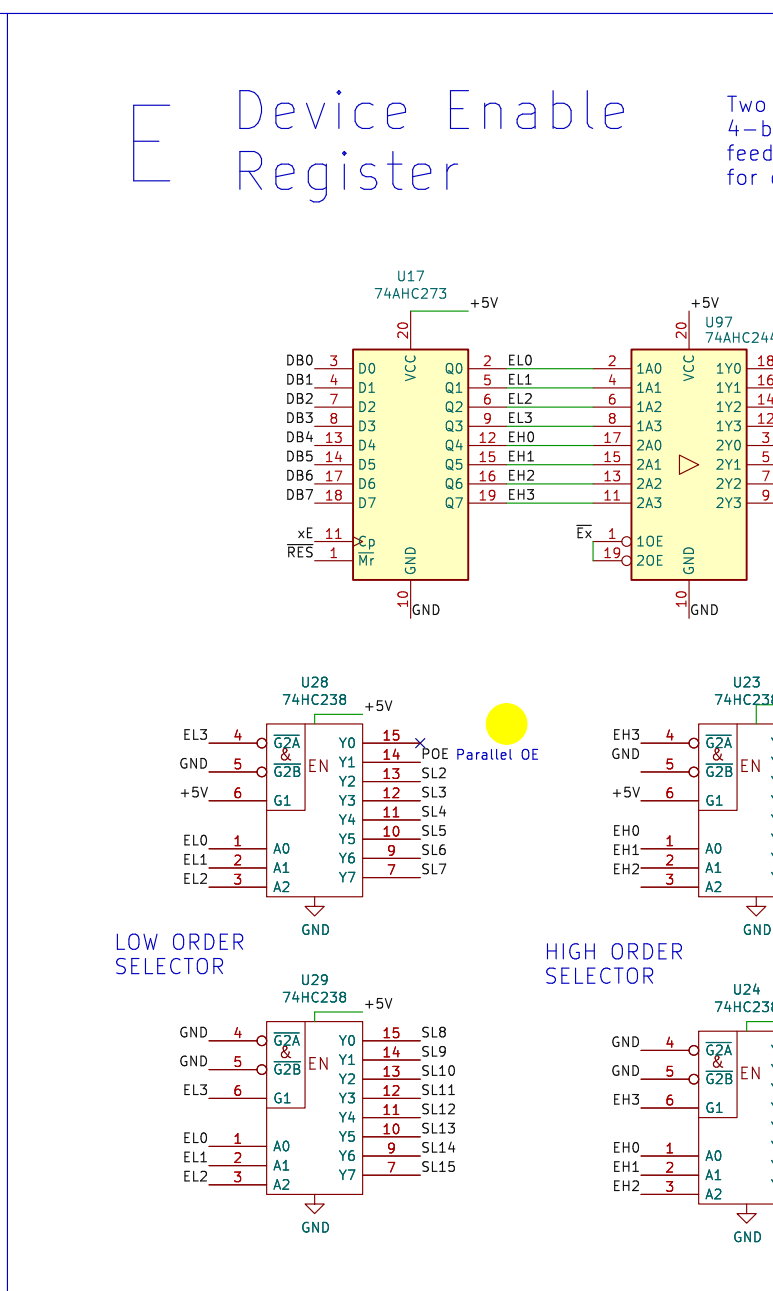
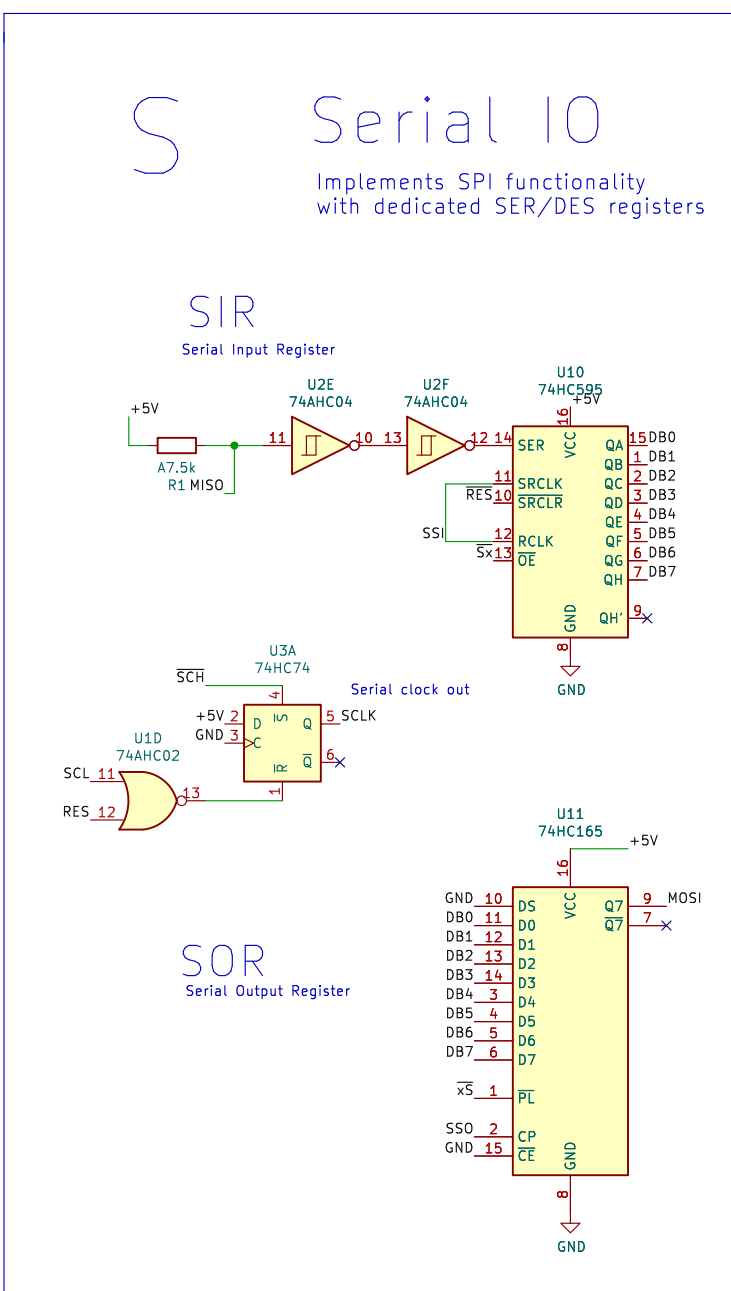
Instruction Decoder

Start, latch instruction or interrupt vector

Interrupts disabled when "BUSY" and when running code in page 0 (See code page index reg schematics bottom right)



Input/Output



RAM/ROM

