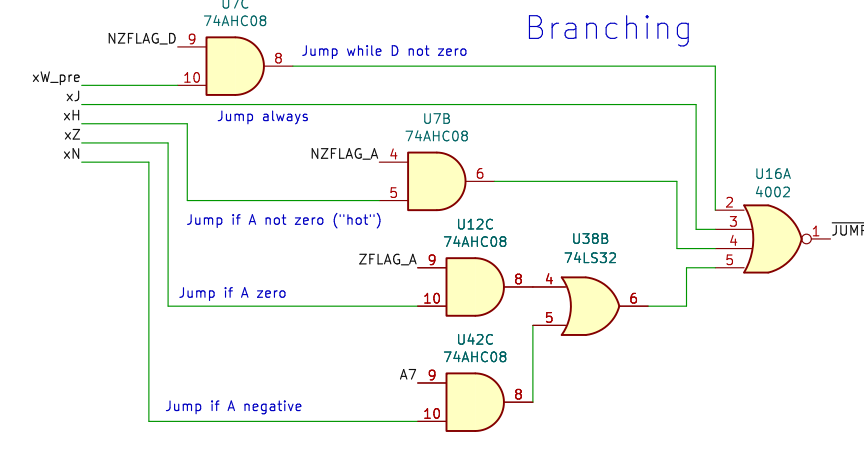
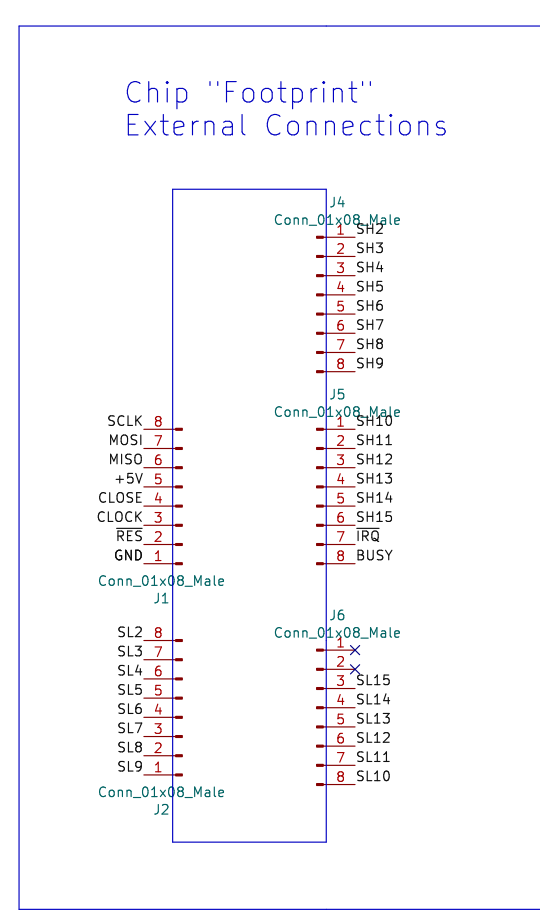
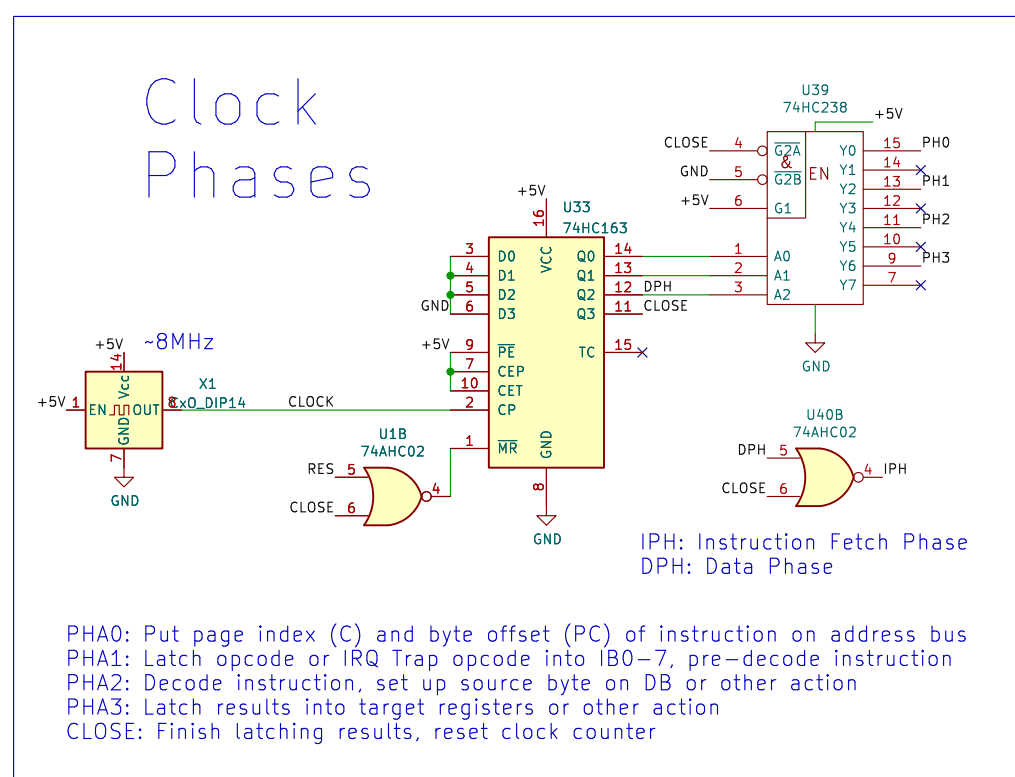


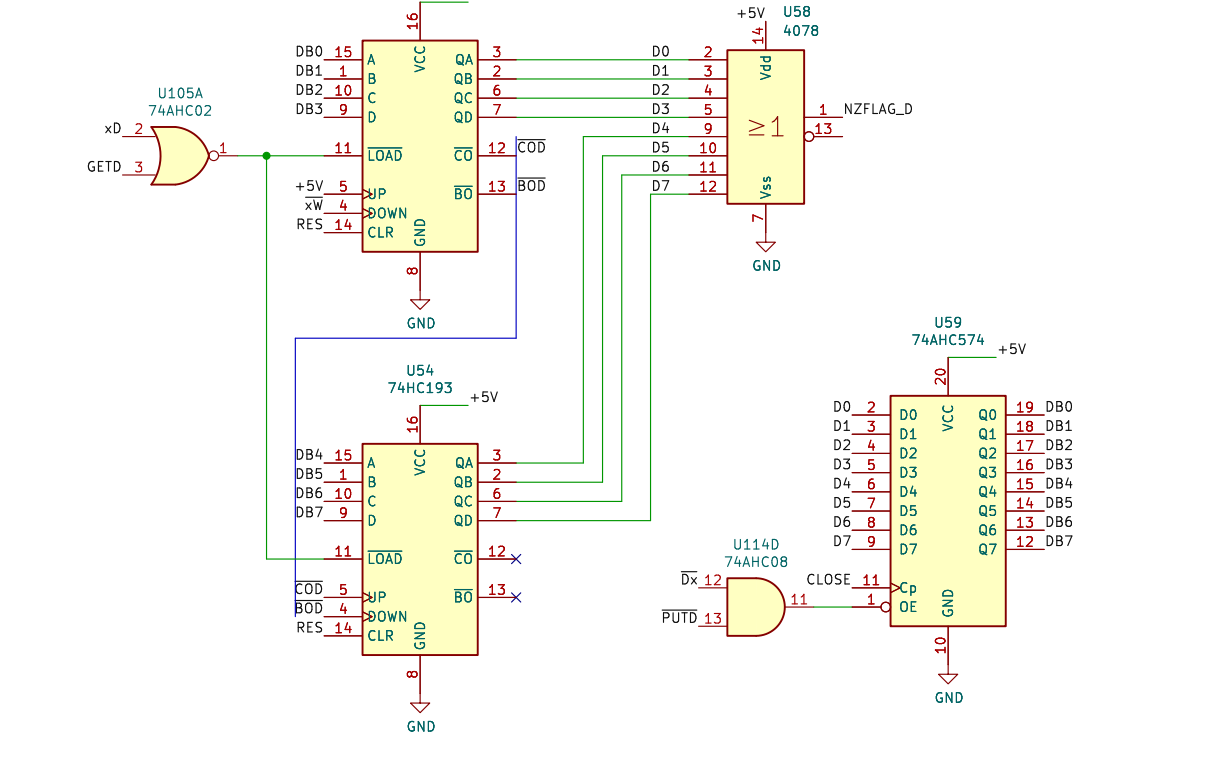
Sonne-8 Microcontroller

Reference Schematics

Rev. Myth



D(OWN) COUNTER Inner-loops



Instruction Decoder

Start, latch instruction or interrupt vector

Interrupts disabled when "BUSY" and when running code in page 0 (See code page index reg schematics bottom right)

Hardware IRQ TRAP instruction: 001.00000 to page 0

On instruction fetch: If IRQ and not BUSY, inject "TRAP 0" opcode, else fetch opcode from memory at C:PC

TRAP opcode triggers call to interrupt service routine in page 0, disabling further interrupts, and toggles ("BUSY")

BUSY state removed by RTI instruction

Opcode Type Decoder

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

Instruction Decoder

Precode signals for early triggers

Pre-Decoder PAIR Target

Pre-Decoder PAIR Source

Pre-Decoder PAIR Target

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Instruction Decoder

Precode signals for early triggers

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Serial IO

Implements SPI functionality with dedicated SER/DES registers

SIR Serial Input Register

SOR Serial Output Register

Device Enable Register

Two independent A-BUS groups (high/low) feed into 4-to-2 decoders for device selection

LOW ORDER SELECTOR

HIGH ORDER SELECTOR

Parallel IO

External GPIO BUS

PIR Parallel Input Register

POR Parallel Output Register

(Local Page Index Register)

This register is recommended during CALL/TRAP/ENTER and is incremented during RET/LEAVE. It holds the local page index for the current instruction. It is 16 bits wide and holds the local page index.

{LL[7..0]}

Low order address byte after from ALI, reg B, control flow (see page 0) to the local page index. It is 8 bits wide and holds the local page index.

{LO[7..0]}

Low order address byte after from ALI, reg B, control flow (see page 0) to the local page index. It is 8 bits wide and holds the local page index.

{HI[7..0]}

High order address byte after from ALI, reg B, control flow (see page 0) to the local page index. It is 8 bits wide and holds the local page index.

{H[7..0]}

High order address byte after from ALI, reg B, control flow (see page 0) to the local page index. It is 8 bits wide and holds the local page index.

{DB[7..0]}

DB[7..0] is a 16-bit register that holds the data bus value. It is 16 bits wide and holds the data bus value.

Based on working prototype PCB: <https://github.com/michaelmagerdorf/sonne8>
Rev. 0.0.1
Project homepage: <https://github.com/michaelmagerdorf/sonne8>
Author: Michael Magerdorf

Copyright: 2025-26-05
Title: Sonne-8 Micro-Controller
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