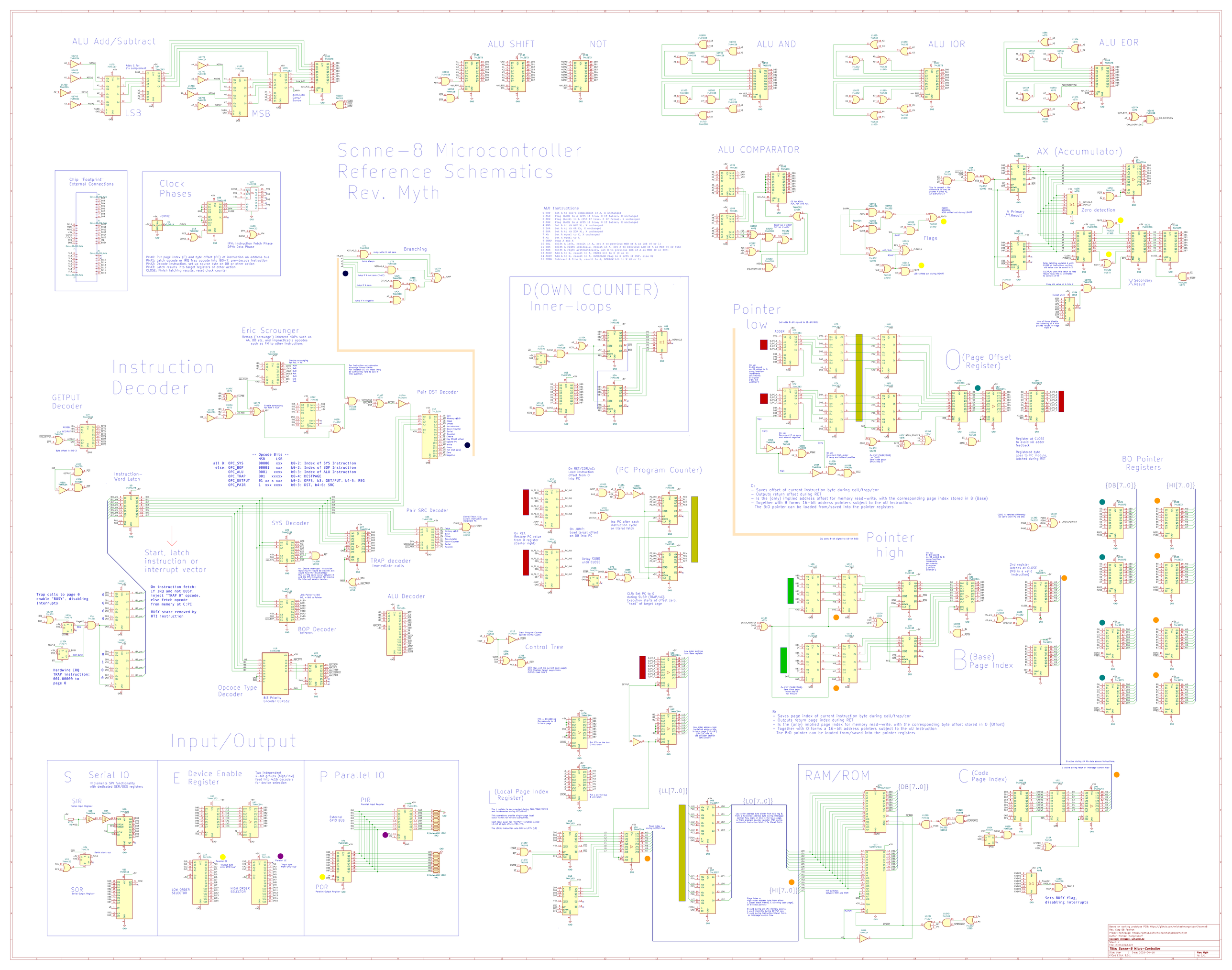
Sonne-8 Microcontroller
Reference Schematics
Rev. Myth
ALU Add/Subtract
LSB
MSB
Adds 1 for 2's complement
ALU SHIFT
NOT
ALU AND
ALU IOR
ALU EOR
ALU COMPARATOR
Flags
AX (Accumulator)
Primary Result
Zero detection
Secondary Result
Chip "Footprint" External Connections
Clock Phases
8MHz
IPH: Instruction Fetch Phase
DPH: Data Phase
PHA0: Put page index (C) and byte offset (PC) of instruction on address bus
PHA1: Latch opcode or IRQ Trap opcode into IRD-7, pre-decode instruction
PHA2: Decode instruction, set up source byte on DB or other action
PHA3: Latch results into target registers or other action
CLOSE: Finish latching results, reset clock counter
ALU Instructions
0 NOT Set A to one's complement of X, X unchanged
1 ALU Flag (A<X) in A (255 if true, 0 if false), X unchanged
2 ADC Flag (A<=X) in A (255 if true, 0 if false), X unchanged
3 AGE Flag (A>X) in A (255 if true, 0 if false), X unchanged
4 ADD Set A to (A AND X), X unchanged
5 IOR Set A to (A OR X), X unchanged
6 EOR Set A to (A XOR X), X unchanged
7 XA Set A equal to X, X unchanged
8 XAZ Set X equal to A
9 SWAP Swap A and X
10 ORL Shift A left, result in A, set X to previous MSB of A as LSB (0 or 1)
11 ORR Shift A right logically, result in A, set X to previous LSB of A as MSB (0 or 80h)
12 ASR Shift A right arithmetically, set X to previous LSB of A as MSB (0 or 80h)
13 ADOC Add A to X, result in A, CARRY bit (in X (0 or 1)
14 ADOV Add A to X, result in A; OVERFLOW flag (in X (255 if OVF, else 0)
15 SUBB Subtract A from X, result in A, BORROW bit in X (0 or 1)
Branching
D(OWN COUNTER)
Inner-loops
Pointer low
(Page Offset Register)
Eric Scrounger
Remap ("scrounge") inherent NOPs such as AA, DD etc. and impracticable opcodes such as FM to other instructions
Instruction Decoder
GETPUT Decoder
Instruction-Word Latch
Start, latch instruction or interrupt vector
Pair DST Decoder
Pair SRC Decoder
SYS Decoder
TRAP decoder
Immediate calls
ALU Decoder
BOP Decoder
Opcode Type Decoder
8:3 Priority Encoder CD4532
Trap calls to page 0 enable "BUSY", disabling Interrupts
Hardwire IRQ TRAP instruction: 001.00000 to page 0
-- Opcode Bits --
MSB LSB
all 0: OPC_SYS 00000 xxx b0-2: Index of SYS Instruction
else: OPC_BOP 00001 xxx b0-2: Index of BOP Instruction
OPC_ALU 0001 xxxx b0-3: Index of ALU Instruction
OPC_TRAP 001 xxxxx b0-4: DESTPAGE
OPC_GETPUT 01 xx x xxx b0-2: OFFS, b3: GET/PUT, b4-5: REG
OPC_PAIR 1 xxx xxxx b0-3: DST, b4-6: SRC
(PC Program Counter)
On RET/COR/vC: Load instruction offset from O into PC
On RET: Restore PC value from O register (Center right)
On JUMP: Load target offset on DB into PC
Inc PC after each instruction cycle or literal fetch
Delay SUBR until CLOSE
CLR: Set PC to 0 during SUBR (TRAP/vC). Execution starts at offset zero, 'head' of target page
Control Tree
Pointer high
2nd register latches at CLOSE (MB is a valid instruction)
B (Base) Page Index
BO Pointer Registers
{DB[7..0]}
{HI[7..0]}
Input/Output
S Serial IO
Implements SPI functionality with dedicated SER/DES registers
SIR
Serial Input Register
SOR
Serial Output Register
E Device Enable Register
Two independent 4-bit groups (high/low) feed into 4:16 decoders for device selection
LOW ORDER SELECTOR
HIGH ORDER SELECTOR
P Parallel IO
PIR
Parallel Input Register
POR
Parallel Output Register
External GPIO BUS
(Local Page Index Register)
{LL[7..0]}
{LO[7..0]}
{HI[7..0]}
RAM/ROM
C (Code Page Index)
Sets BUSY flag, disabling Interrupts
Based on working prototype PCB: https://github.com/michaelmangelsdorf/sonne8
Rev. Sony SB Feathch
Project homepage: https://github.com/michaelmangelsdorf/myth
Author: Michael Mangelsdorf
Contact: mim@ok-schafer.de
Sheet: /
File: myth-mixed.kicad_sch
Title: Sonne-8 Micro-Controller
Size: User Date: 2025-08-16 Rev: Myth
KiCad 8.0.4, 9.0.1 Id: 1/1