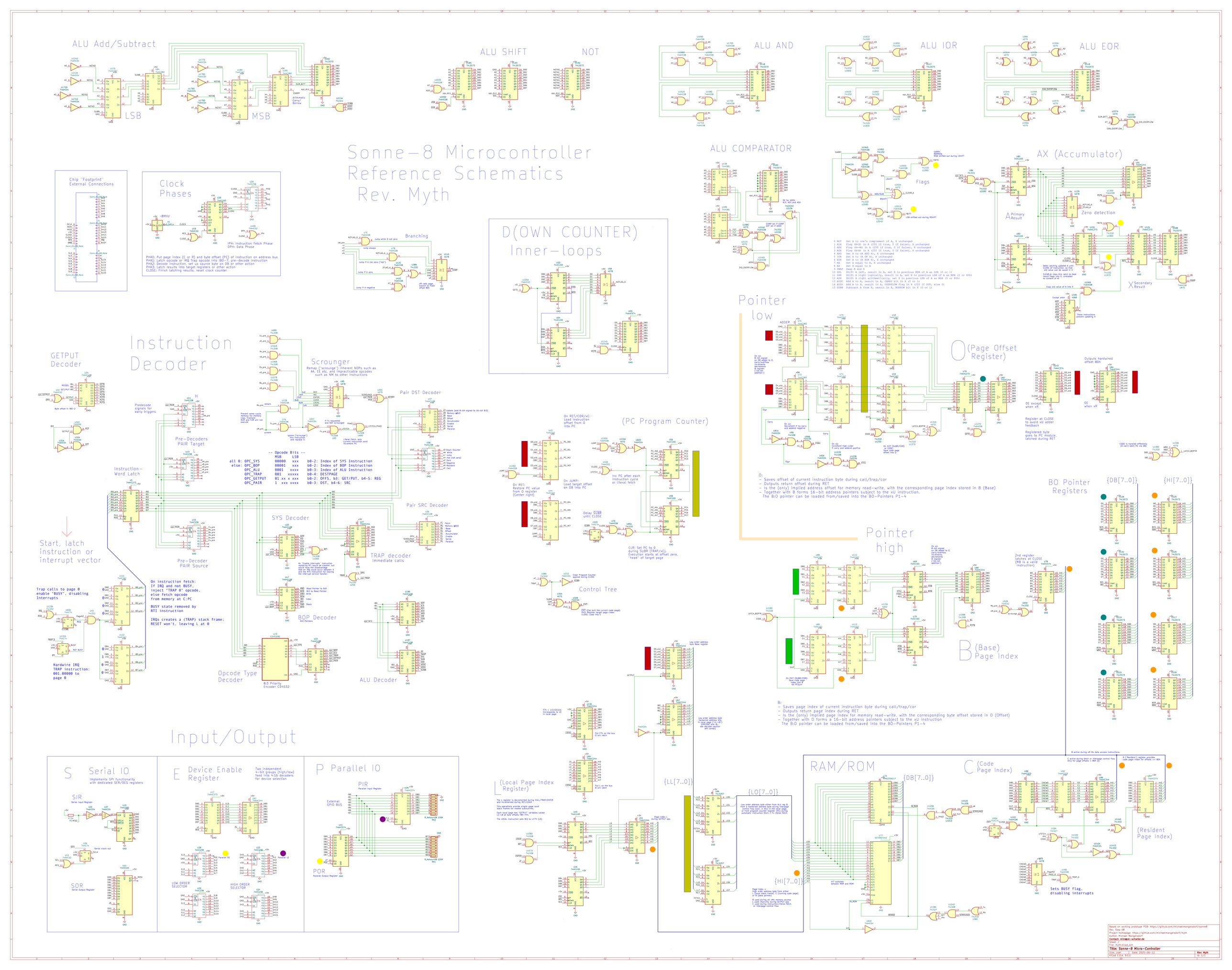
Sonne-8 Microcontroller
Reference Schematics
Rev. Myth
ALU Add/Subtract
LSB
MSB
ALU SHIFT
NOT
ALU AND
ALU IOR
ALU EOR
ALU COMPARATOR
Flags
AX (Accumulator)
Primary Result
Zero detection
Secondary Result
Chip "Footprint" External Connections
Clock Phases
PHA0: Put page index (C or R) and byte offset (PC) of instruction on address bus
PHA1: Latch opcode or IRQ Trap opcode into IR0-7, pre-decode instruction
PHA2: Decode instruction, set up source byte on DB or other action
PHA3: Latch results into target registers or other action
CLOSE: Finish latching results, reset clock counter
IPH: Instruction Fetch Phase
DPH: Data Phase
D(OWN COUNTER)
Inner-loops
Branching
Pointer low
ADDER
O (Page Offset Register)
O:
- Saves offset of current instruction byte during call/trap/cor
- Outputs return offset during RET
- Is the (only) implied address offset for memory read-write, with the corresponding page index stored in B (Base)
- Together with B forms 16-bit address pointers subject to the xU instruction.
The B:O pointer can be loaded from/saved into the B0-Pointers P1-4
GETPUT Decoder
Instruction Decoder
Scrounger
Remap ("scrounge") inherent NOPs such as AA, EE etc. and impracticable opcodes such as NN to other instructions
Pair DST Decoder
Pair SRC Decoder
Predecode signals for early triggers
Pre-Decoders PAIR Target
Pre-Decoder PAIR Source
Instruction-Word Latch
SYS Decoder
BOP Decoder
TRAP decoder
Immediate calls
Opcode Type Decoder
ALU Decoder
Start, latch instruction or interrupt vector
On instruction fetch:
IF IRQ and not BUSY,
inject "TRAP 0" opcode,
else fetch opcode
from memory at C:PC
BUSY state removed by
RTI instruction
IRQs creates a (TRAP) stack frame;
RESET won't, leaving L at 0
Trap calls to page 0
enable "BUSY", disabling
Interrupts
Hardwire IRQ
TRAP instruction:
001.00000 to
page 0
-- Opcode Bits --
MSB LSB
all 0: OPC_SYS 00000 xxx b0-2: Index of SYS Instruction
else: OPC_BOP 00001 xxx b0-2: Index of BOP Instruction
OPC_ALU 0001 xxxx b0-3: Index of ALU Instruction
OPC_TRAP 001 xxxxx b0-4: DESTPAGE
OPC_GETPUT 01 xx x xxx b0-2: OFFS, b3: GET/PUT, b4-5: REG
OPC_PAIR 1 xxx xxxx b0-3: DST, b4-6: SRC
(PC Program Counter)
On RET/COR/xC:
Load instruction
offset from O
into PC
On JUMP:
Load target offset
on DB into PC
Inc PC after each
instruction cycle
or literal fetch
On RET:
Restore PC value
from O register
(Center right)
Delay SUBR
until CLOSE
CLR: Set PC to 0
during SUBR (TRAP/xC).
Execution starts at offset zero,
"head" of target page
Control Tree
Pointer high
2nd register
latches at CLOSE
(MB is a valid
instruction)
B (Base) Page Index
B:
- Saves page index of current instruction byte during call/trap/cor
- Outputs return page index during RET
- Is the (only) implied page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
The B:O pointer can be loaded from/saved into the B0-Pointers P1-4
BO Pointer Registers
{DB[7..0]}
{HI[7..0]}
Input/Output
S Serial IO
Implements SPI functionality with dedicated SER/DIS registers
SIR
Serial Input Register
SOR
Serial Output Register
E Device Enable Register
Two independent 4-bit groups (high/low) feed into 4:16 decoders for device selection
LOW ORDER SELECTOR
HIGH ORDER SELECTOR
P Parallel IO
PIR
Parallel Input Register
External GPIO BUS
POR
Parallel Output Register
L (Local Page Index Register)
The L register is decremented during CALL/TRAP/ENTER and incremented during RET/LEAVE
This operations provide single-page local stack frames for nested subroutines.
Each local page has "GETPUT" variables called L:L+0 at byte offsets 00h-FFh.
The LOCAL instruction sets B:O to L:FFh (L0)
{LL[7..0]}
{LO[7..0]}
{HI[7..0]}
RAM/ROM
C (Code Page Index)
(Resident Page Index)
Sets BUSY flag,
disabling interrupts
Based on working prototype PCB: https://github.com/michaelmangelsdorf/sonne8
Rev. Step 5B
Project homepage: https://github.com/michaelmangelsdorf/myth
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