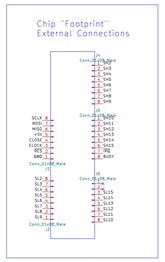
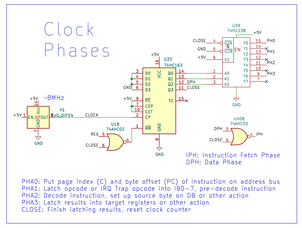
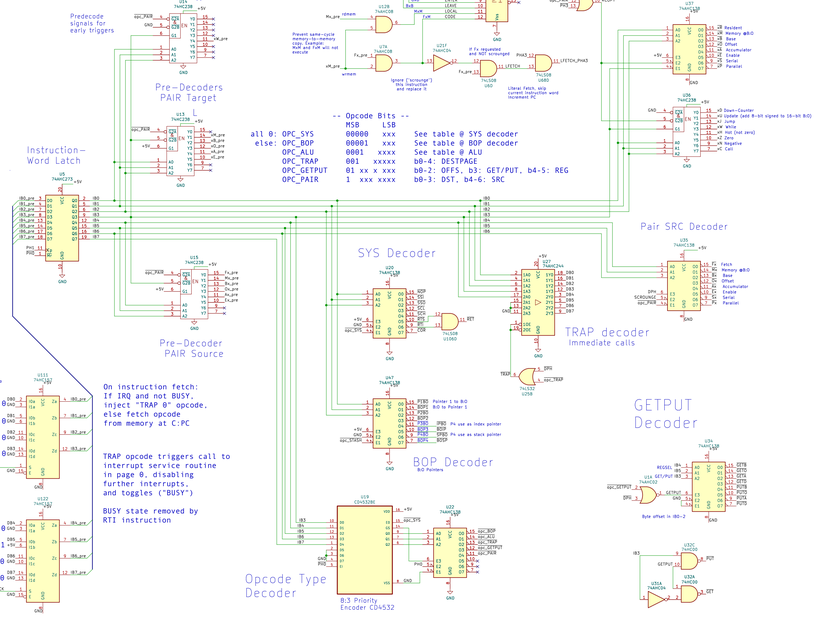
Sonne-8 Microcontroller Reference Schematics Rev. Myth

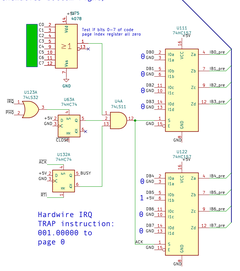




Instruction Decoder



Interrupts disabled when "BUSY" and when running code in page 0 (See code page index reg schematics bottom right)



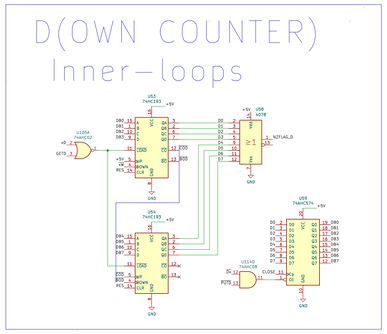
On instruction fetch: If IRQ and not BUSY, inject "TRAP 0" opcode, else fetch opcode from memory at C:PC

TRAP opcode triggers call to interrupt service routine in page 0, disabling further interrupts, and toggles ("BUSY")

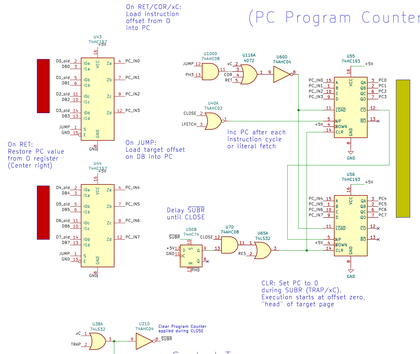
BUSY state removed by RTI instruction

Hardwire IRQ TRAP instruction: 001.00000 to page 0

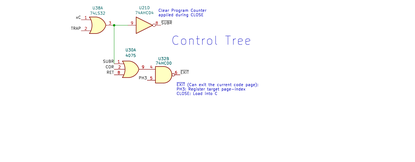
D(OWN COUNTER) Inner-loops



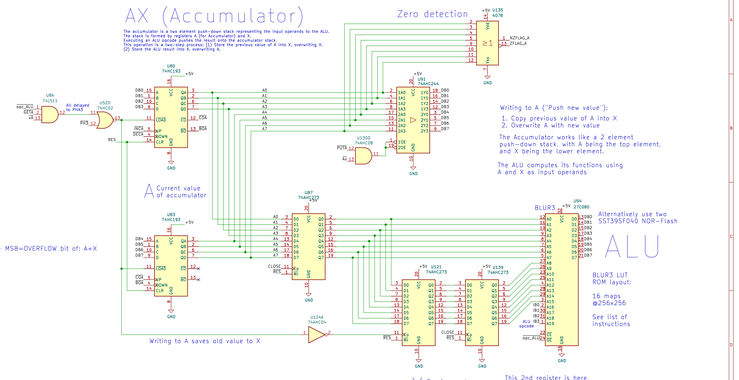
(PC Program Counter)



Control Tree



AX (Accumulator)



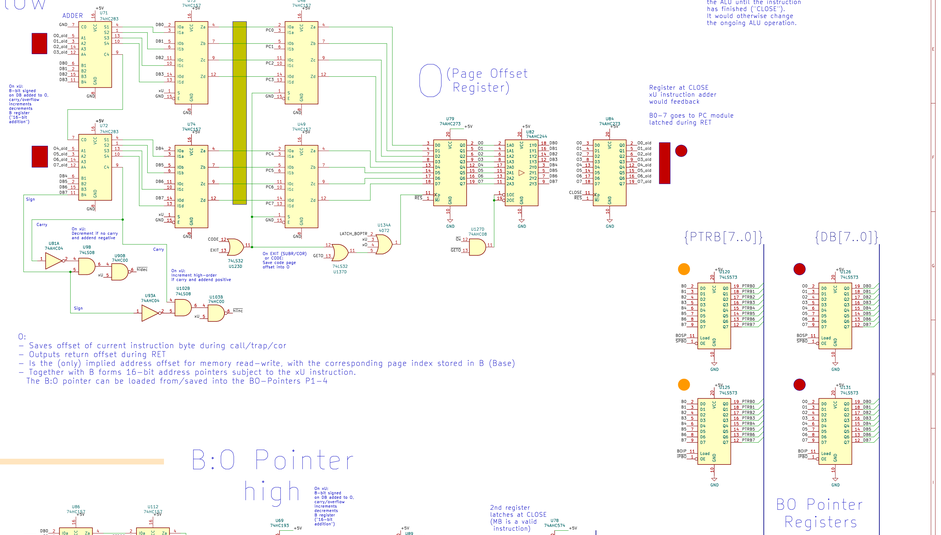
ALU

ALU Instructions

(Results are pushed)

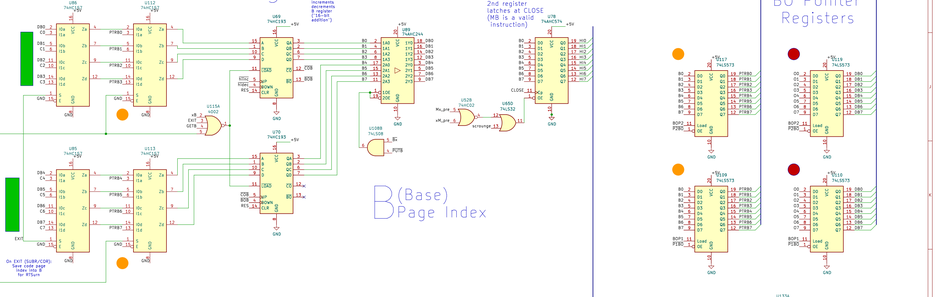
0 DUP ("Copy of A")	A := A
1 SWAP ("Copy of X")	A := X
2 NOTA ("One's Complement of A")	A := ~A
3 NOTX ("One's Complement of X")	A := ~X
4 SLA ("Shift left A")	A := A<<1
5 SLX ("Shift left X")	A := X<<1
6 SRA ("Shift right A")	A := A>>1
7 SRX ("Shift right X")	A := X >> 1
8 AND ("A boolean-and X")	A := A & X
9 IOR ("A inclusive-or X")	A := A | X
10 EOR ("A exclusive-or X")	A := A ^ X
11 ADD ("Add X to A)	A := A + X, bits 0-7
12 OVF ("Carry/Overflow of: A plus X")	A := Zero + LSB=CARRY + MSB=OVERFLOW bit of: A+X
13 ALX ("A less than X")	A := (A<X)? FFh:0
14 AEX ("A equal to X")	A := (A==X)? FFh:0
15 AGX ("A greater than X")	A := (A>X)? FFh:0

B:0 Pointer low



O:
- Saves offset of current instruction byte during call/trap/cor
- Outputs return offset during RET
- Is the (only) implied address offset for memory read-write, with the corresponding page index stored in B (Base)
- Together with B forms 16-bit address pointers subject to the xU instruction.
The B:0 pointer can be loaded from/saved into the B0-Pointers P1-4

B:0 Pointer high

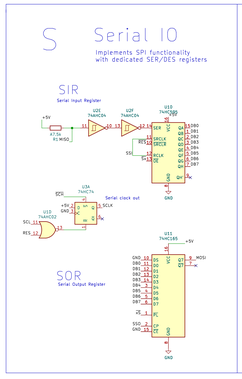


B:
- Saves page index of current instruction byte during call/trap/cor
- Outputs return page index during RET
- Is the (only) implied page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
The B:0 pointer can be loaded from/saved into the B0-Pointers P1-4

Input/Output

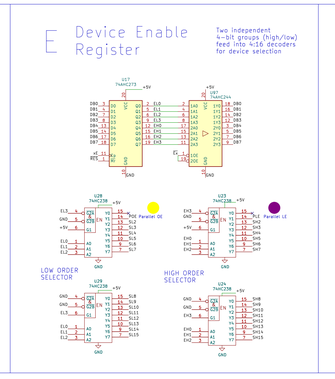
S Serial IO

Implements SPI functionality with dedicated SER/DES registers

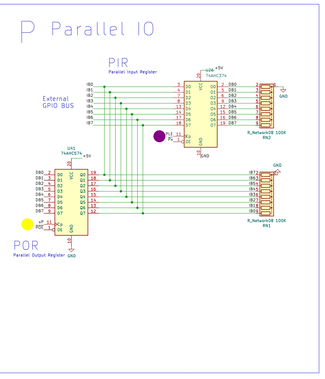


E Device Enable Register

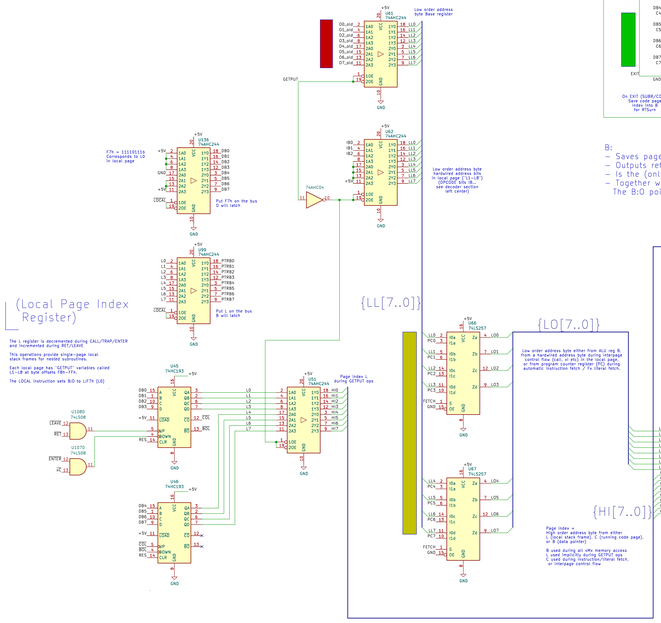
Two independent 4-bit groups (high/low) feed into 4:16 decoders for device selection



P Parallel IO



(Local Page Index Register)



Based on working prototype PCB: https://github.com/michaelmangelsdorf/sonne8
Rev. Step "Zero"
Project homepage: https://github.com/michaelmangelsdorf/myth
Author: Michael Mangelsdorf
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Sheet: /
File: myth.kicad_sch

Title: Sonne-8 Micro-Controller

Size: A0	Date: 2025-06-07	Rev: Myth
KiCad 8.0.4, 9.0.1		Id: 1/1