

Sonne-8 Microcontroller

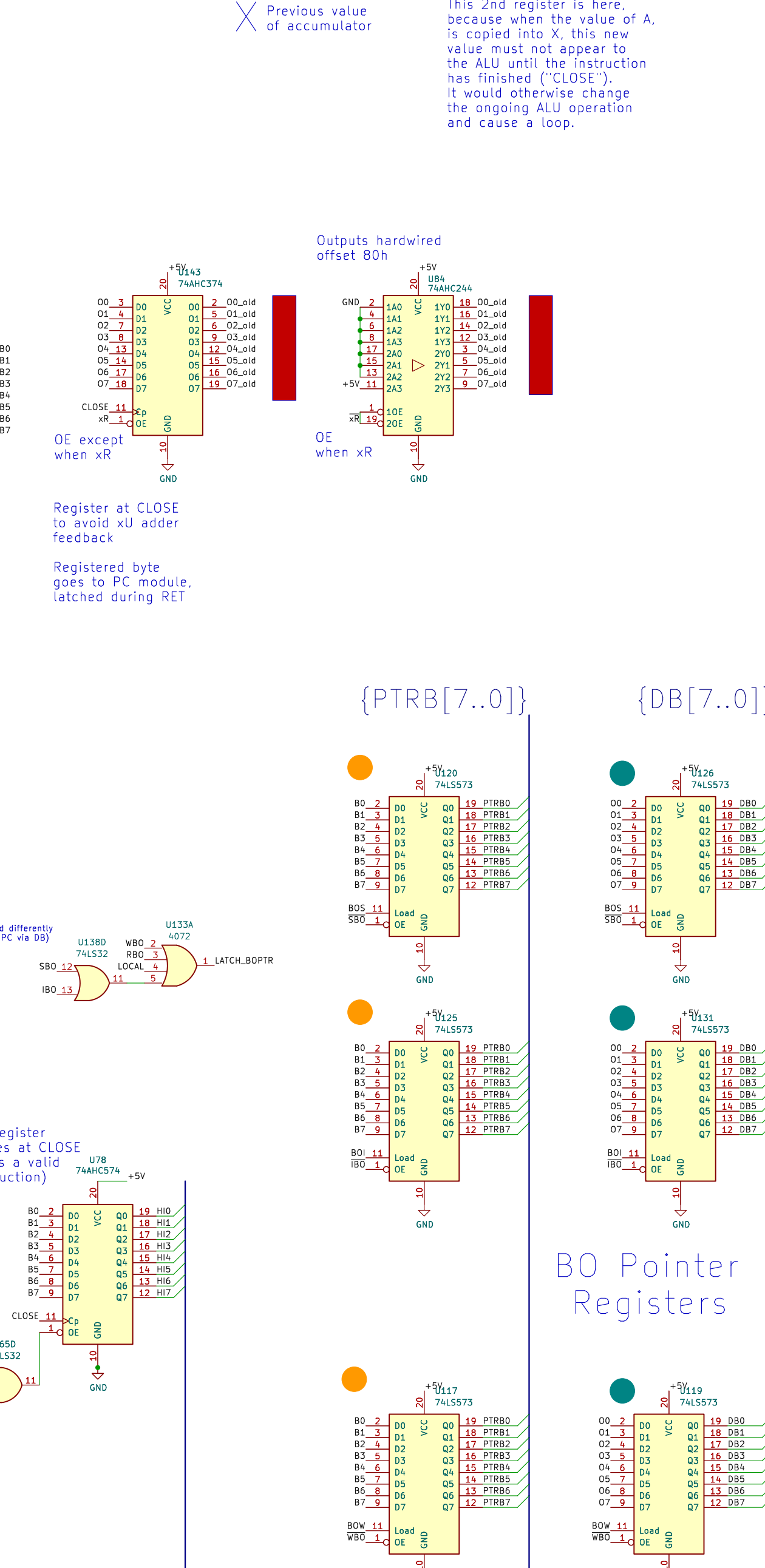
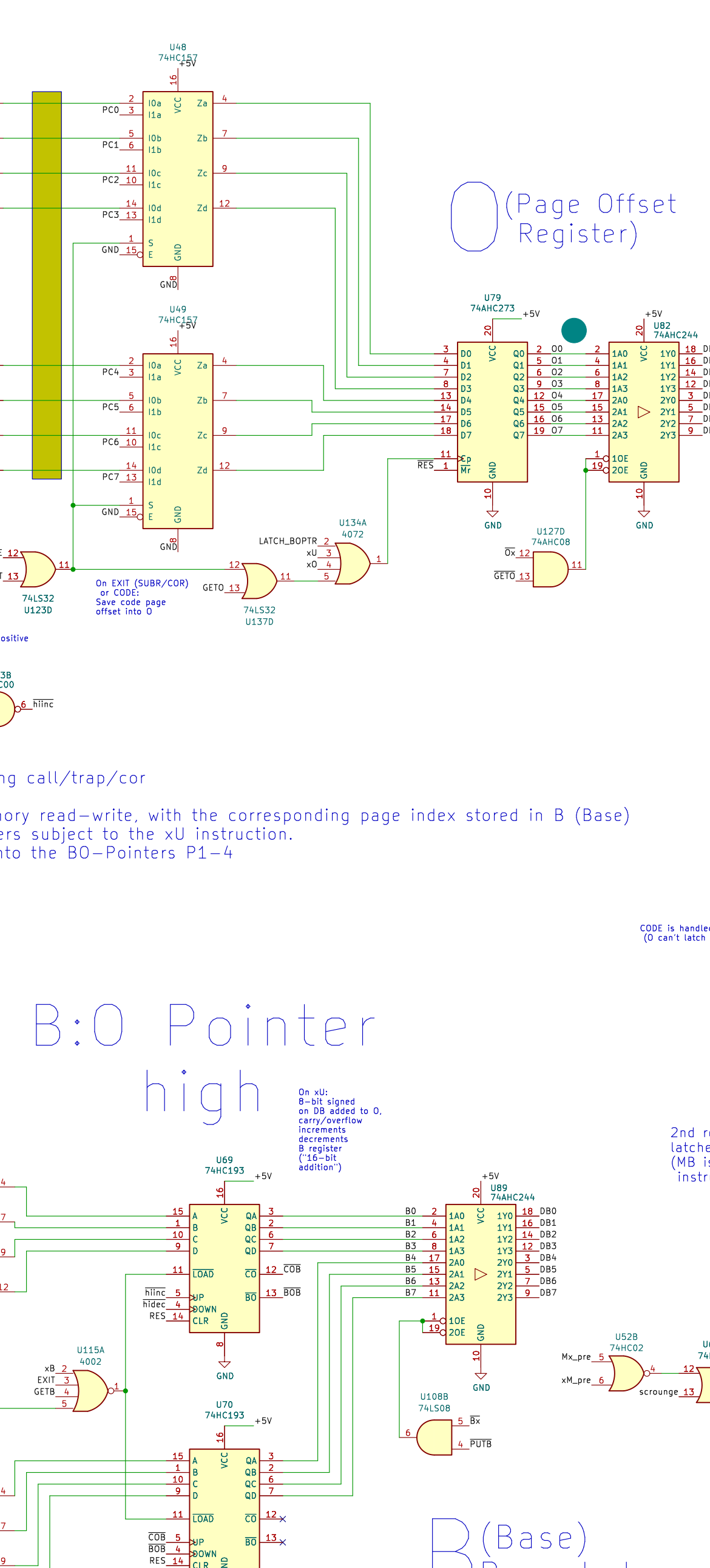
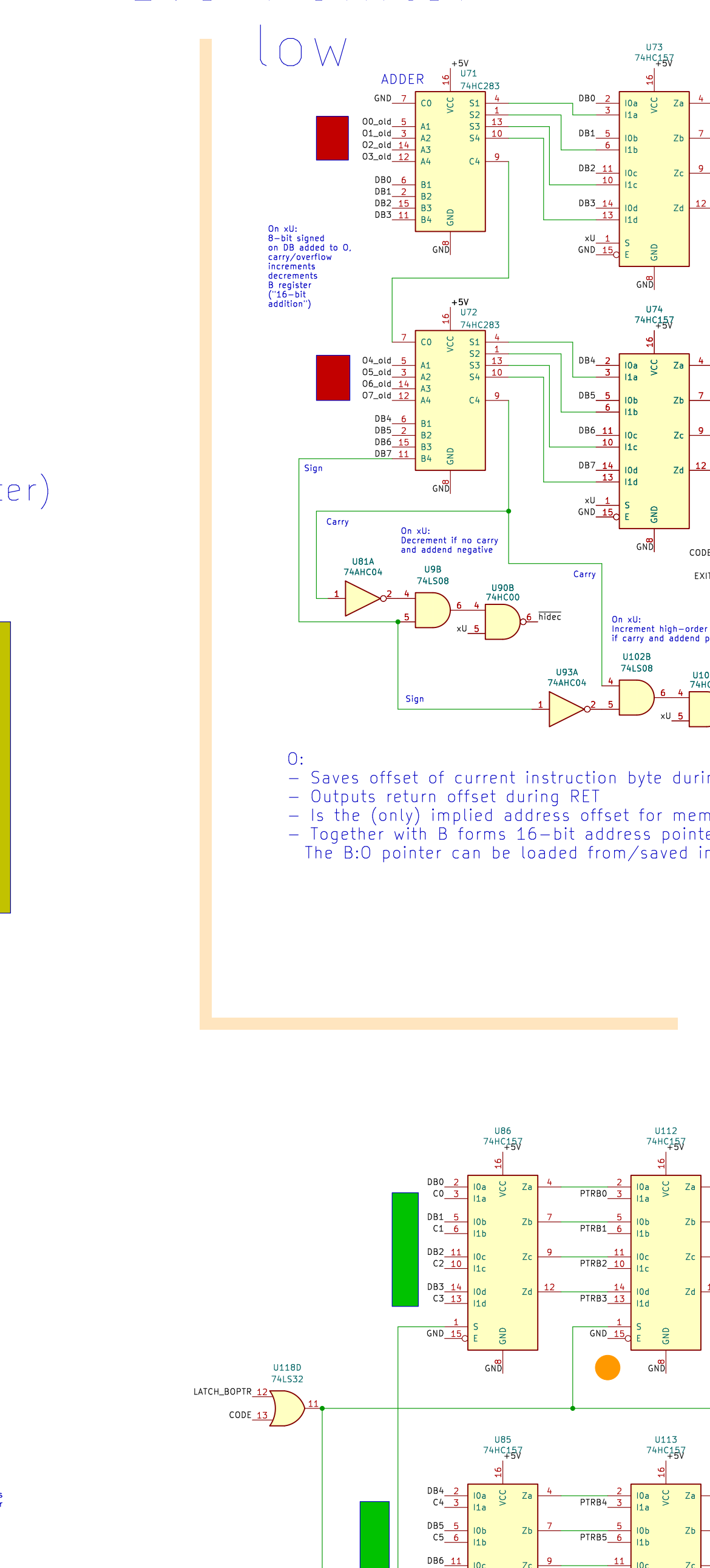
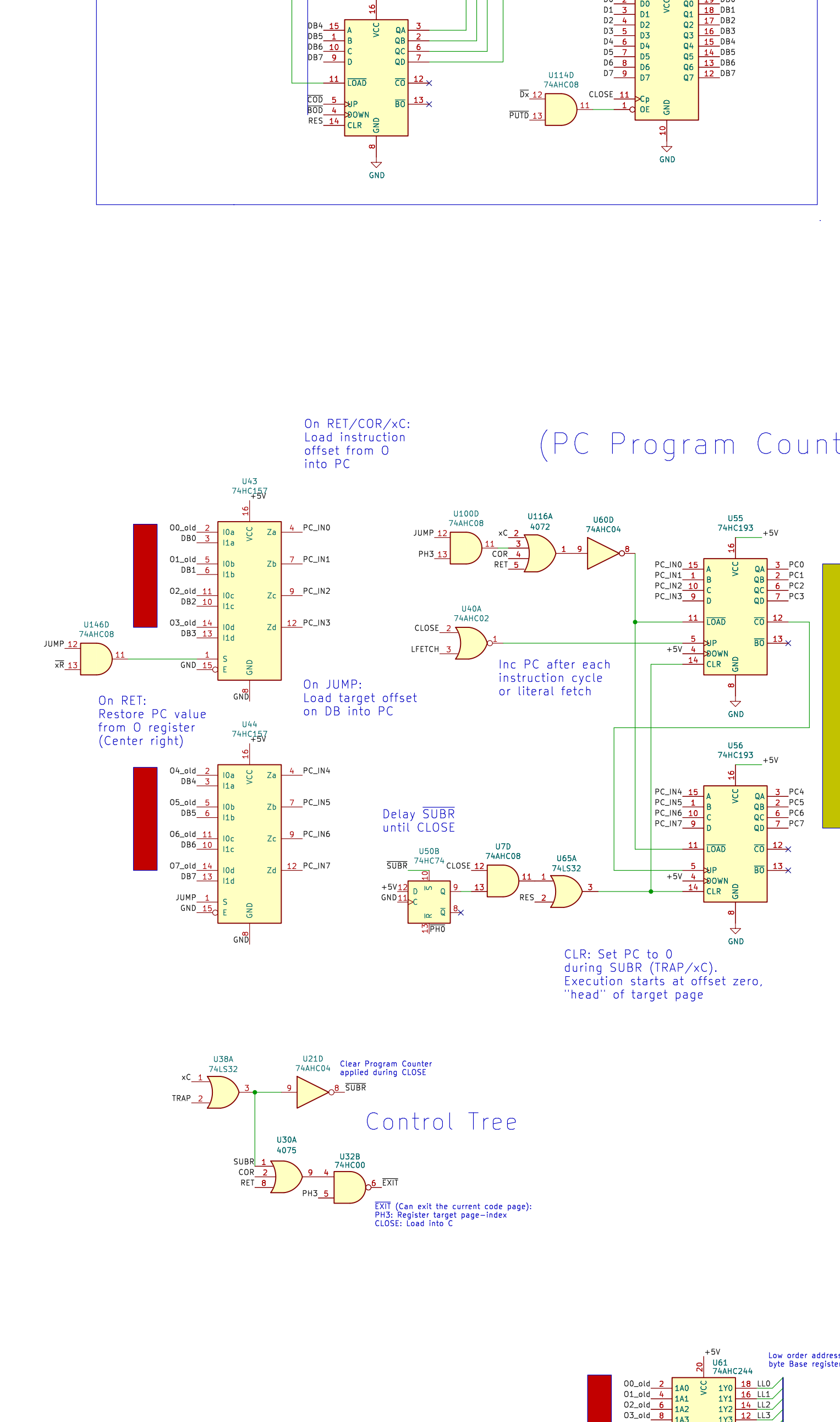
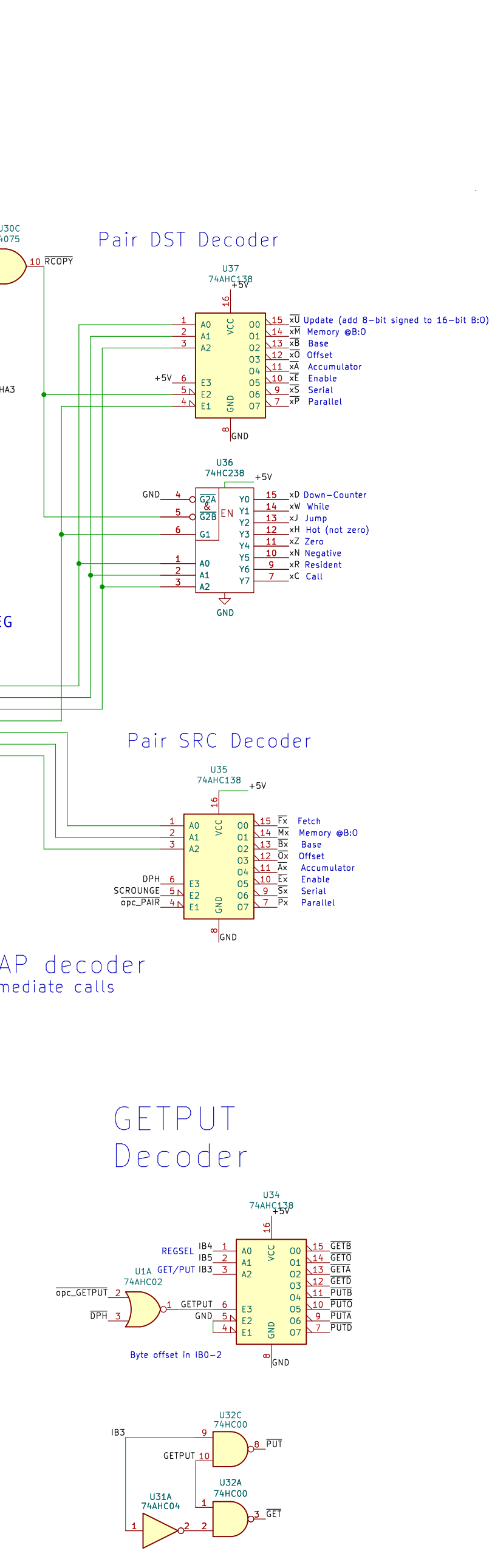
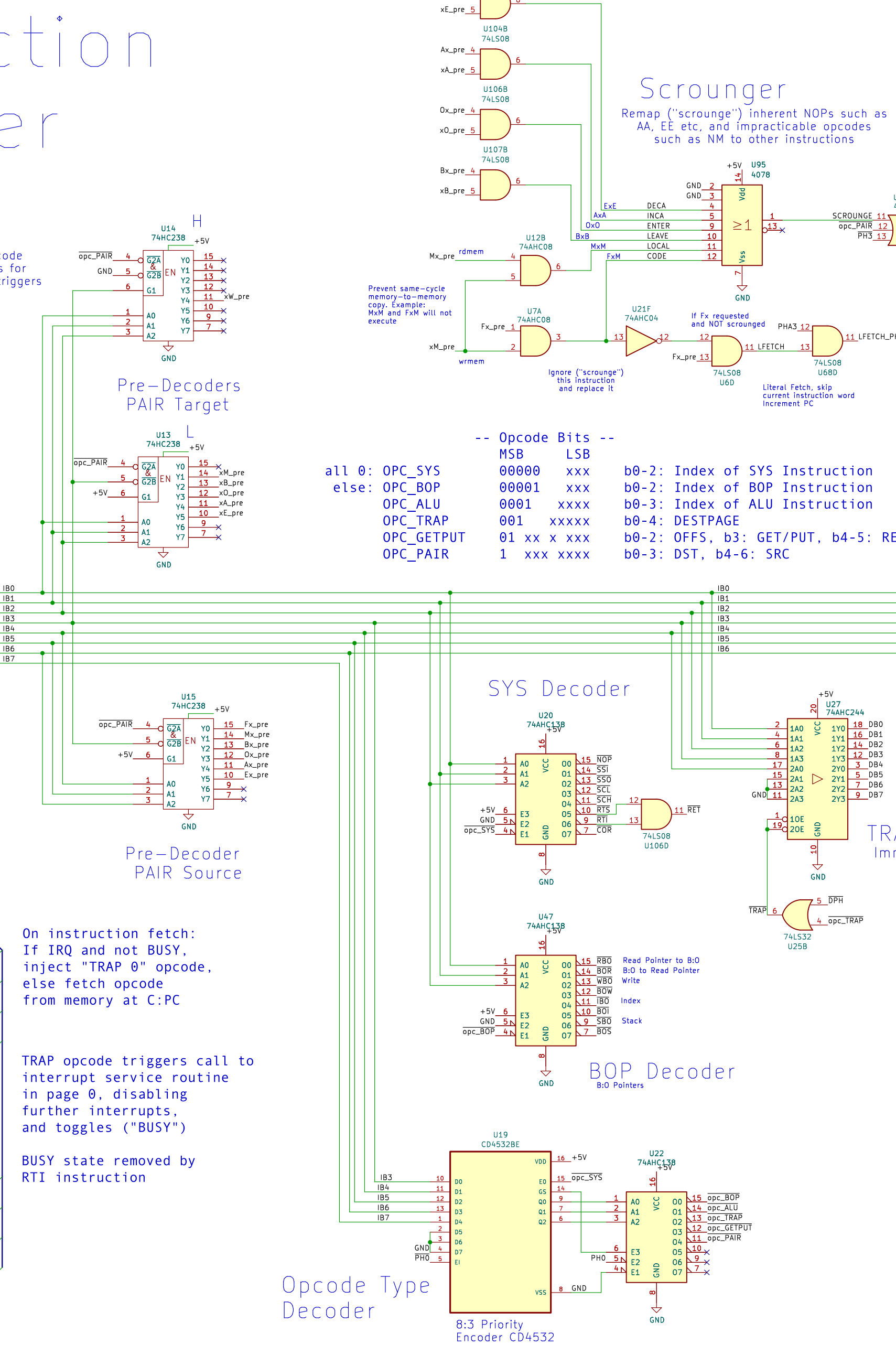
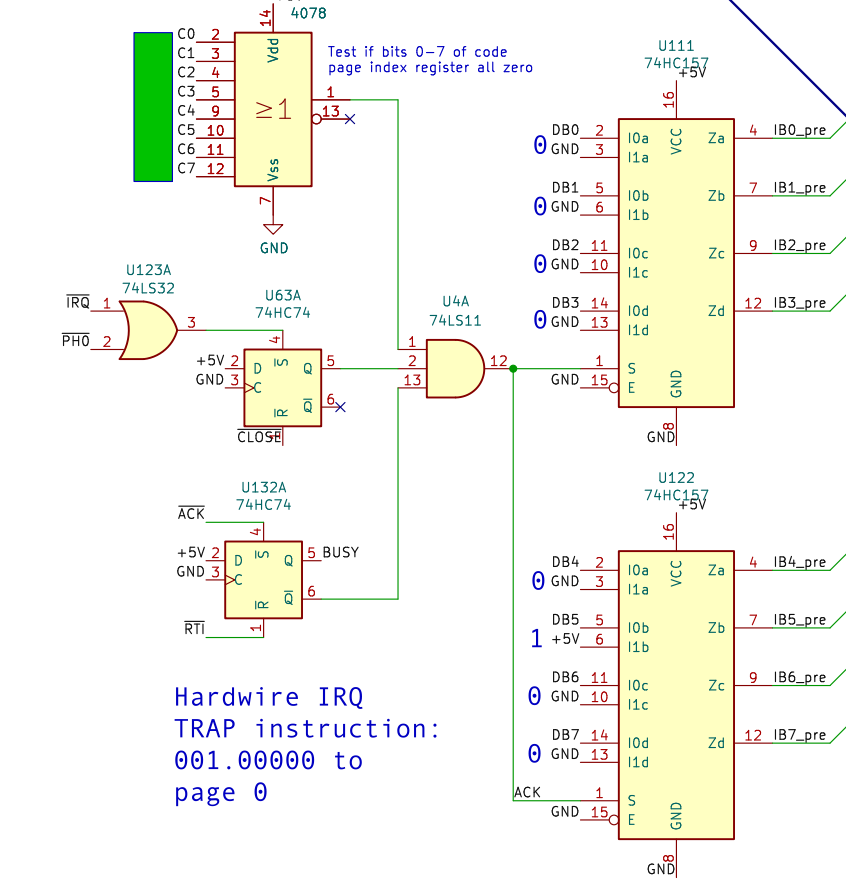
Reference Schematics

Rev. Myth

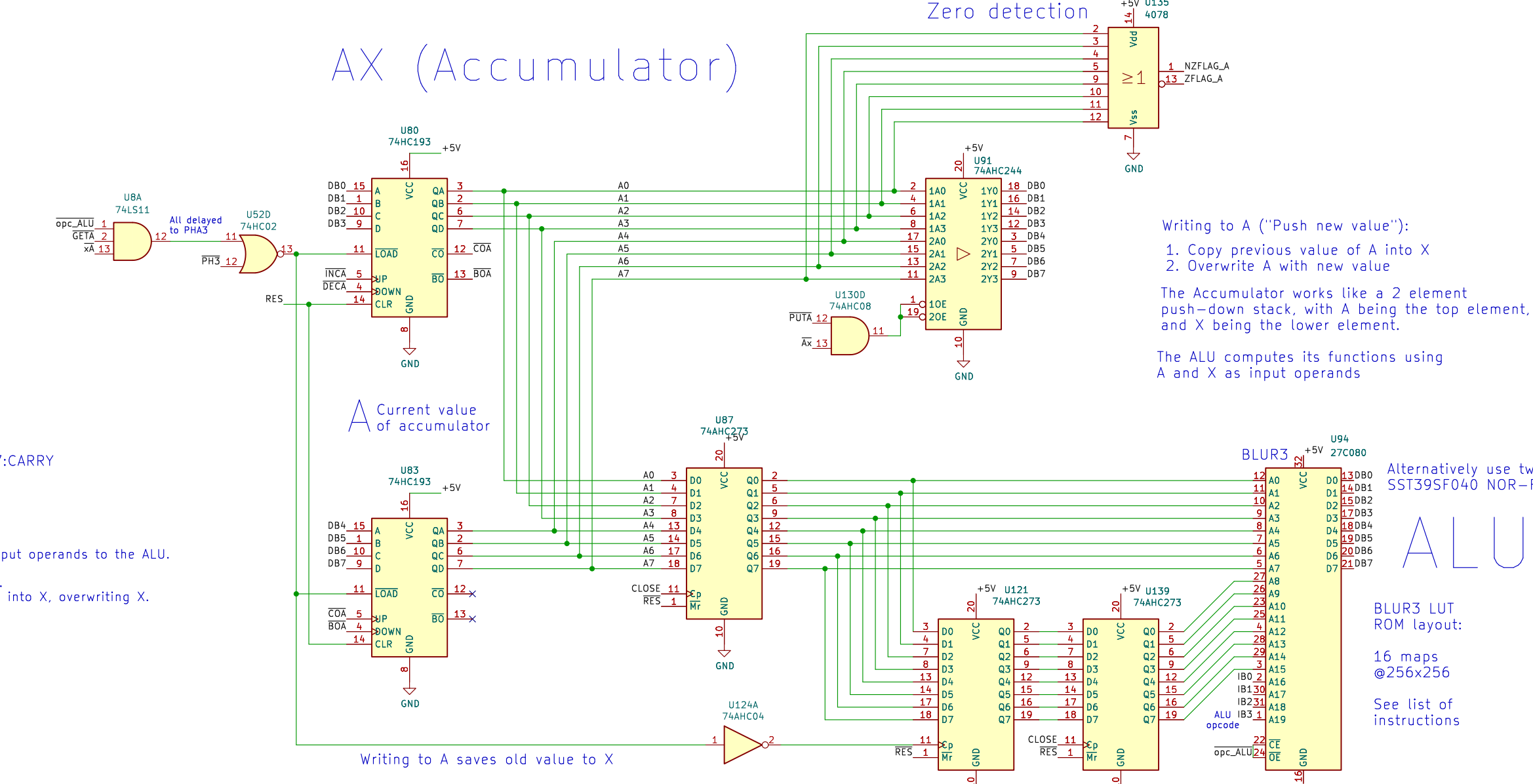
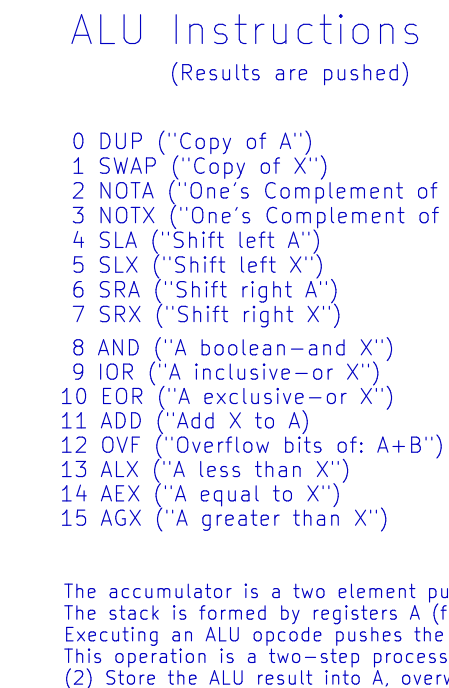
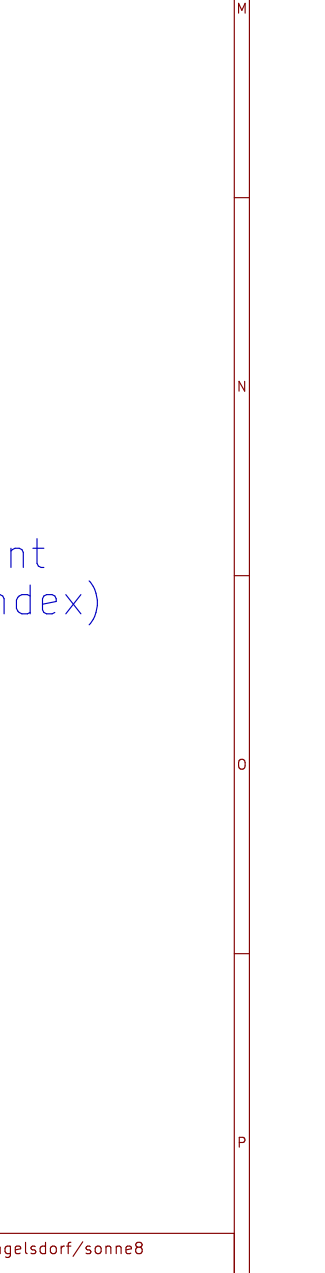
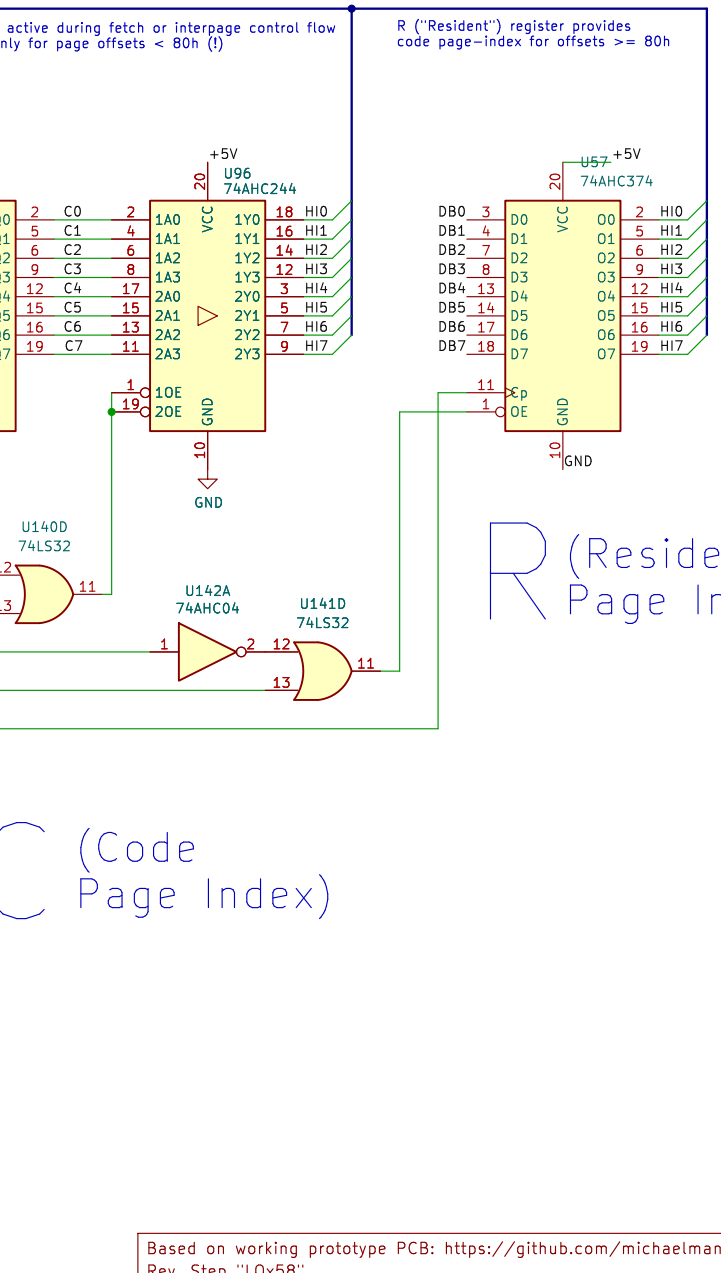
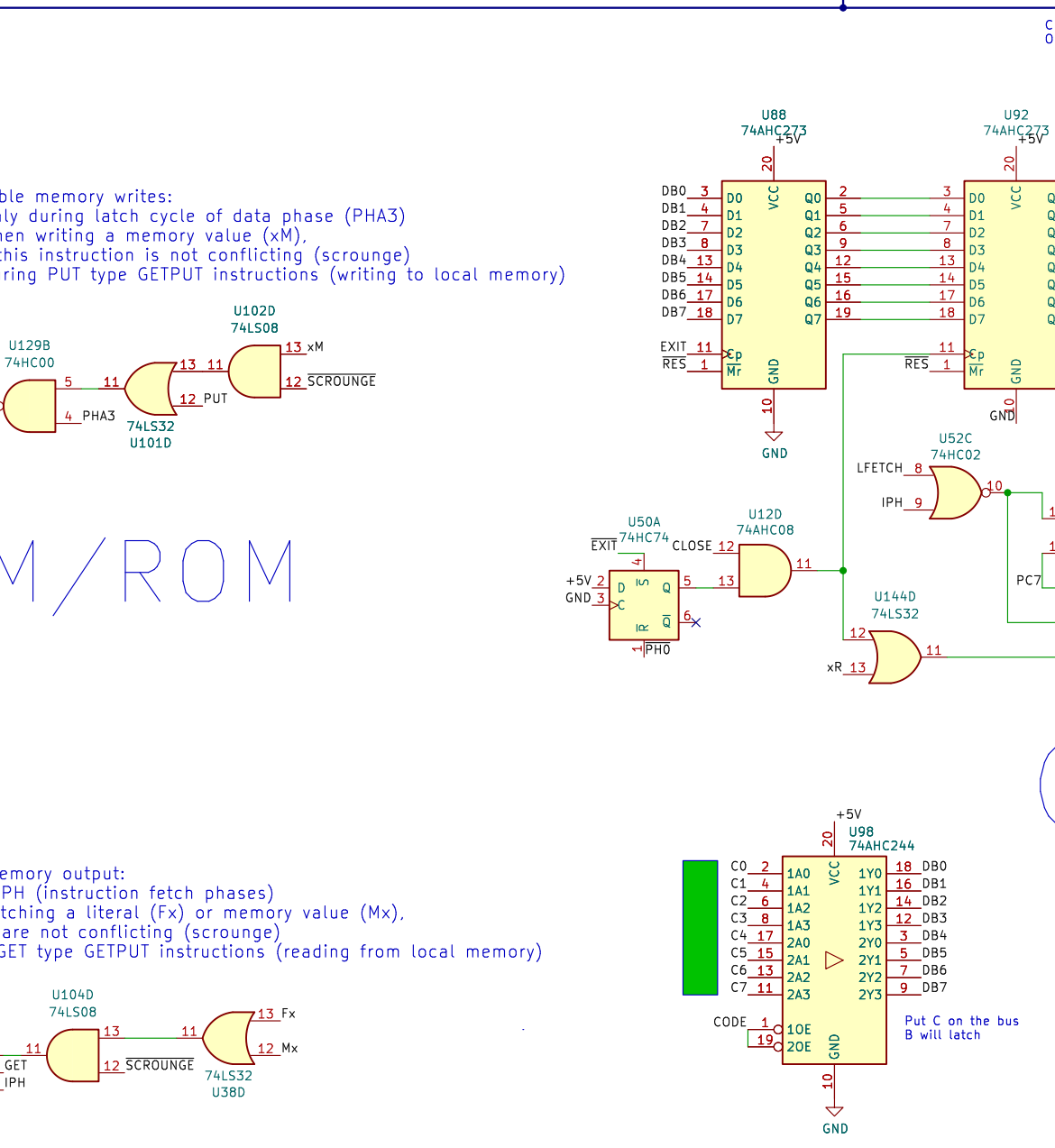
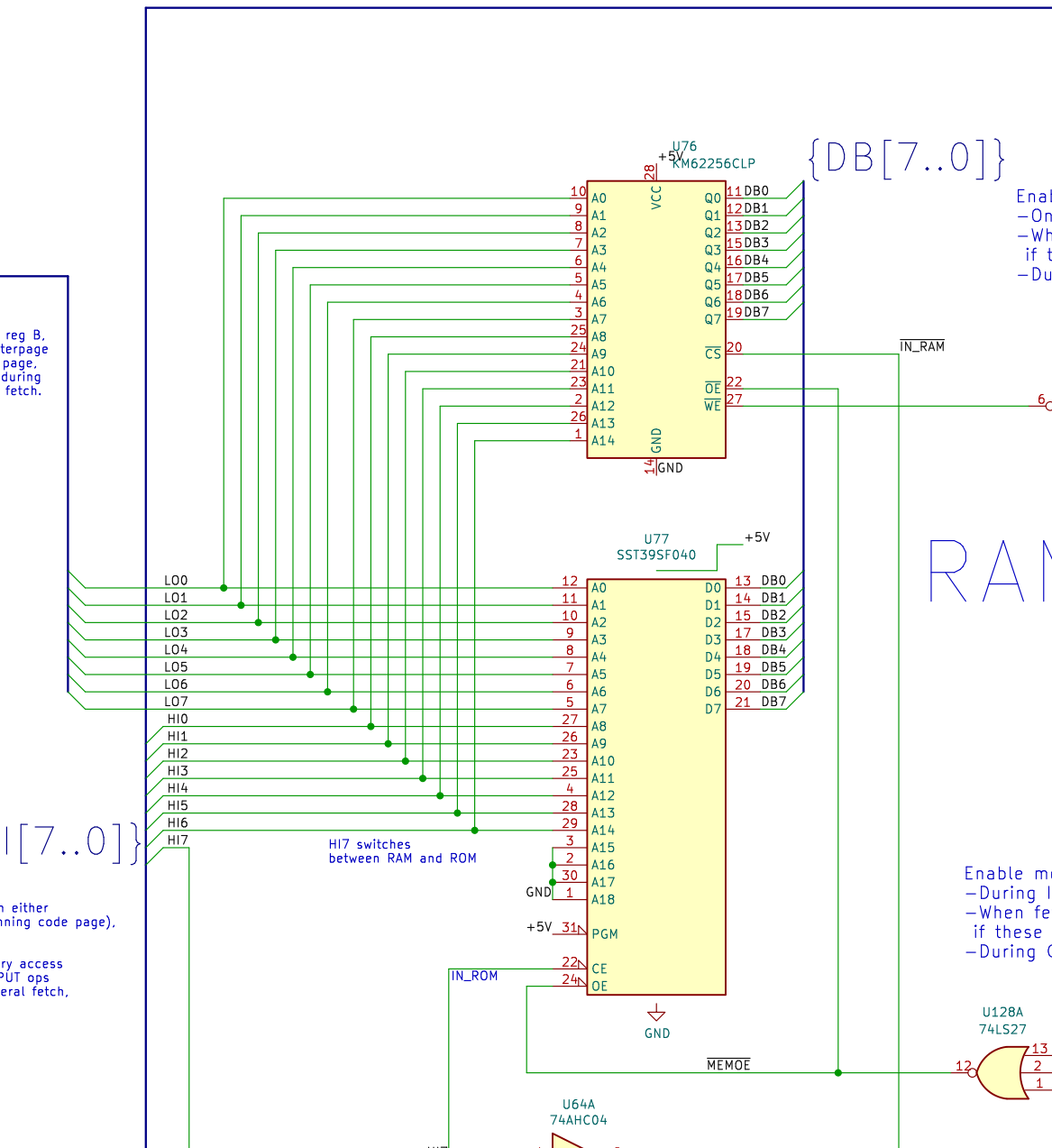
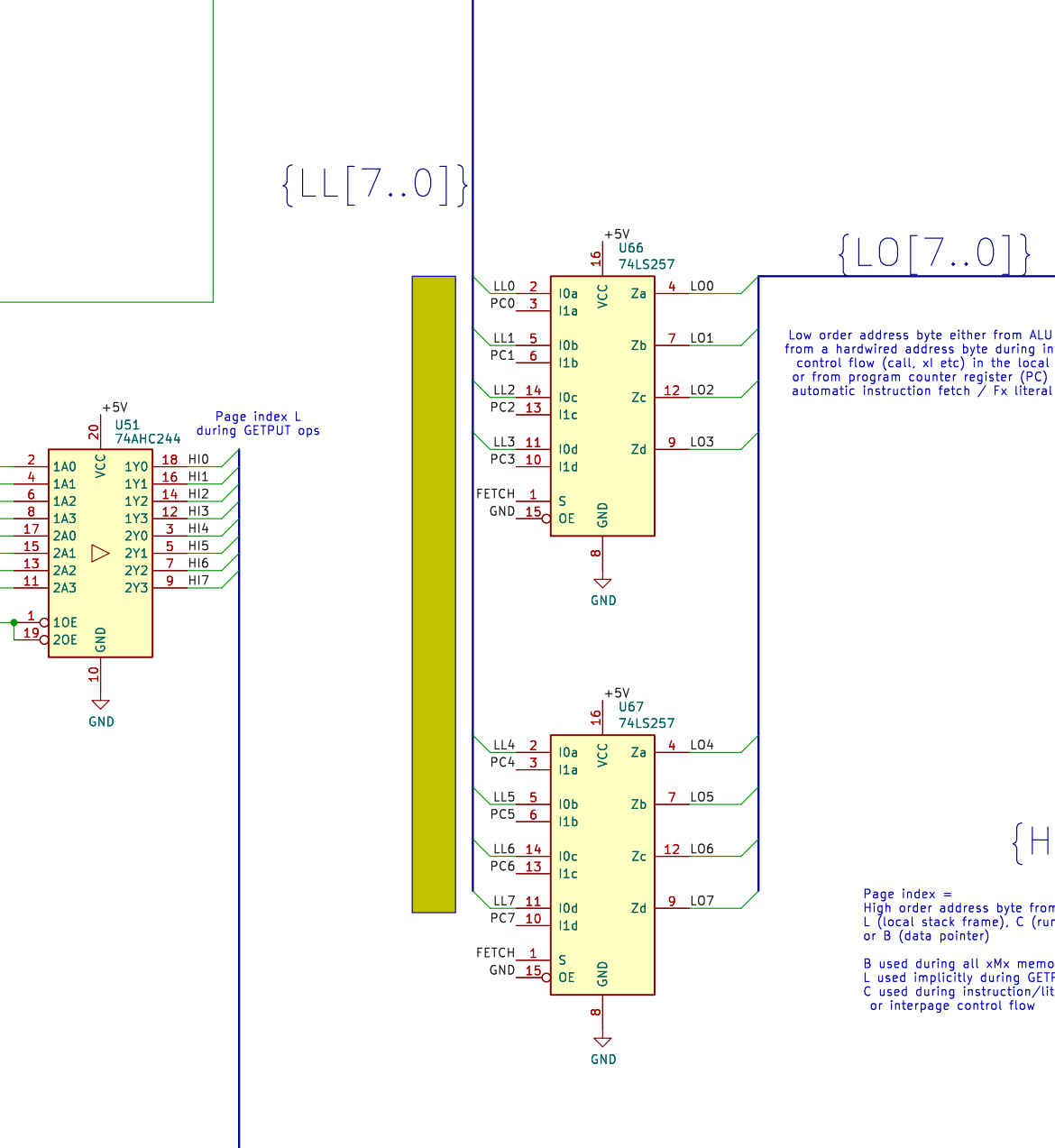
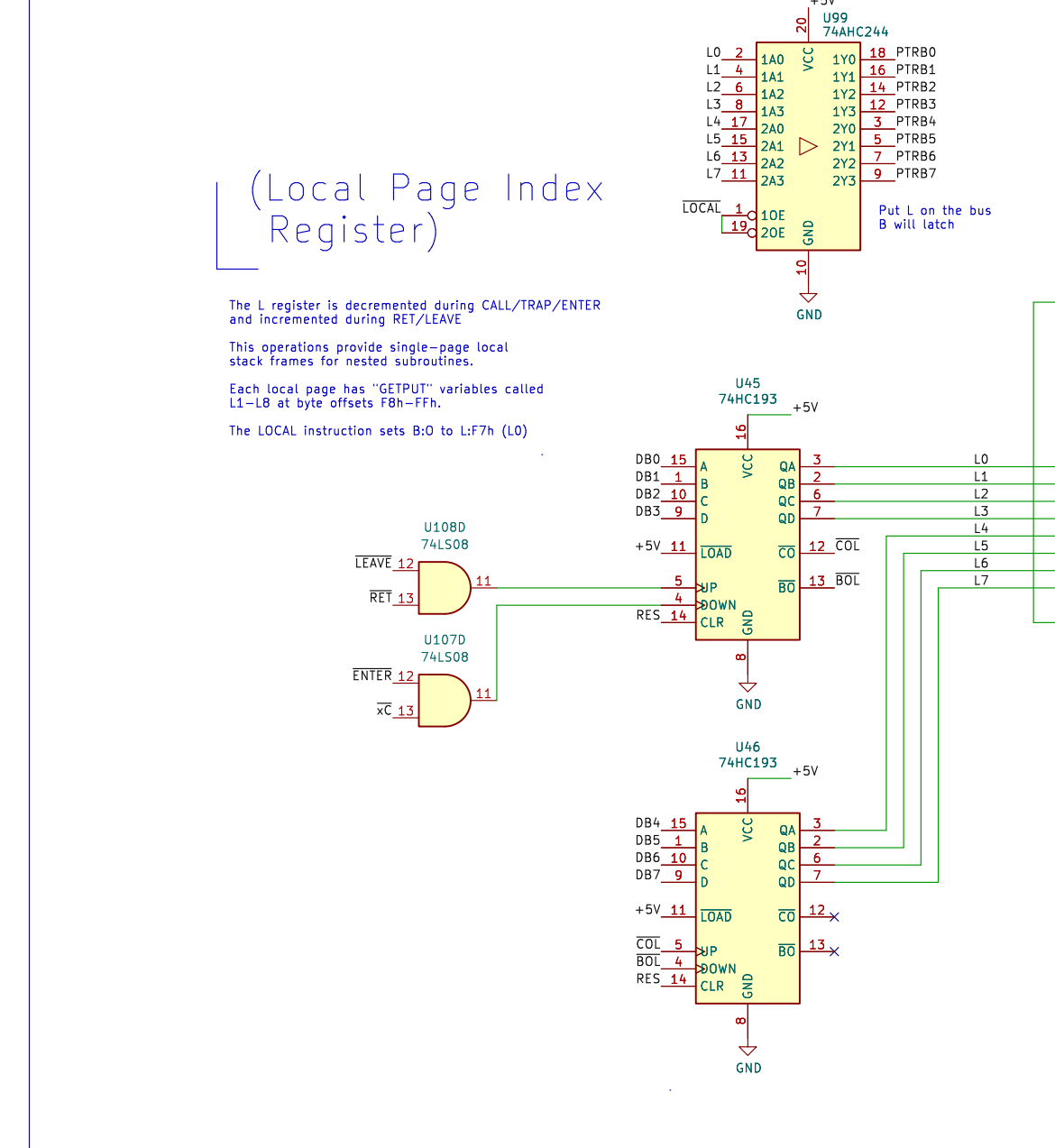
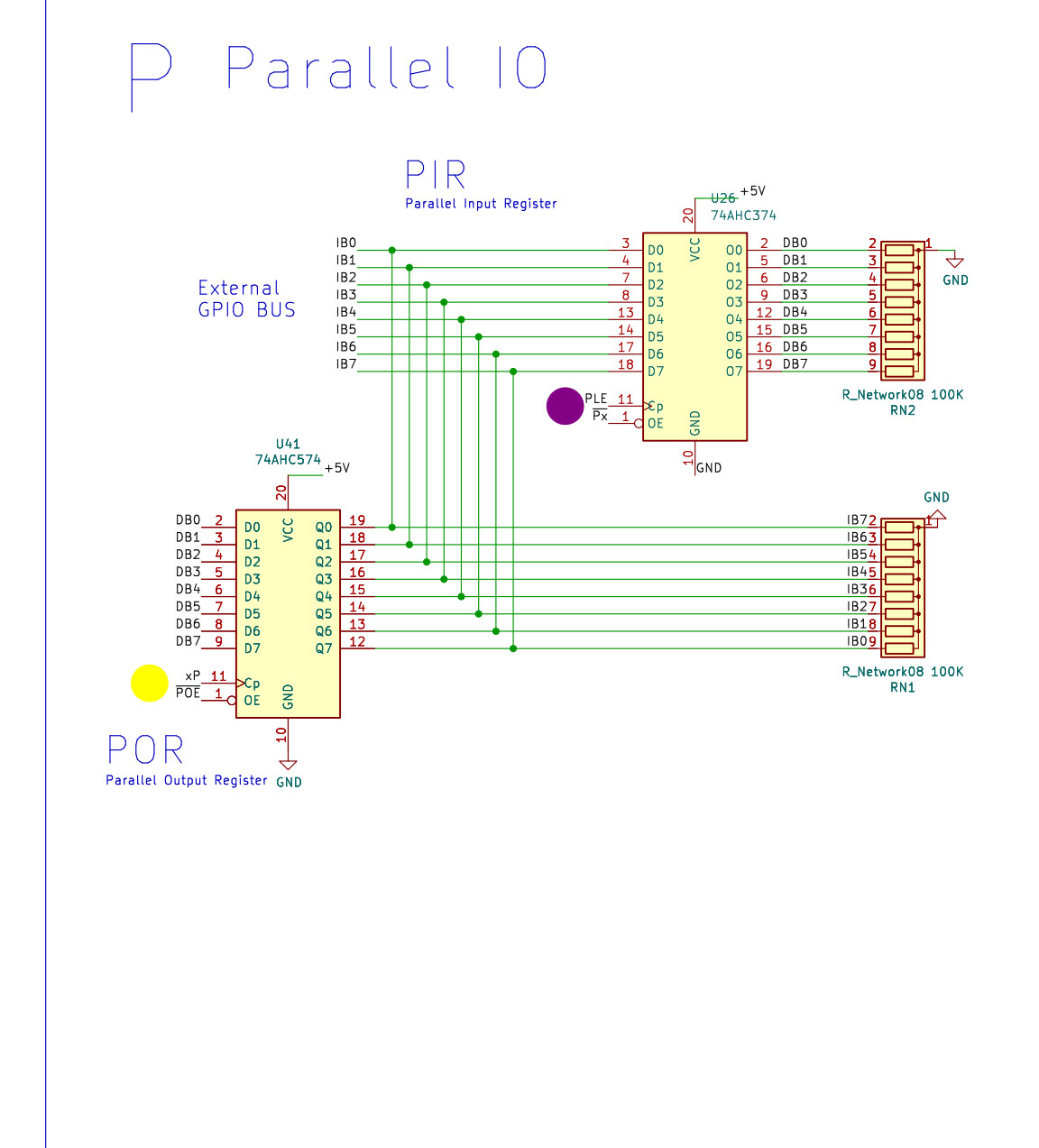
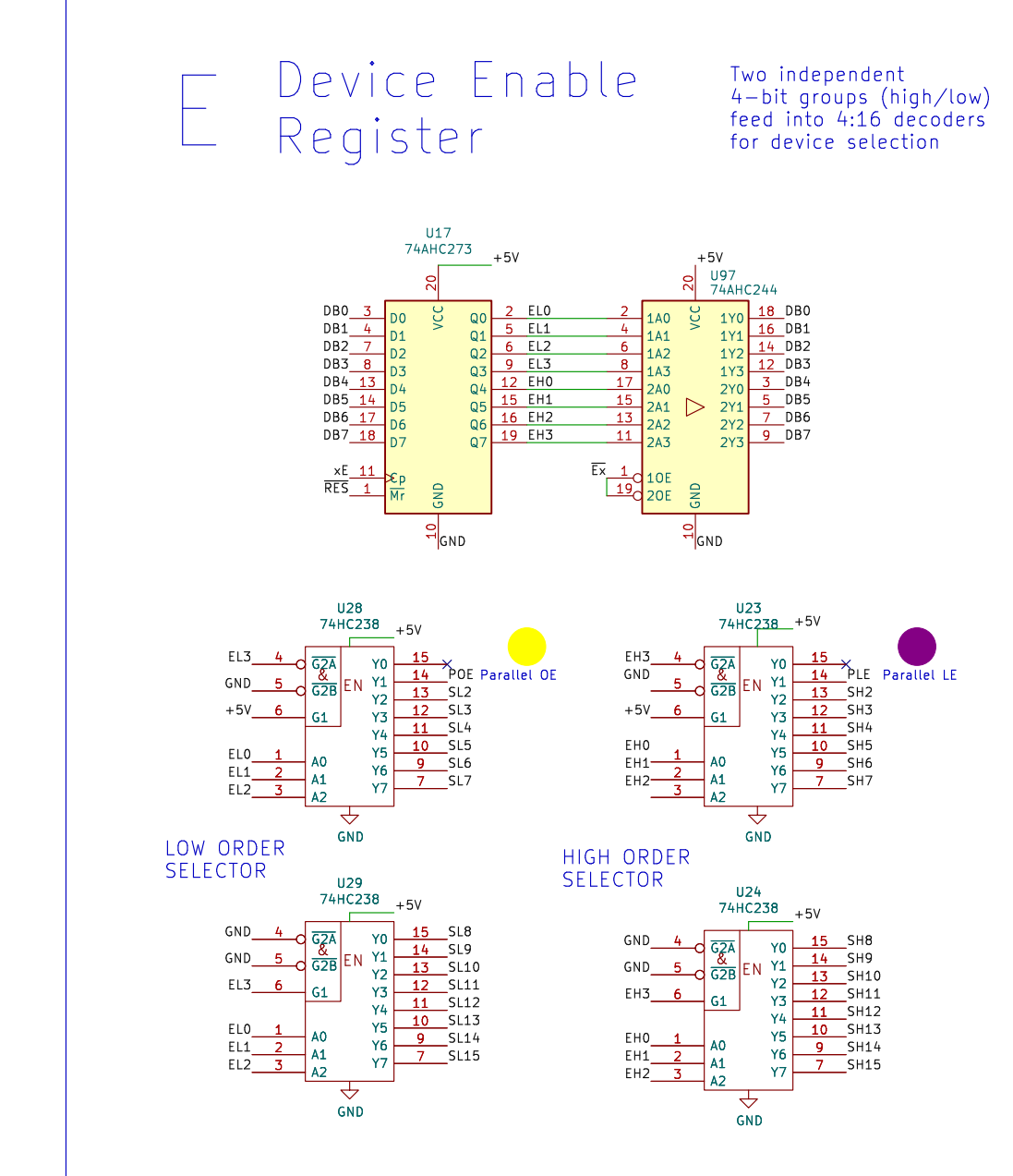
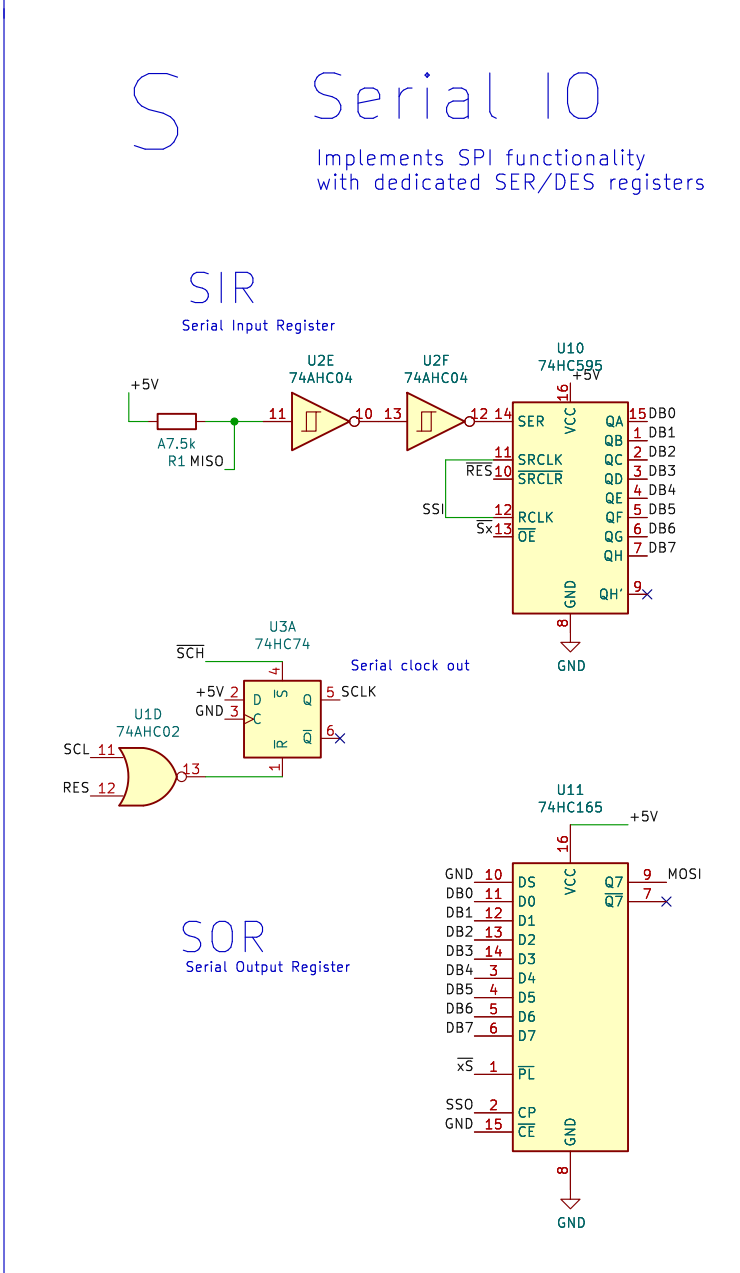
Instruction Decoder

Start, latch instruction or interrupt vector

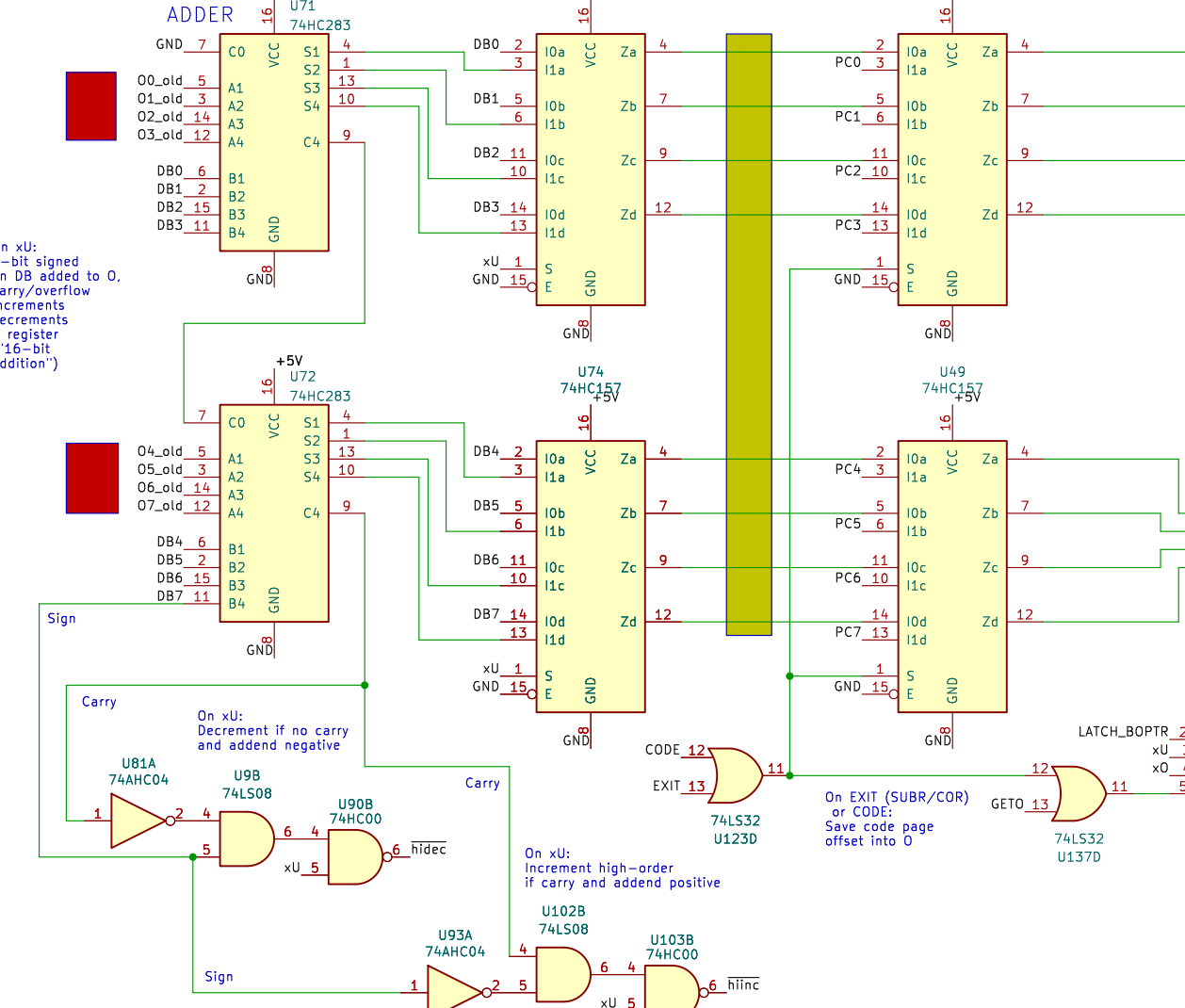
Interrupts disabled when "BUSY" and when running code in page 0 (See code page index reg schematics bottom right)



Input/Output

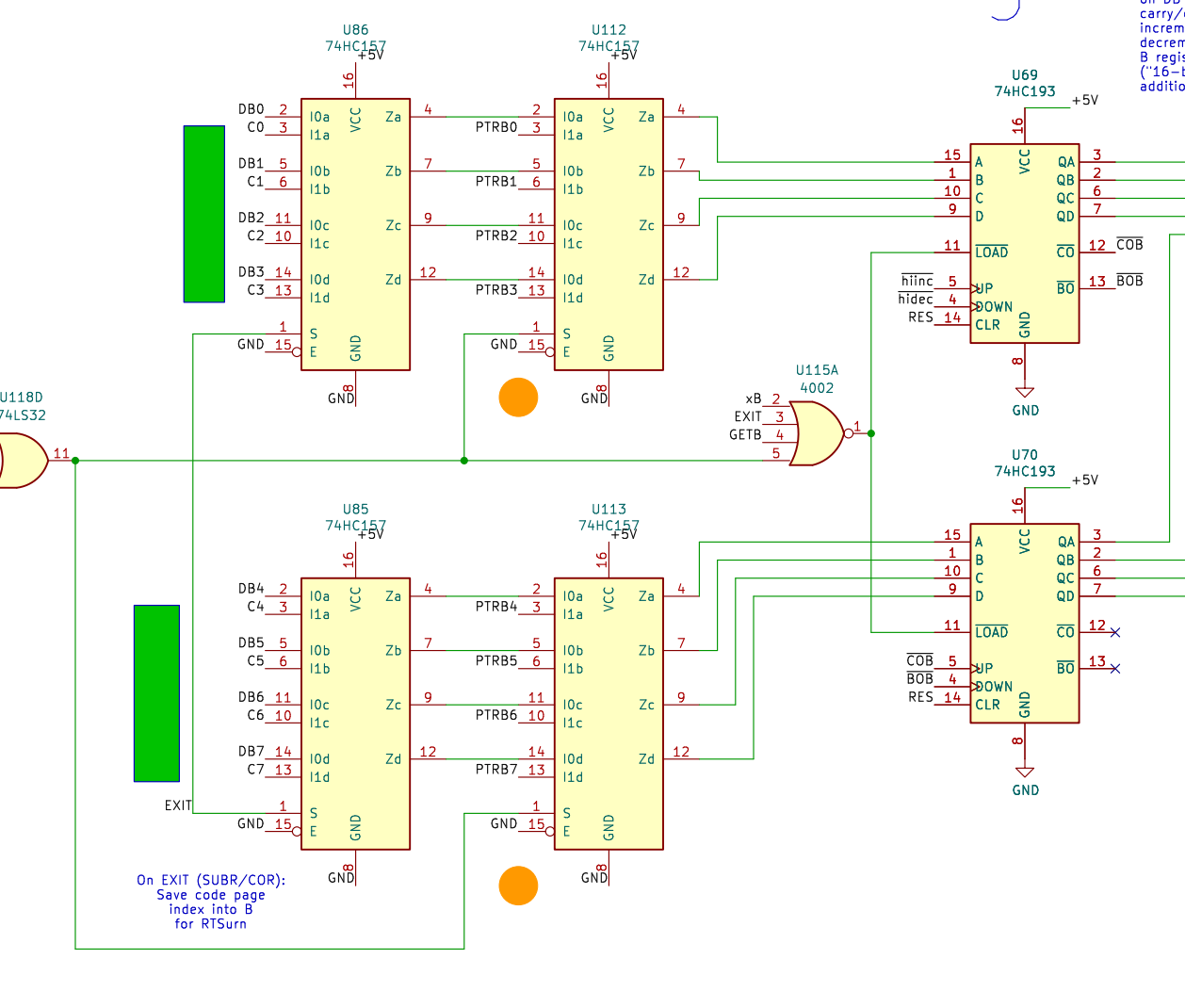


B:O Pointer



- Saves offset of current instruction byte during call/trap/cor
- Outputs return offset during RET
- Is the (only) implied address offset for memory read-write, with the corresponding page index stored in B (Base)
- Together with B forms 16-bit address pointers subject to the xU instruction.
- The B:O pointer can be loaded from/saved into the B0-Pointers P1-4

B:O Pointer



- Saves page index of current instruction byte during call/trap/cor
- Outputs return page index during RET
- Is the (only) implied page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
- The B:O pointer can be loaded from/saved into the B0-Pointers P1-4

B (Base) Page Index



RAM/ROM



- Enable memory writes
- Only during latch cycle of data phase (PHA3)
- When writing a literal (F) or memory value (M)
- If there are no conflicting (scrounger)
- During GET type GETPUT instructions (reading from local memory)

Page Index =
- If 0: order address byte after the ALU
- If 1: order address byte after the ALU
- If 2: order address byte after the ALU
- If 3: order address byte after the ALU

C (Code) Page Index



Page Index =
- If 0: order address byte after the ALU
- If 1: order address byte after the ALU
- If 2: order address byte after the ALU
- If 3: order address byte after the ALU