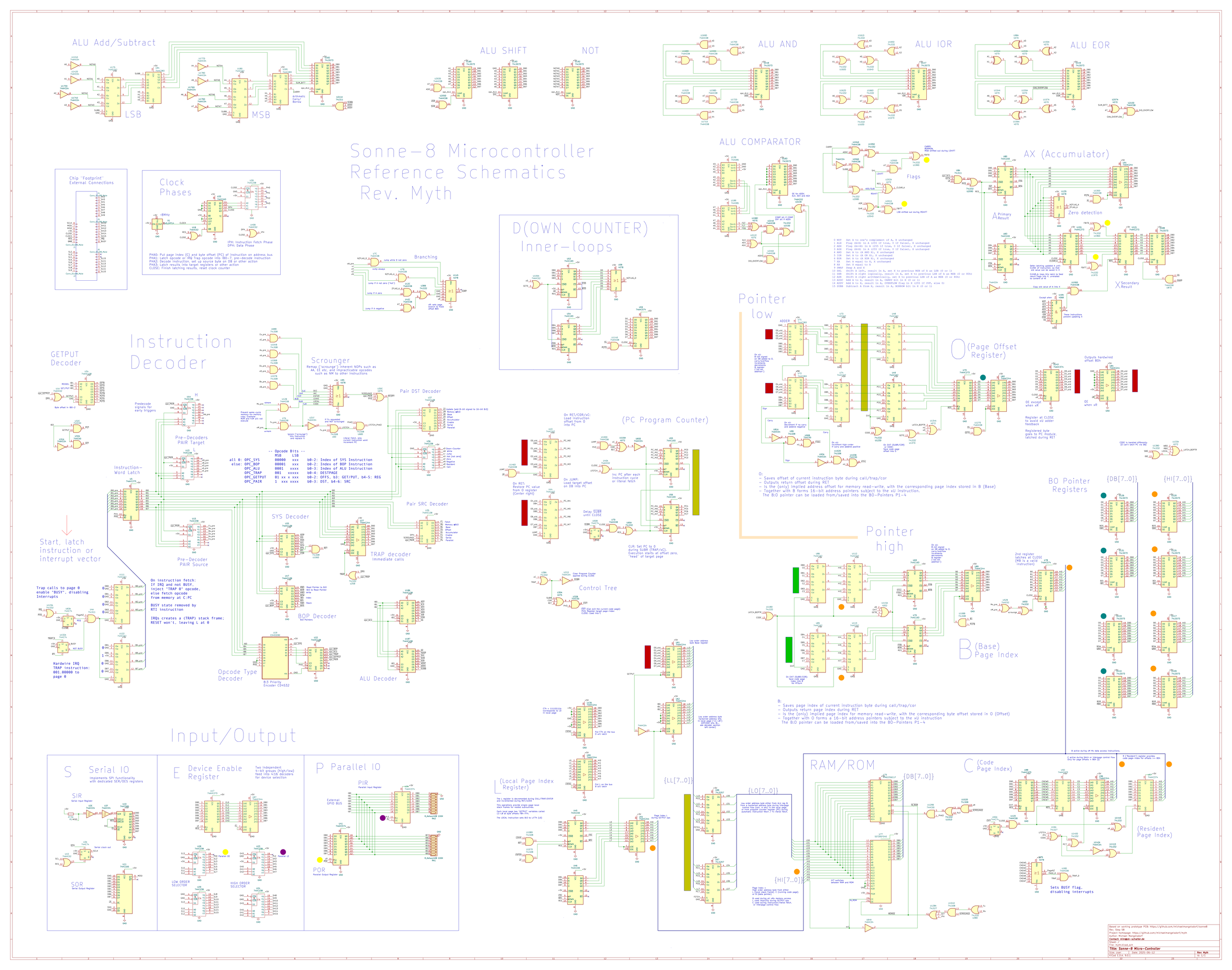
Sonne-8 Microcontroller
Reference Schematics
Rev. Myth
ALU Add/Subtract
LSB
MSB
ALU SHIFT
NOT
ALU AND
ALU IOR
ALU EOR
ALU COMPARATOR
Flags
AX (Accumulator)
Zero detection
Chip "Footprint" External Connections
Clock Phases
IPH: Instruction Fetch Phase
DPH: Data Phase
D(OWN COUNTER) Inner-loops
Branching
Pointer low
(Page Offset Register)
Pointer high
BO Pointer Registers
{DB[7..0]}
{HI[7..0]}
GETPUT Decoder
Instruction Decoder
Scrounger
Pair DST Decoder
Pair SRC Decoder
(PC Program Counter)
Predecode signals for early triggers
Pre-Decoders PAIR Target
Pre-Decoder PAIR Source
Instruction-Word Latch
Start, latch instruction or interrupt vector
SYS Decoder
TRAP decoder
Immediate calls
BOP Decoder
Control Tree
Opcode Type Decoder
ALU Decoder
Trap calls to page 0 enable "BUSY", disabling Interrupts
Hardwire IRQ TRAP instruction: 001.00000 to page 0
Input/Output
S Serial IO
Implements SPI functionality with dedicated SER/DES registers
SIR
Serial Input Register
SOR
Serial Output Register
E Device Enable Register
Two independent 4-bit groups (high/low) feed into 4:16 decoders for device selection
LOW ORDER SELECTOR
HIGH ORDER SELECTOR
P Parallel IO
PIR
Parallel Input Register
POR
Parallel Output Register
(Local Page Index Register)
{LL[7..0]}
{LO[7..0]}
{HI[7..0]}
RAM/ROM
C (Code Page Index)
(Resident Page Index)
Sets BUSY flag, disabling interrupts
Title: Sonne-8 Micro-Controller
Rev: Myth