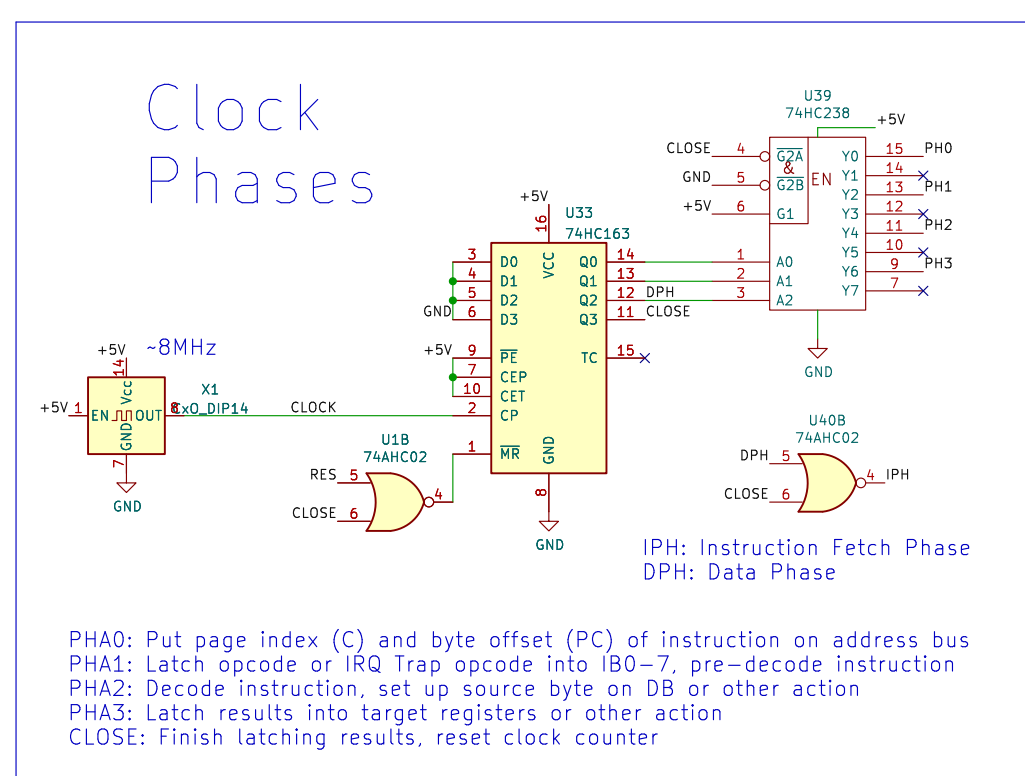
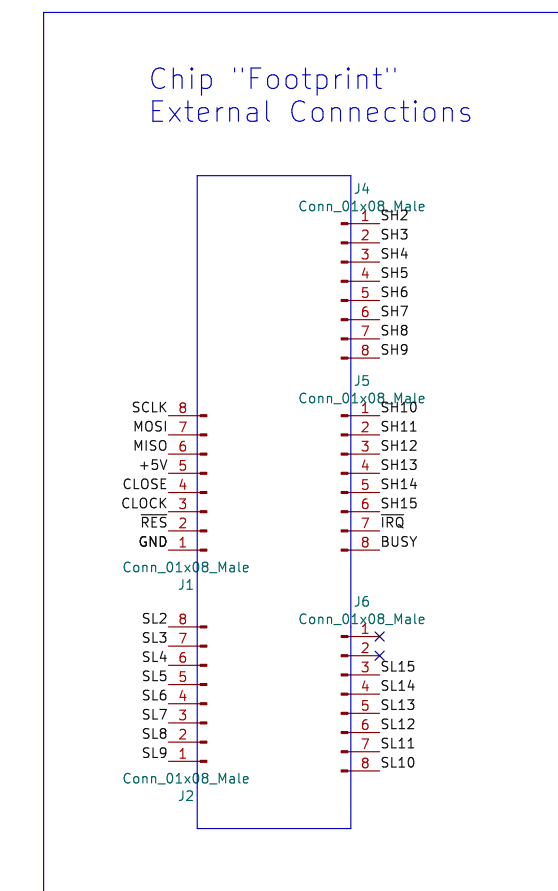


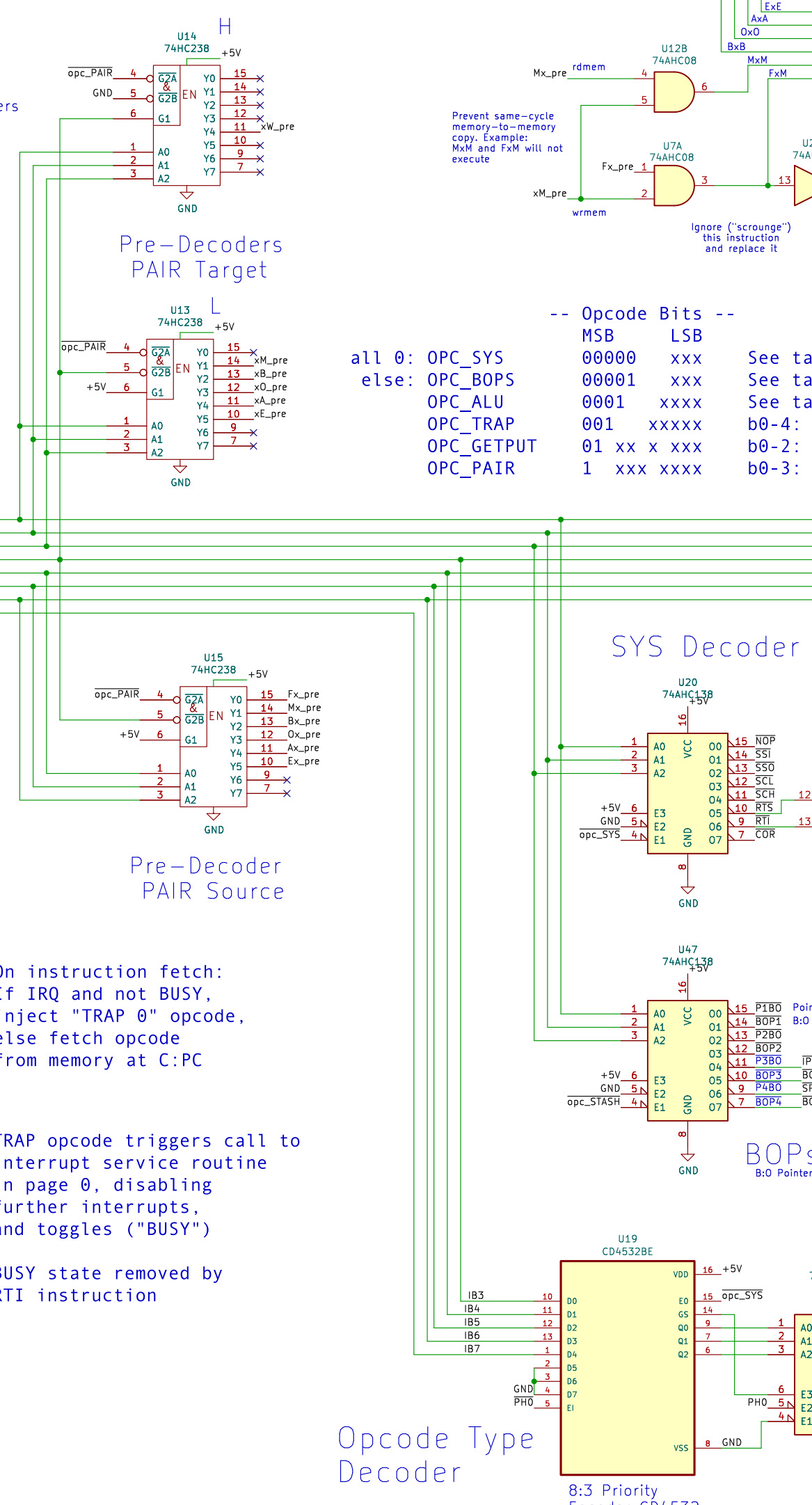
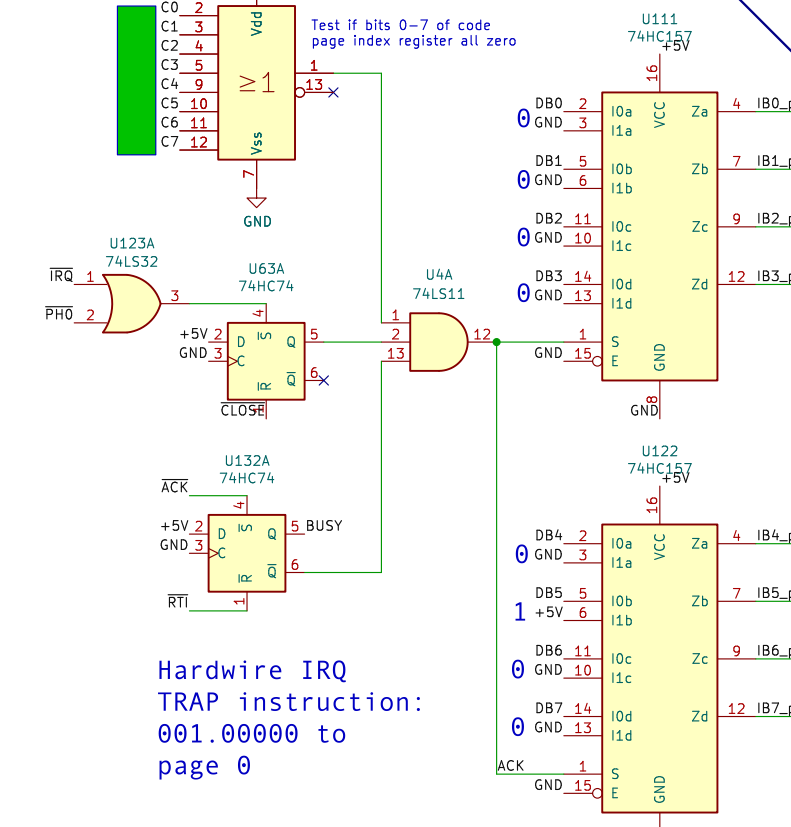
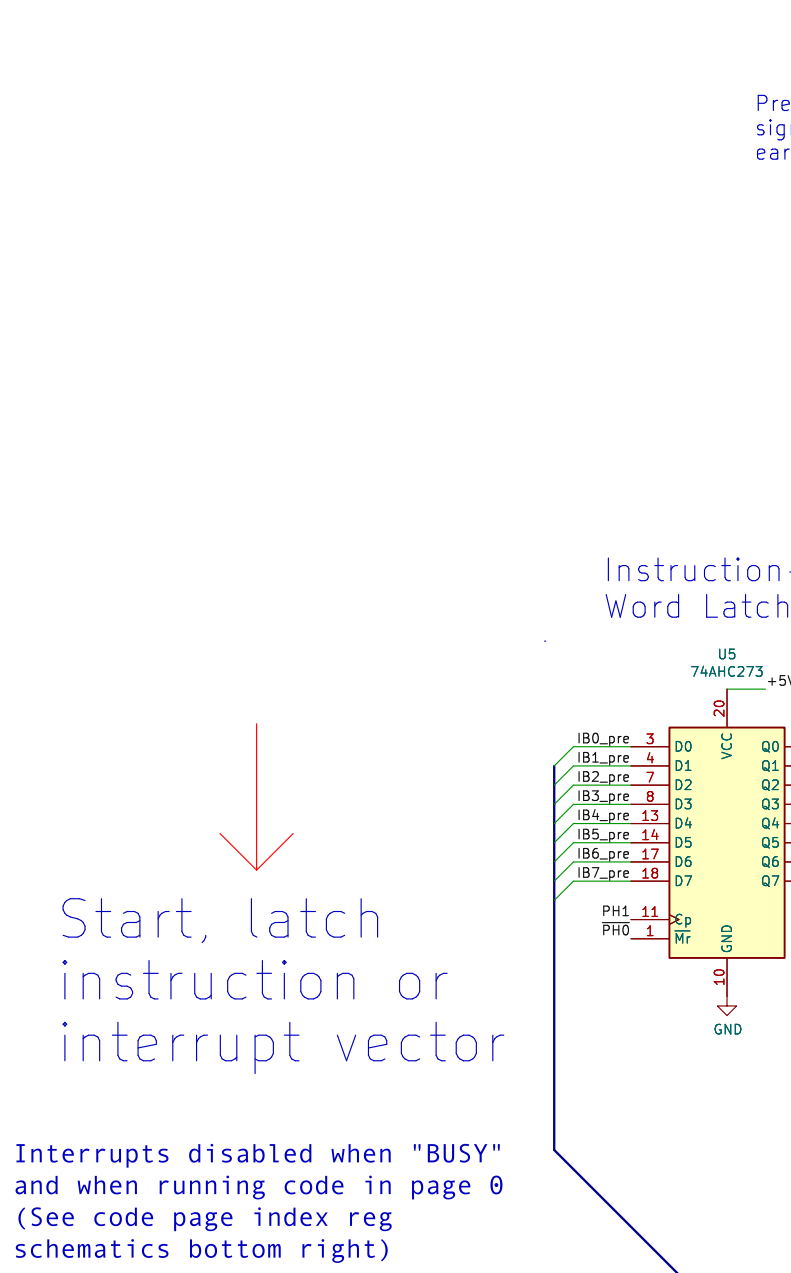
Sonne-8 Microcontroller

Reference Schematics

Rev. Myth

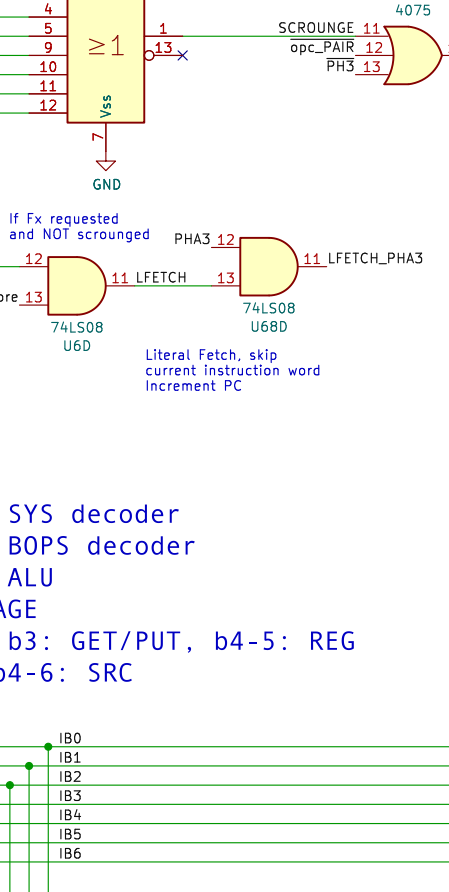


Instruction Decoder



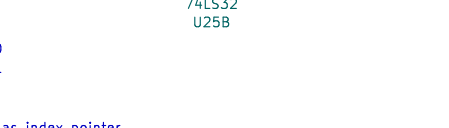
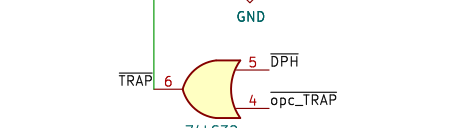
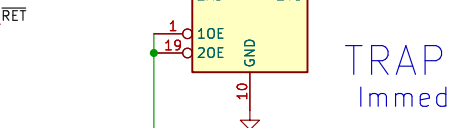
Scrounger

Remap ("scrounge") inherent NOPs such as AA, EE, etc. and impracticable opcodes such as 00 to other instructions



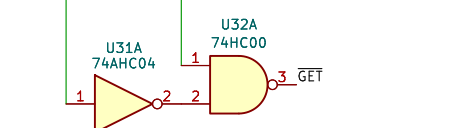
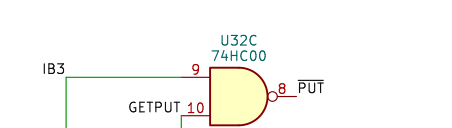
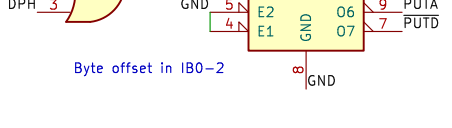
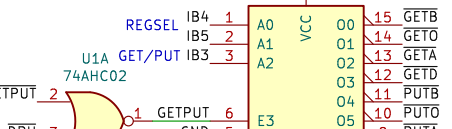
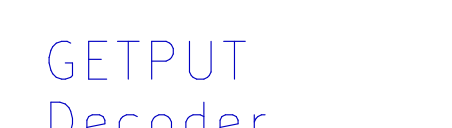
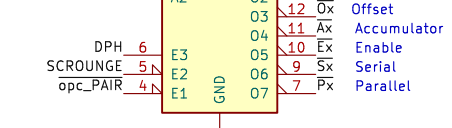
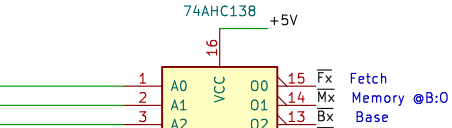
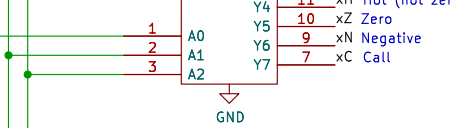
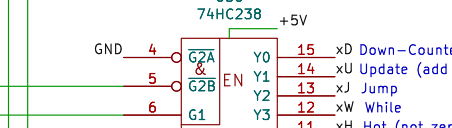
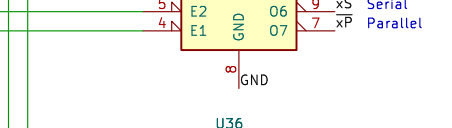
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



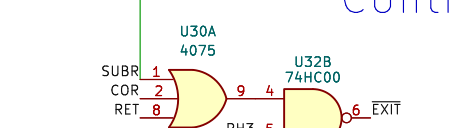
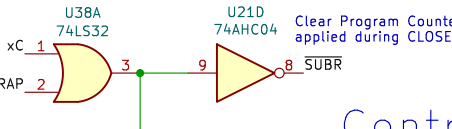
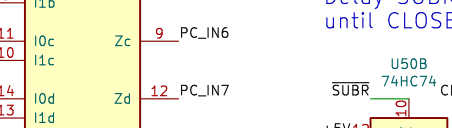
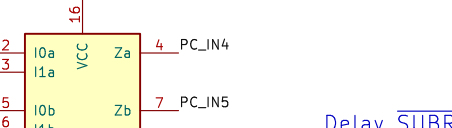
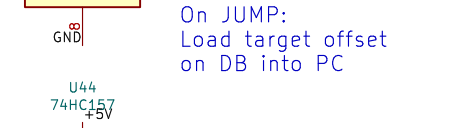
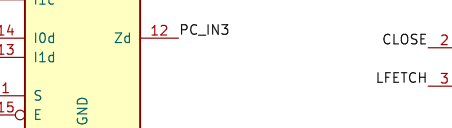
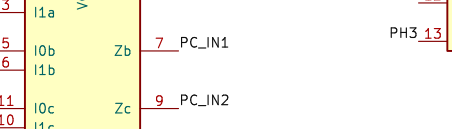
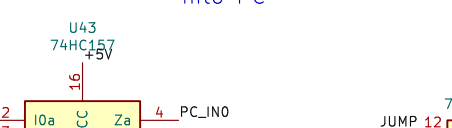
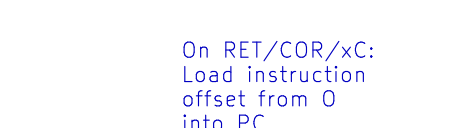
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



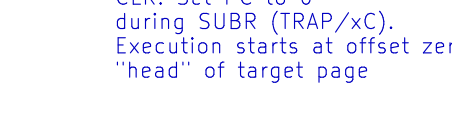
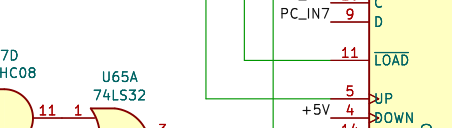
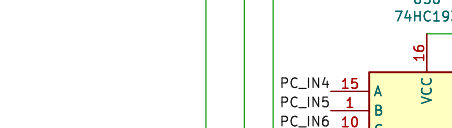
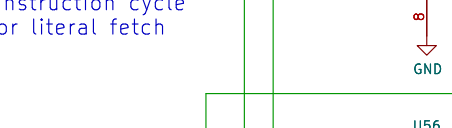
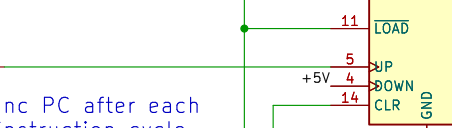
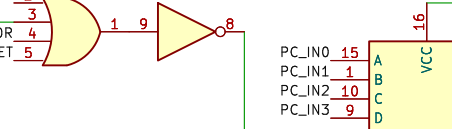
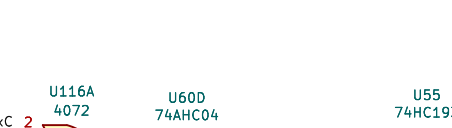
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



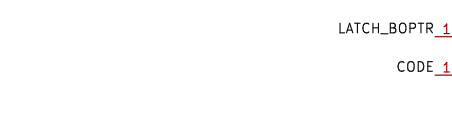
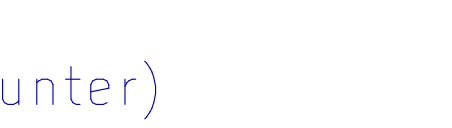
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



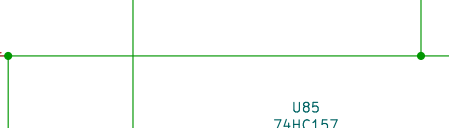
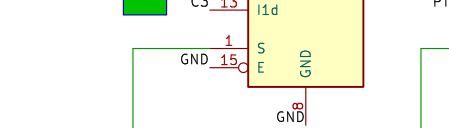
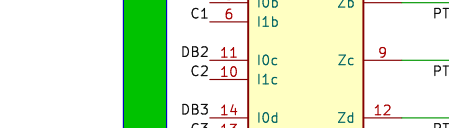
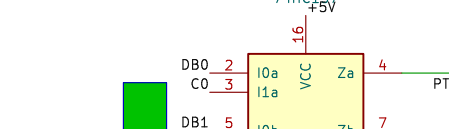
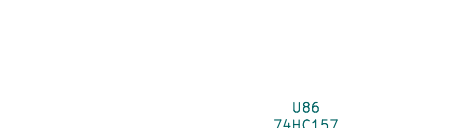
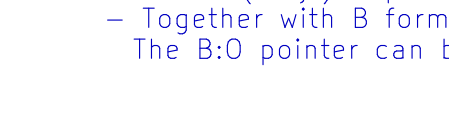
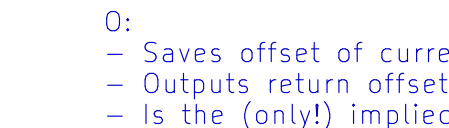
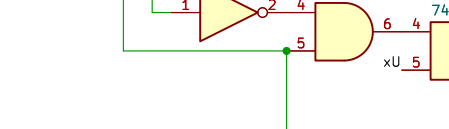
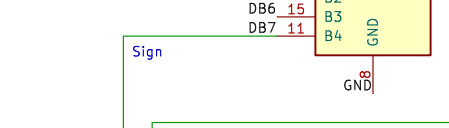
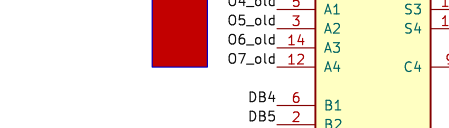
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



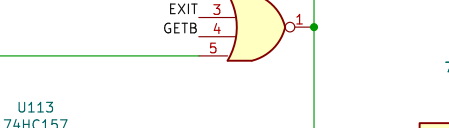
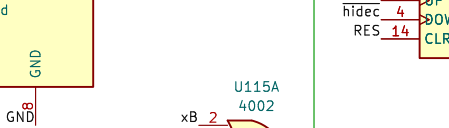
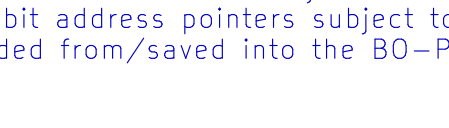
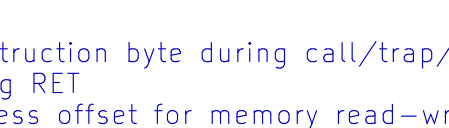
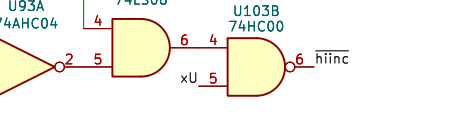
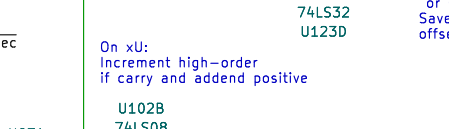
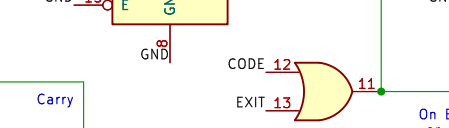
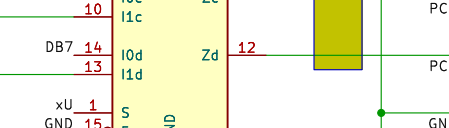
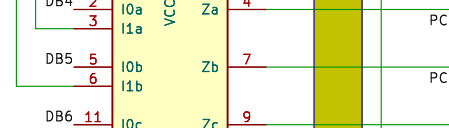
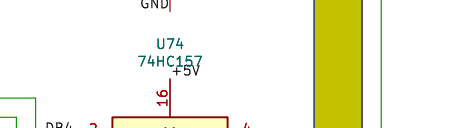
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



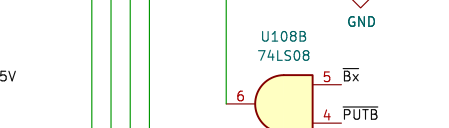
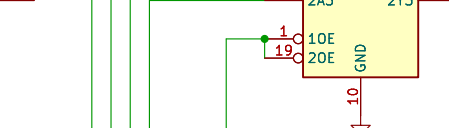
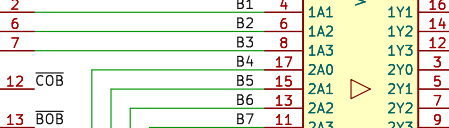
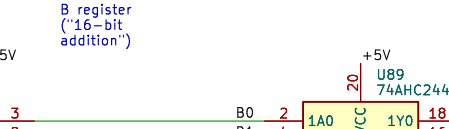
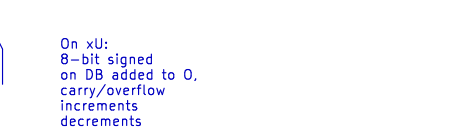
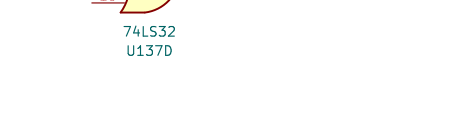
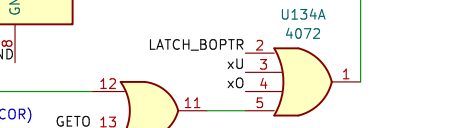
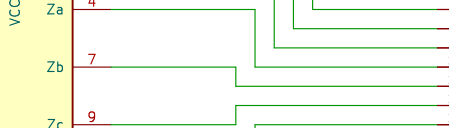
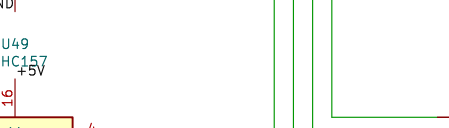
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



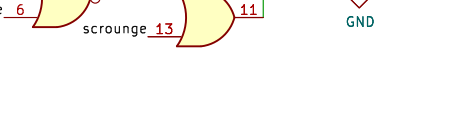
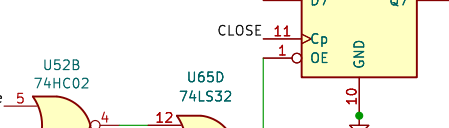
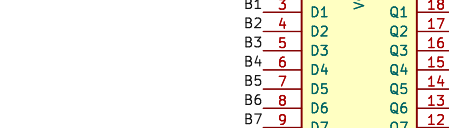
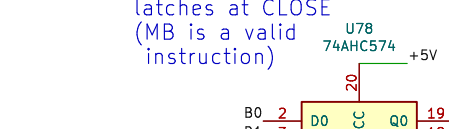
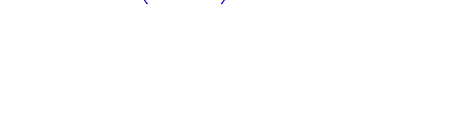
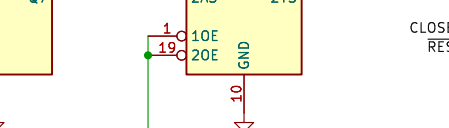
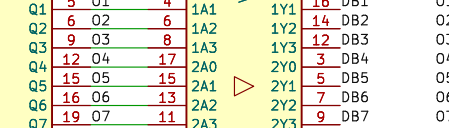
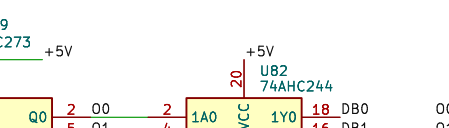
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



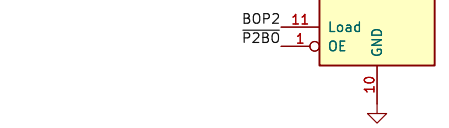
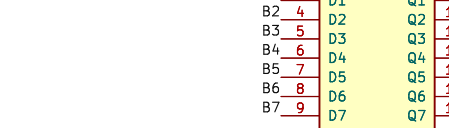
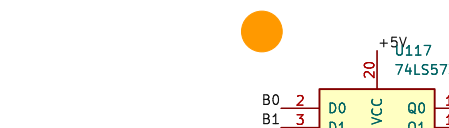
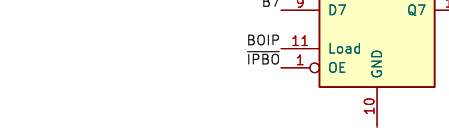
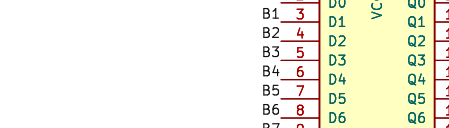
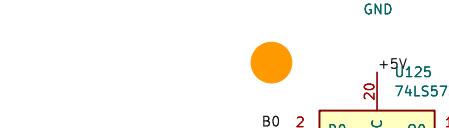
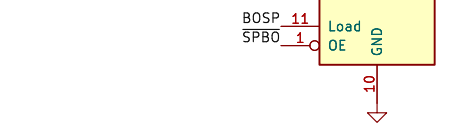
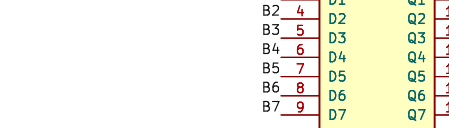
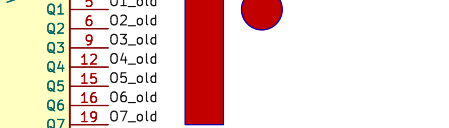
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



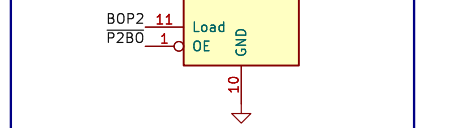
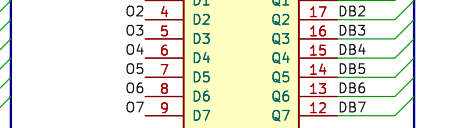
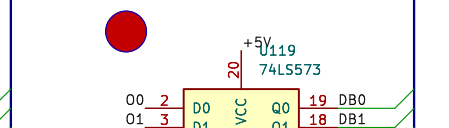
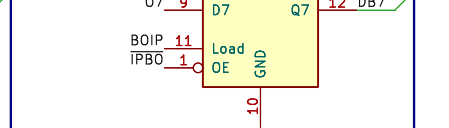
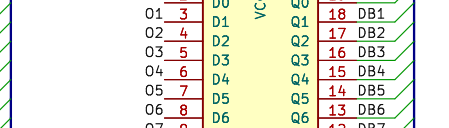
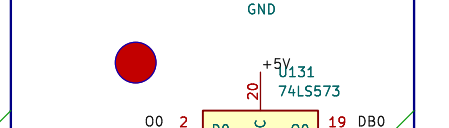
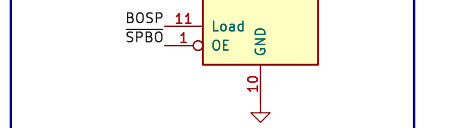
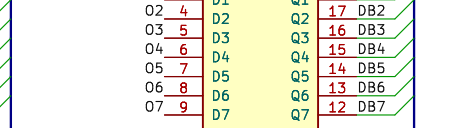
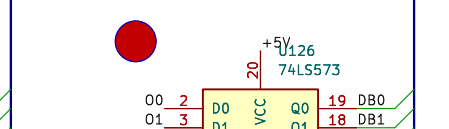
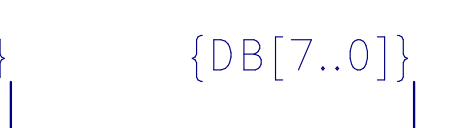
Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



Pair SRC Decoder

On RET/COR/C: Load instruction offset from 0 into PC



Input/Output

