Sonne-8 Microcontroller
Reference Schematics
Rev. Myth
Chip "Footprint" External Connections
Clock Phases
D(OWN COUNTER) Inner-loops
A (Accumulator)
Zero detection
ALU Instructions
0 DUP ("Copy A") A:=A
1 SWAP ("Copy PREV") A:=PREV
2 OCA ("One's Complement A") A:=~A
3 OCP ("One's Complement PREV") A:=~PREV
4 SLA ("A shifted left") A:=A<<1
5 SLP ("PREV shifted left") A:=PREV<<1
6 SRA ("A shifted right") A:=A>>1
7 SRP ("PREV shifted right") A:=PREV>>1
8 AND ("A boolean-and PREV") A:=A&PREV
9 IOR ("A inclusive-or PREV") A:=A|PREV
10 EOR ("A exclusive-or PREV") A:=A^PREV
11 ADD ("Add PREV to A) A:=A+PREV, bits 0-7
12 CAR ("Carry bit of: A plus PREV") A:=9th bit of: A+PREV, 0 or 1
13 ALP ("A less than PRE") A:=(A<PREV)? 0xFF:0
14 AEP ("A equal to PRE") A:=(A==PREV)? 0xFF:0
15 AGP ("A greater than PREV") A:=(A>PREV)? 0xFF:0
ALU
PREV
Instruction Decoder
Branching
Scrounger
Pair DST Decoder
Pre-Decoders PAIR Target
Instruction byte:
all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_BOPS 00001 xxx See table @ BOPS decoder
OPC_ALU 0001 xxxx See table @ ALU
OPC_TRAP 001 xxxxx b0-4: DEST PAGE
OPC_GETPUT 01 xx x xxx b0-2 OFFS, b3:GET/PUT, B4-5:REG(GETPUT)
OPC_PAIR 1 xxx xxxx b0-3 DST, b4-6 SRC
Instruction-Word Latch
Start, latch instruction or interrupt vector
Pair SRC Decoder
SYS Decoder
TRAP decoder Immediate calls
Pre-Decoder PAIR Source
GETPUT Decoder
BOPs Decoder
Opcode Type Decoder
(PC Program Counter)
Control Tree
B:O Pointer low
O (Page Offset Register)
B:O Pointer high
B (Base) Page Index
BO Pointer Registers
{PTRB[7..0]}
{DB[7..0]}
Input/Output
S Serial IO
E Device Enable Register
P Parallel IO
L (Local Page Index Register)
{LL[7..0]}
{LO[7..0]}
{HI[7..0]}
RAM/ROM
R (RESIDENT Page-Index)
C (CODE Page-Index)
Based on working prototype PCB: https://github.com/michaelmangelsdorf/sonne8
Rev. Step "Lox"
Project homepage: https://github.com/michaelmangelsdorf/myth
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