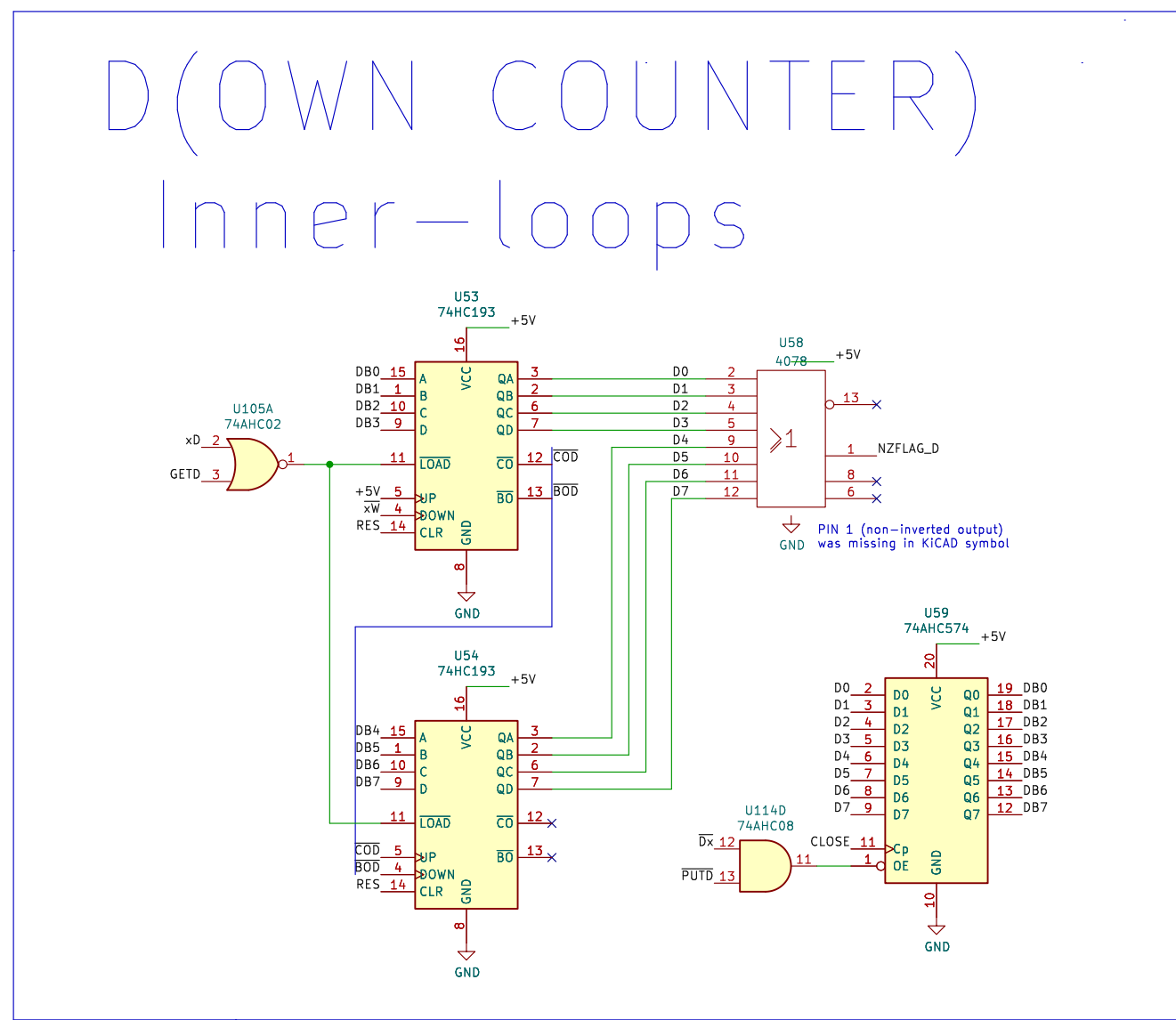


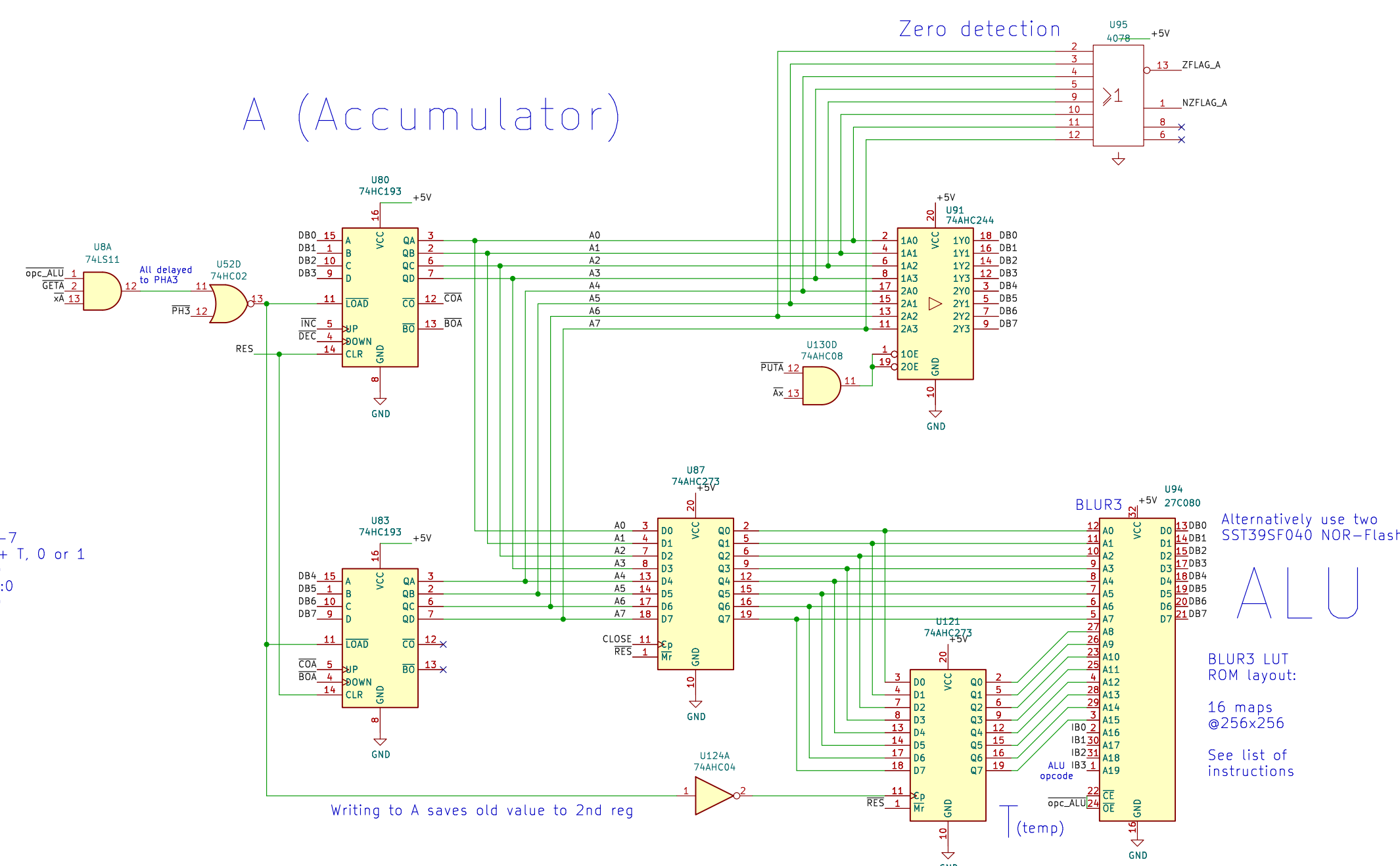
Sonne-8 Microcontroller Reference Schematics Rev. Myth



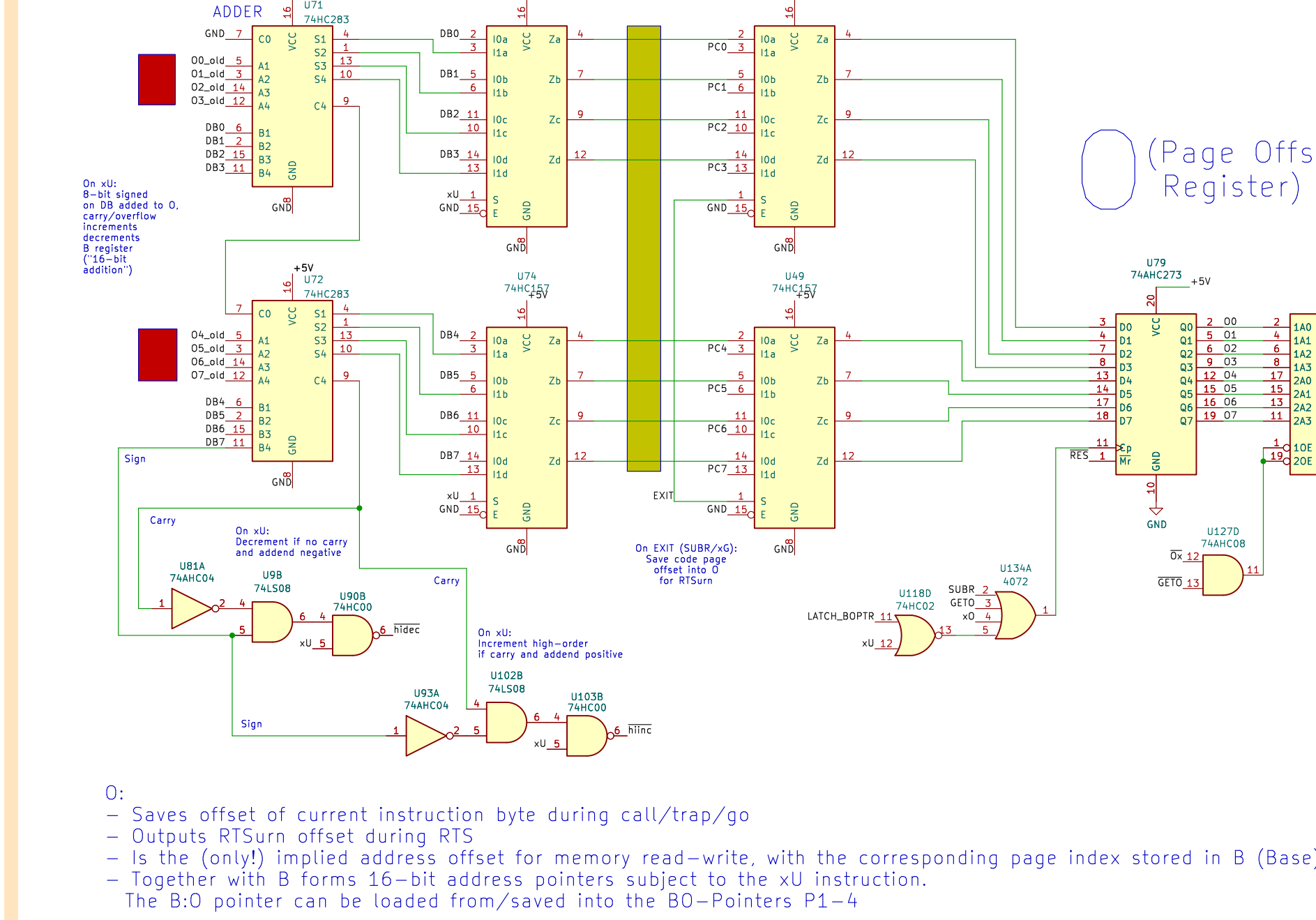
ALU Instructions

- | | |
|----------------------------------|-----------------------------|
| 0 IDA ("Identity A") | A ← A |
| 1 IDT ("Identity T") | A ← T |
| 2 OCA ("One's Complement") | A ← ~A |
| 3 OCT ("One's Complement T") | A ← ~T |
| 4 SLA ("Shift Left") | A ← A << 1 |
| 5 SRT ("Shift Right") | A ← A >> 1 |
| 6 SRA ("Shift Right Arithmetic") | A ← A >> 1 |
| 7 SRT ("Shift Right") | A ← A >> 1 |
| 8 AND ("A boolean-and T") | A ← A & T |
| 9 OR ("A inclusive-or T") | A ← A T |
| 10 XOR ("A exclusive-or T") | A ← A ^ T |
| 11 ADD ("Add 1 to A") | A ← A + 1 |
| 12 CAR ("Carry bit of A plus T") | A ← A + T, bits 0-7, 0 or 1 |
| 13 AL ("A less than T") | A ← (A < T) & 0xFF |
| 14 AE ("A equal to T") | A ← (A == T) & 0xFF |
| 15 AG ("A greater than T") | A ← (A > T) & 0xFF |

A (Accumulator)



Pointer low

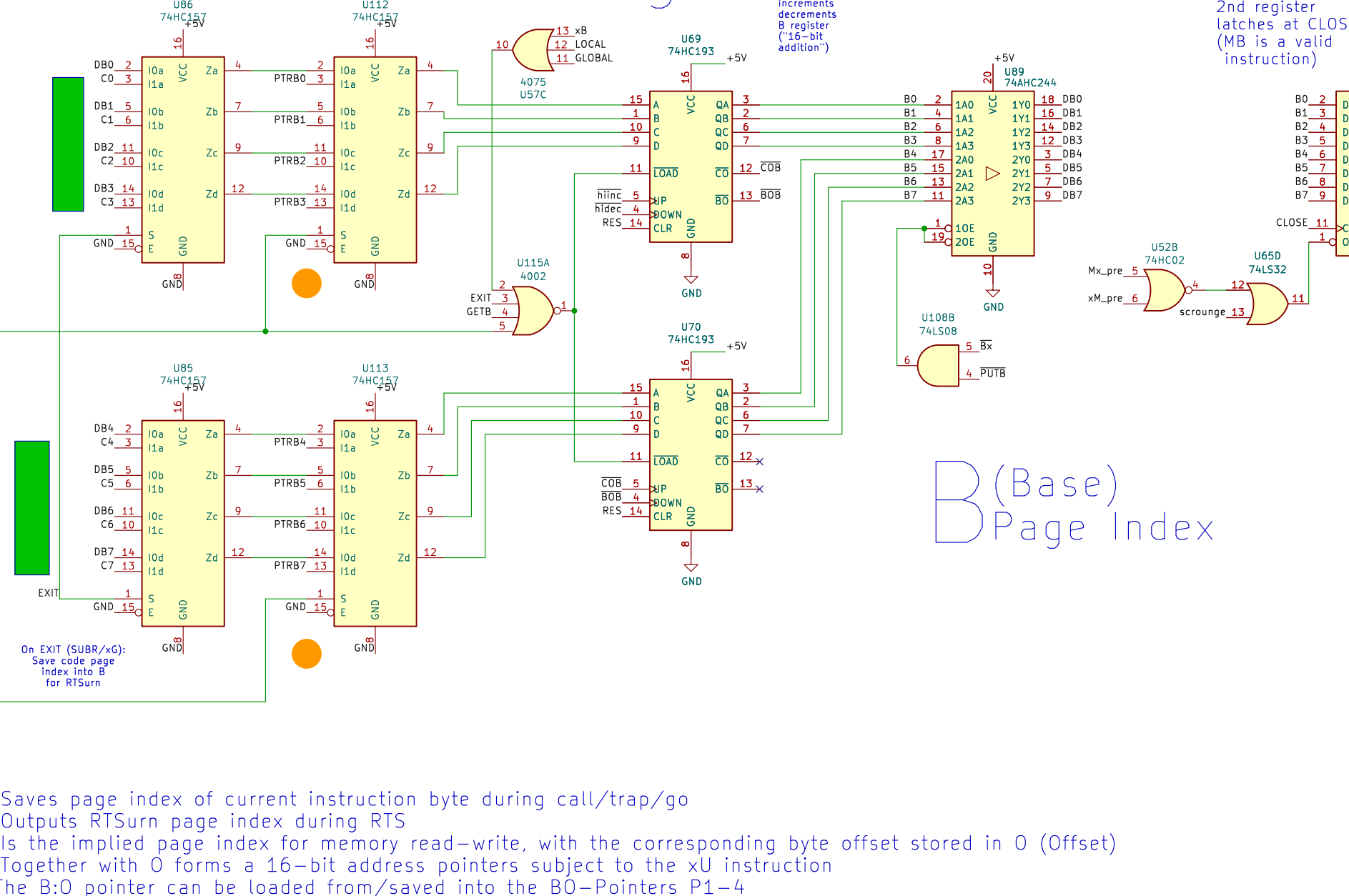


O (Page Offset Register)

Register at CLOS0 x0 instruction address would feedback

- Saves offset of current instruction byte during call/trap/go
- Outputs RtsUm offset during Rts
- Is the (only) implied address offset for memory read-write, with the corresponding page index stored in B (Base)
- Together with B forms 16-bit address pointers subject to the x0 instruction
- The B:O pointer can be loaded from/saved into the B0-Pointers P1-4

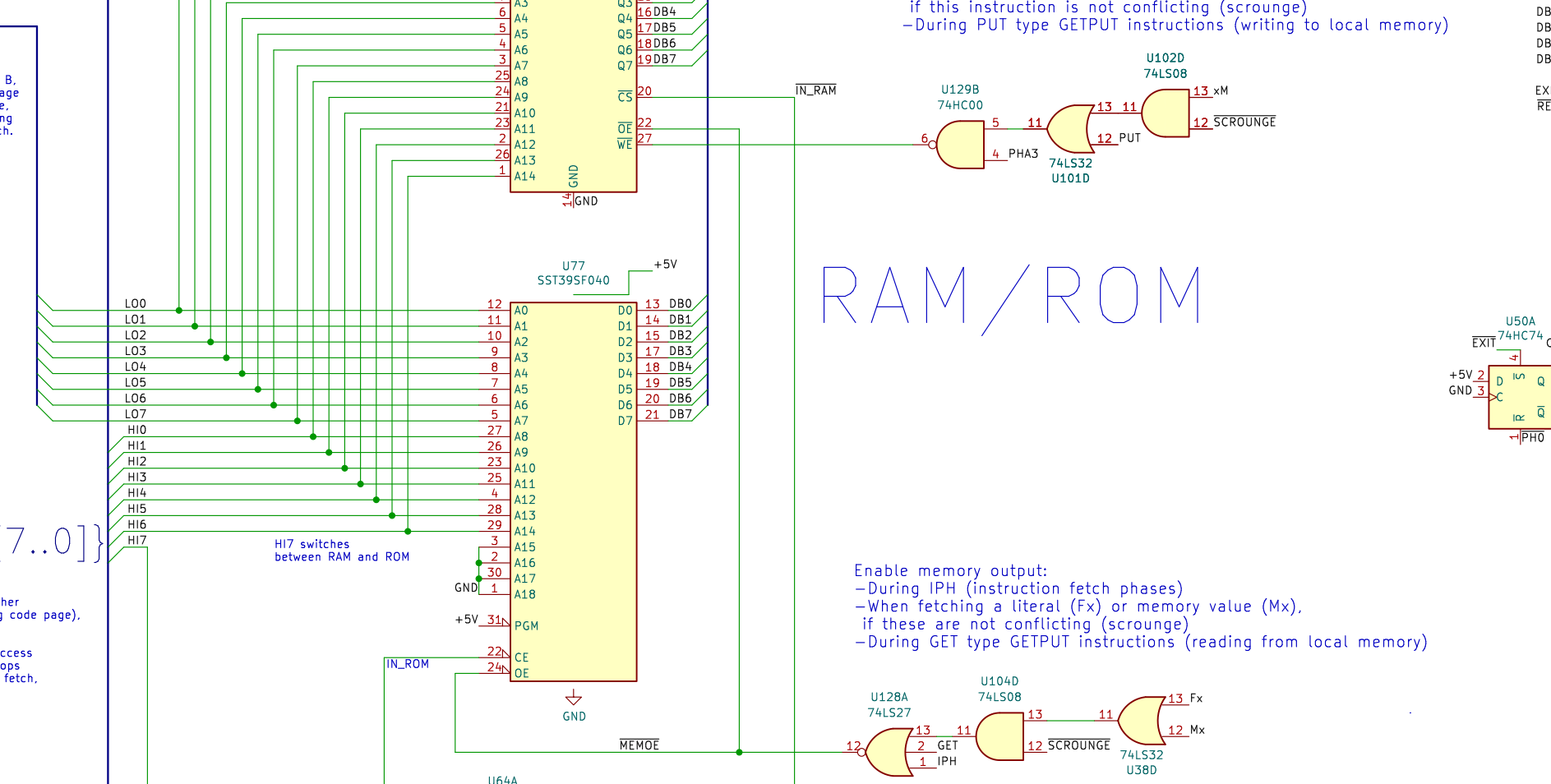
Pointer high



B (Base) Page Index

- Saves page index of current instruction byte during call/trap/go
- Outputs RtsUm page index during Rts
- Is the implied page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the x0 instruction
- The B:O pointer can be loaded from/saved into the B0-Pointers P1-4

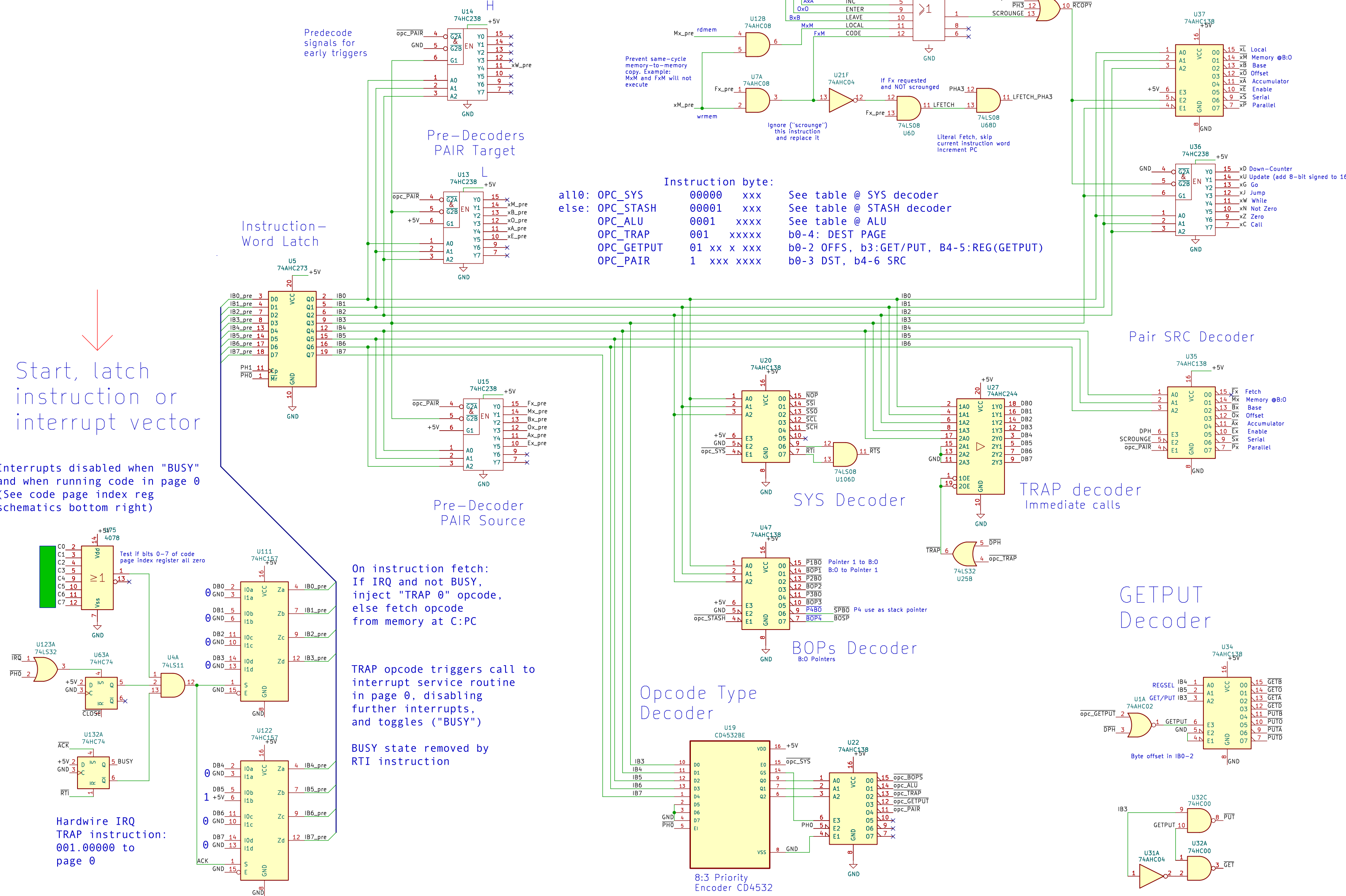
RAM/ROM



C (CODE) Page index



Instruction Decoder

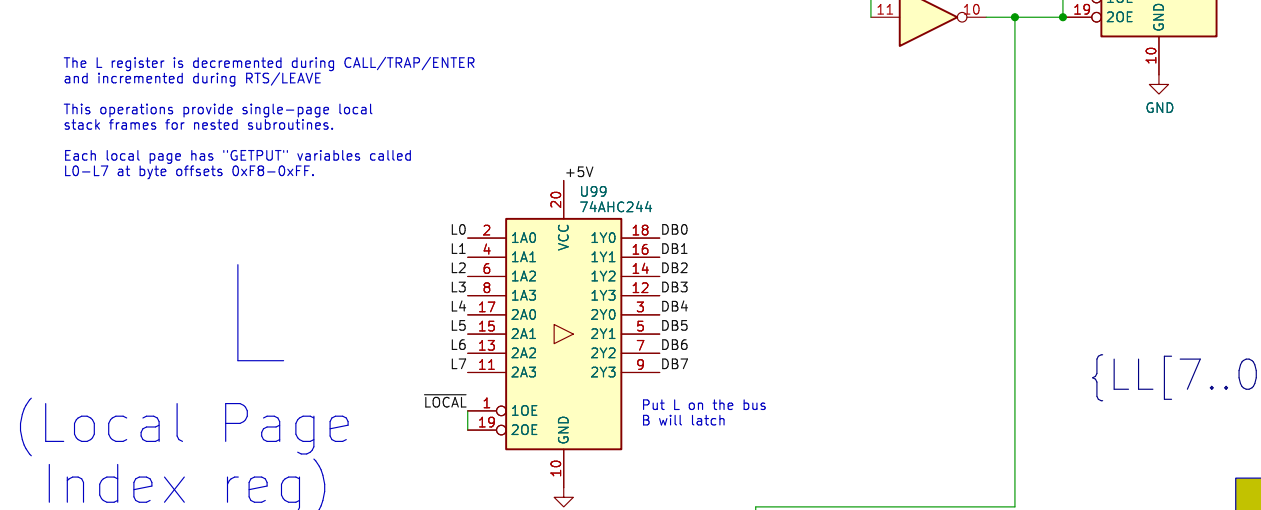
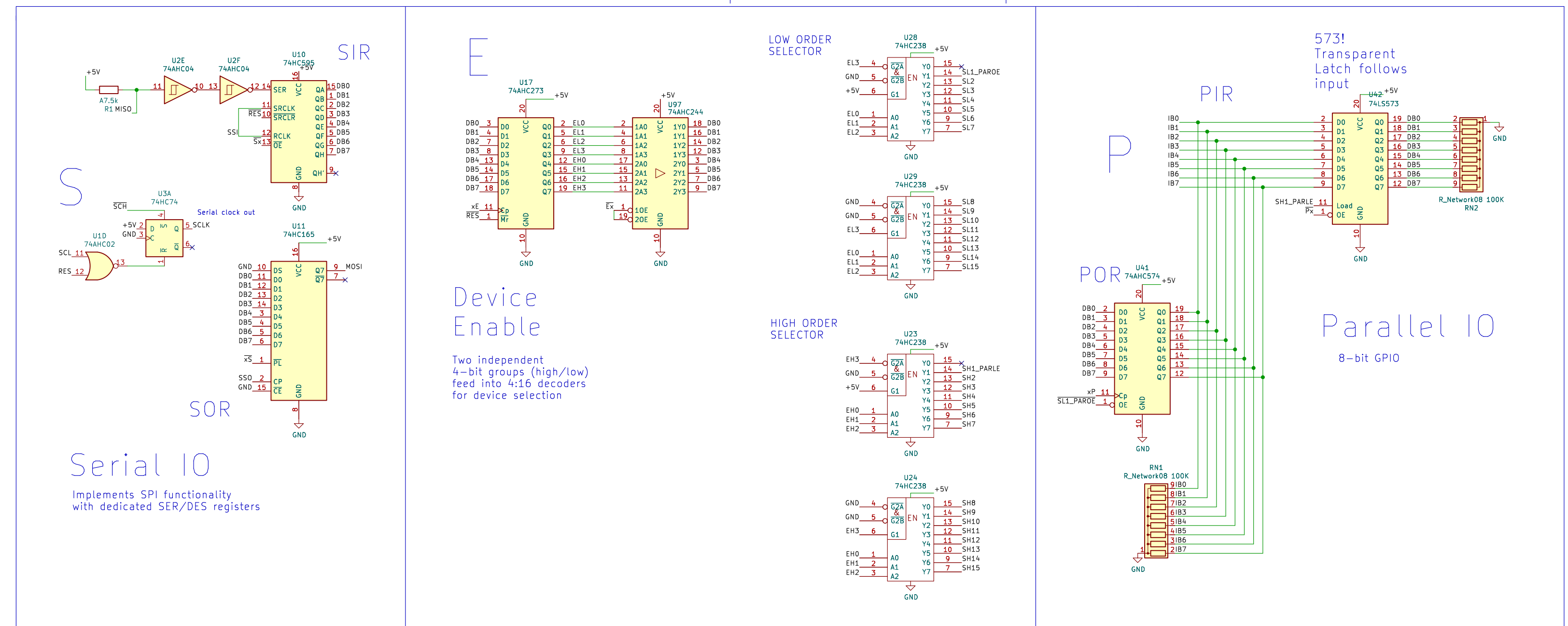


Start, latch instruction or interrupt vector

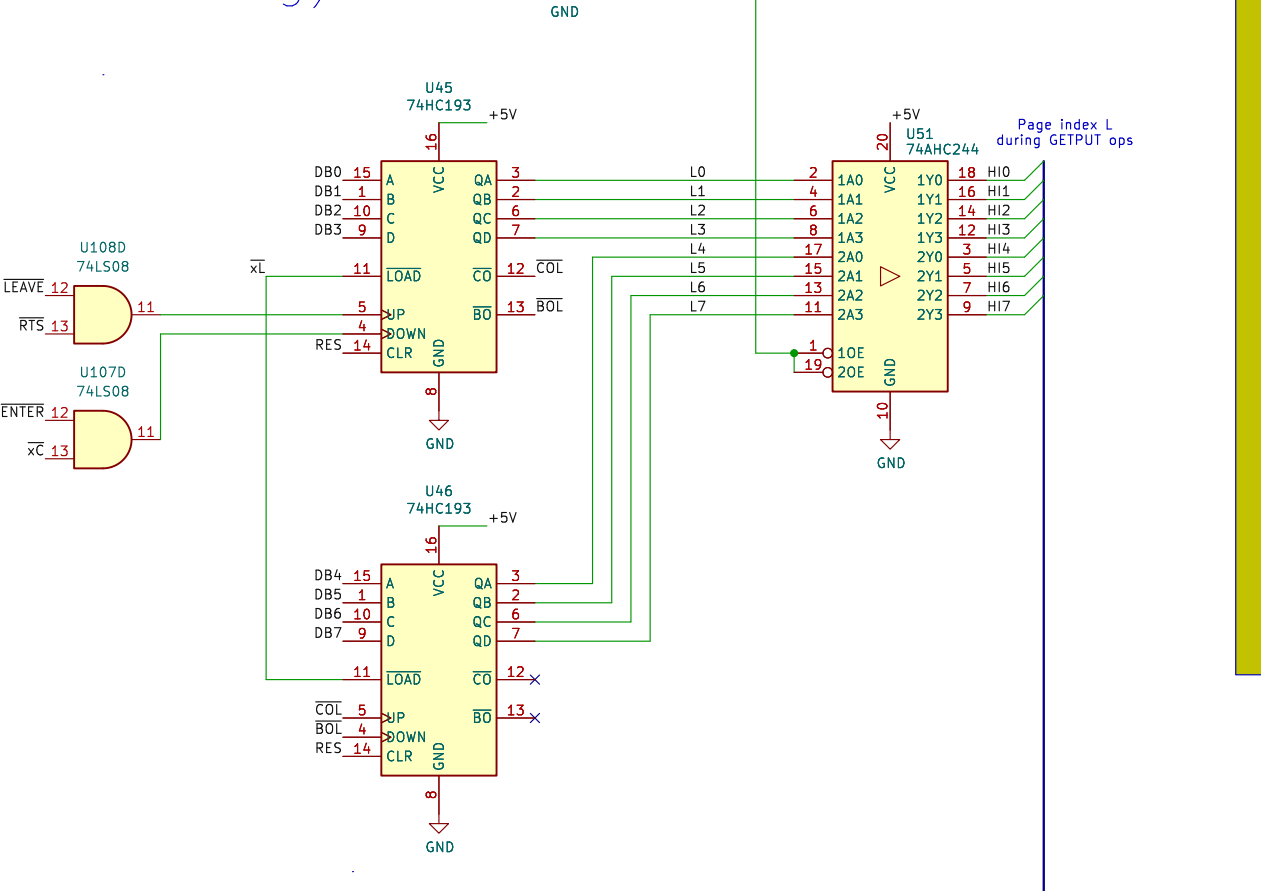
Interrupts disabled when "BUSY" and when running code in page 0 (See code page index reg schematics bottom right)

Hardware IRQ TRAP instruction: 001.00000 to page 0

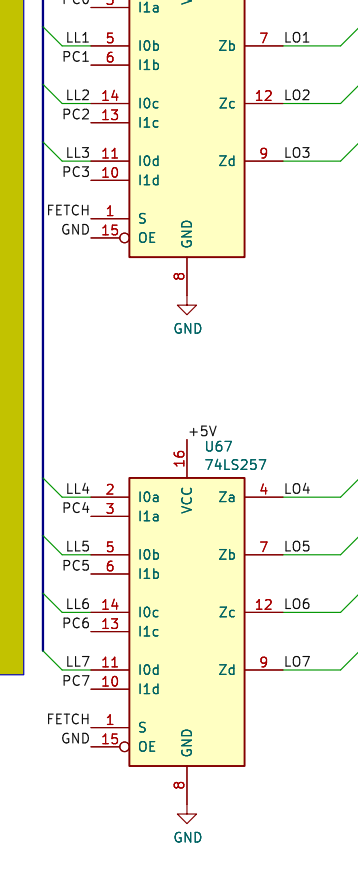
Input/Output



L (Local Page Index reg)



L7[7.0]



L0[7.0]



H[7.0]

