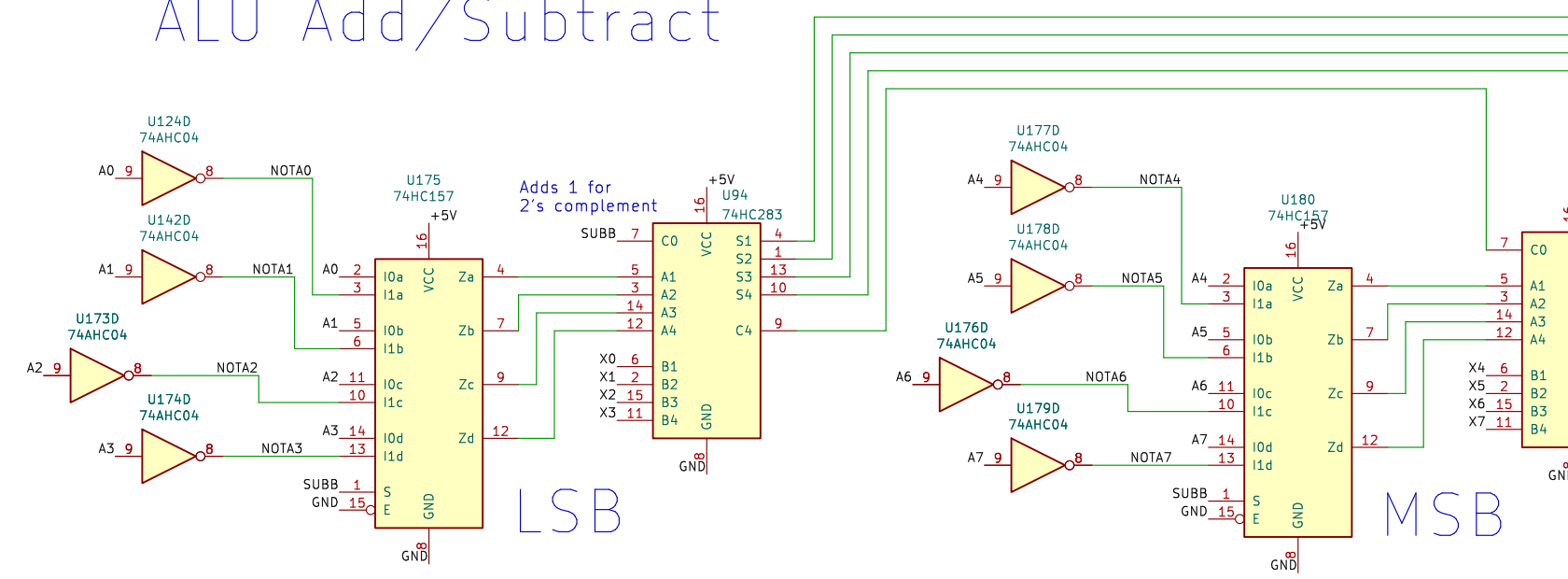
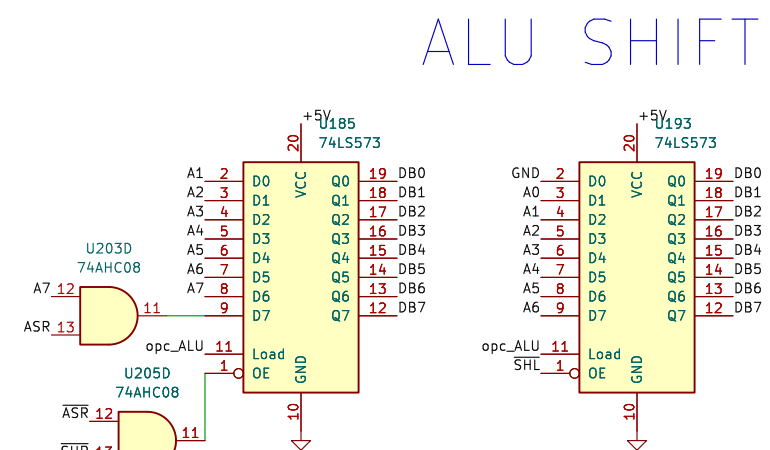


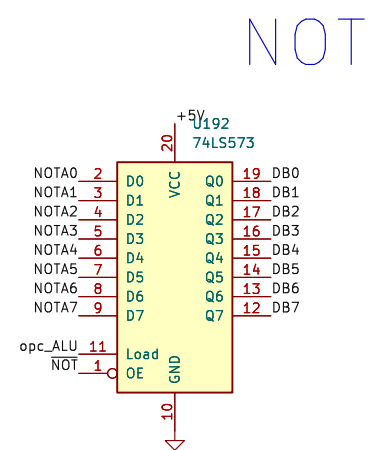
ALU Add/Subtract



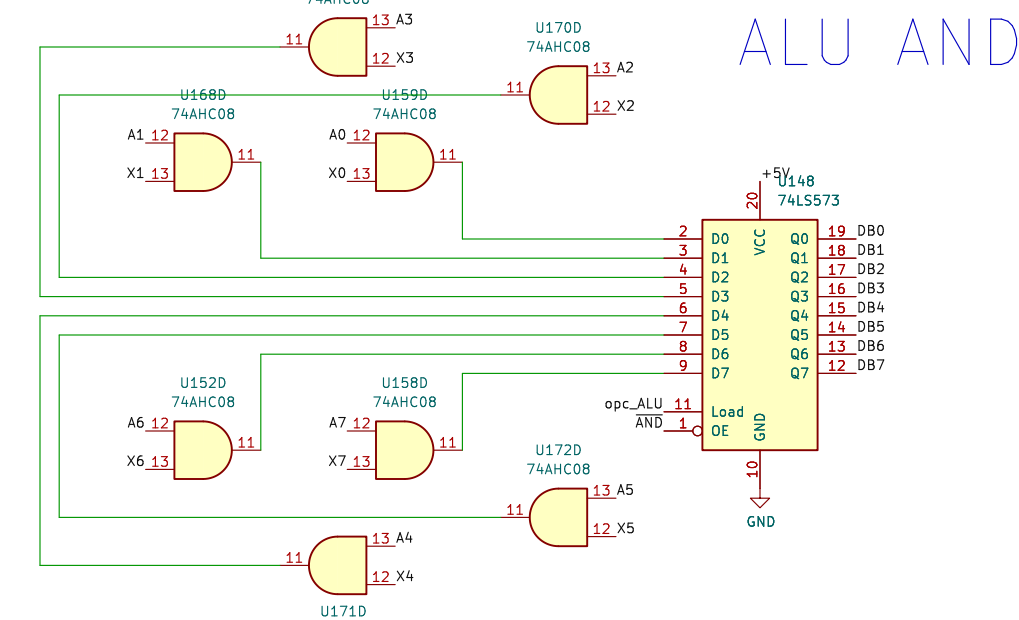
ALU SHIFT



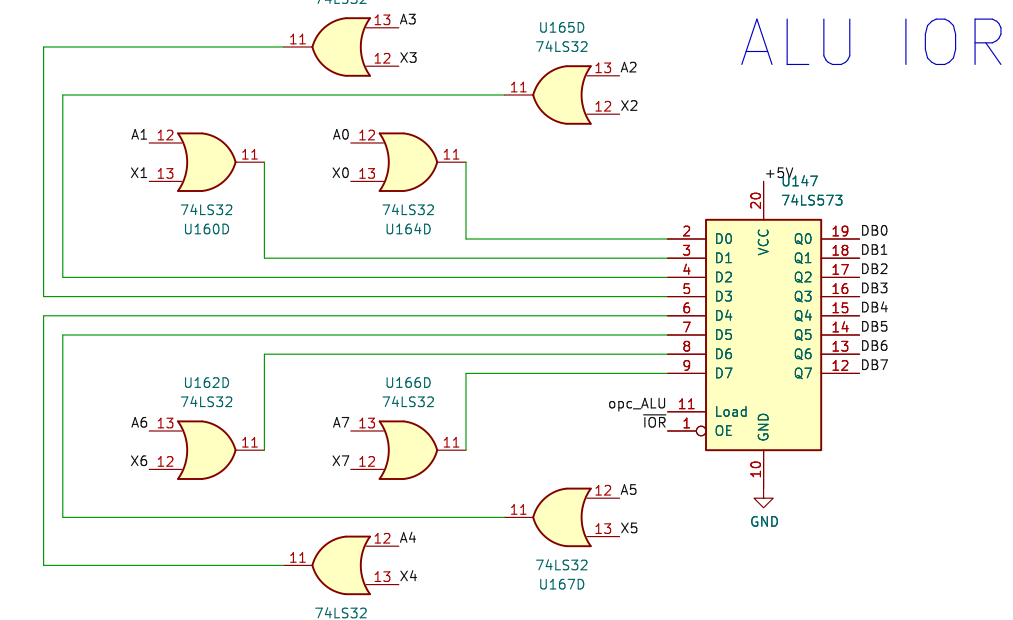
NOT



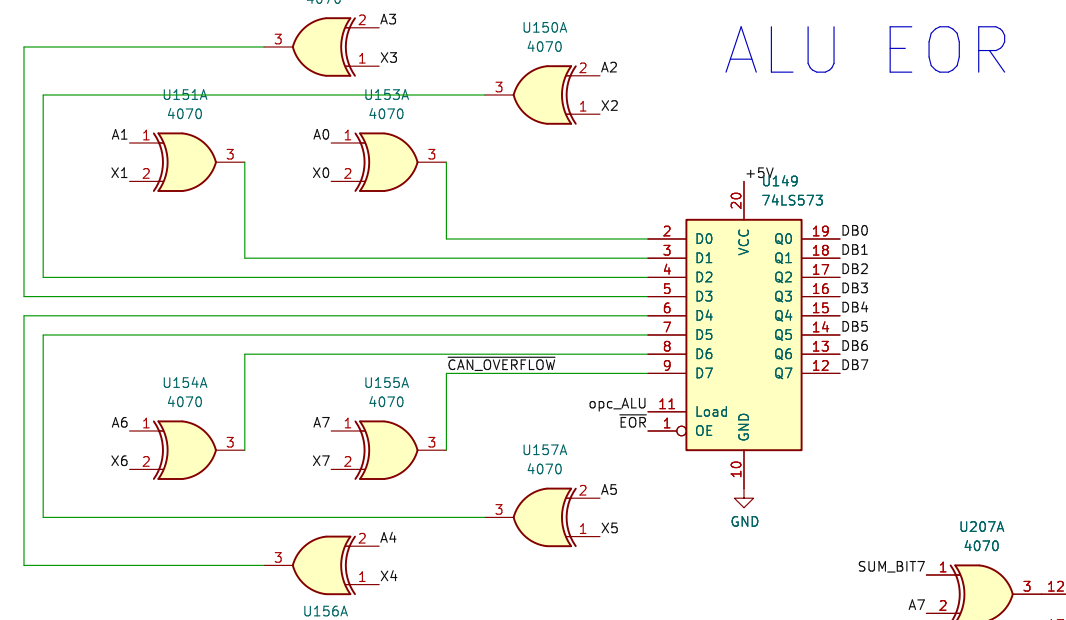
ALU AND



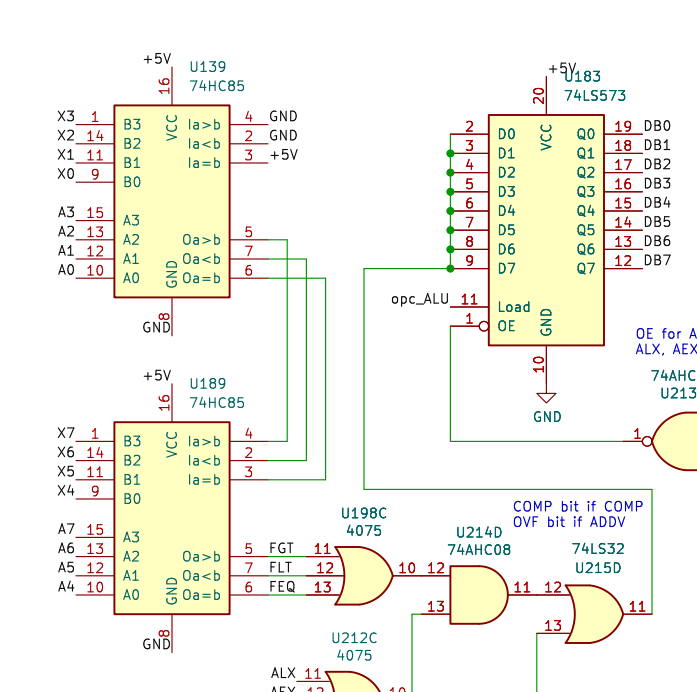
ALU IOR



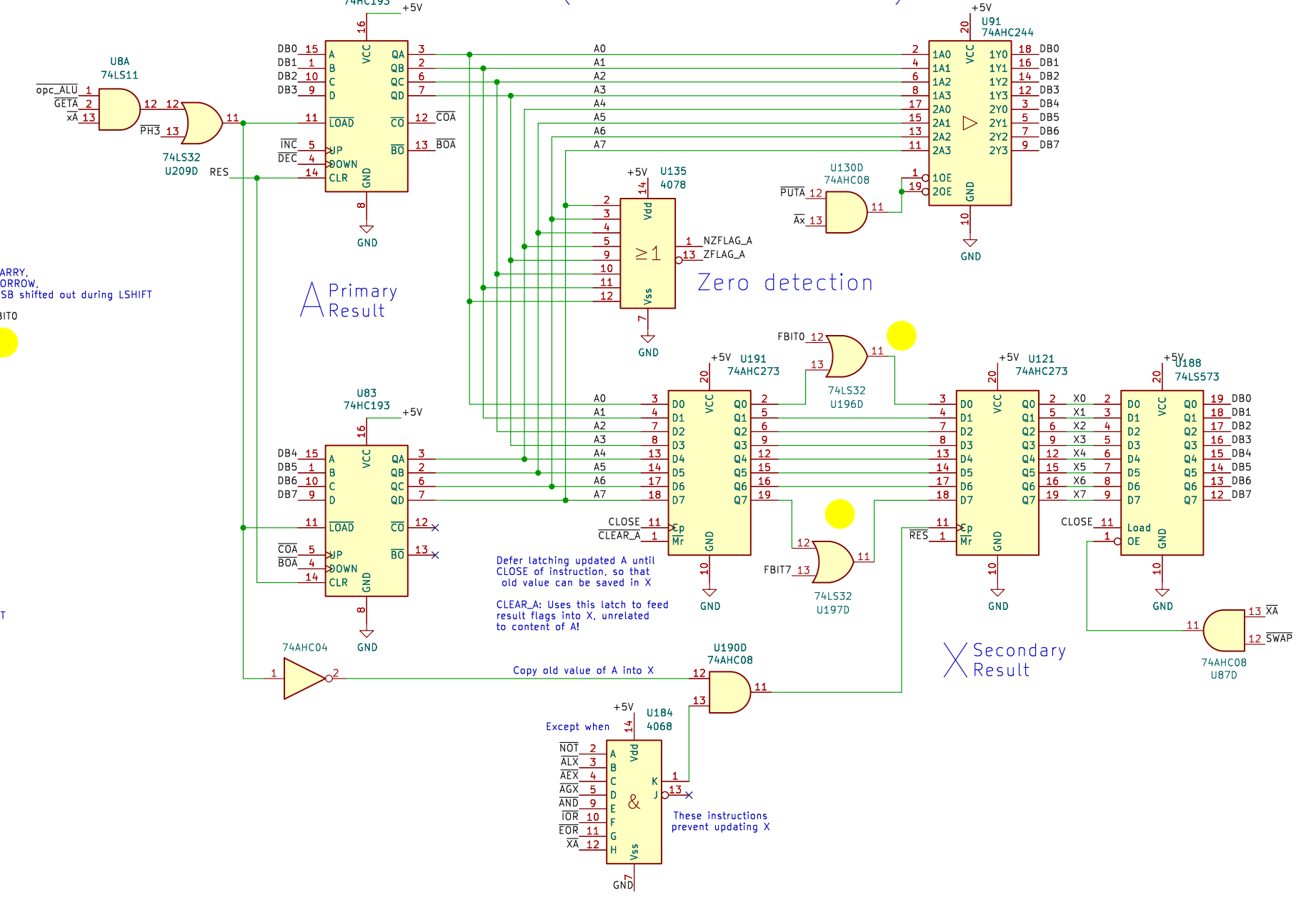
ALU EOR



ALU COMPARATOR



AX (Accumulator)



Sonne-8 Microcontroller

Reference Schematics

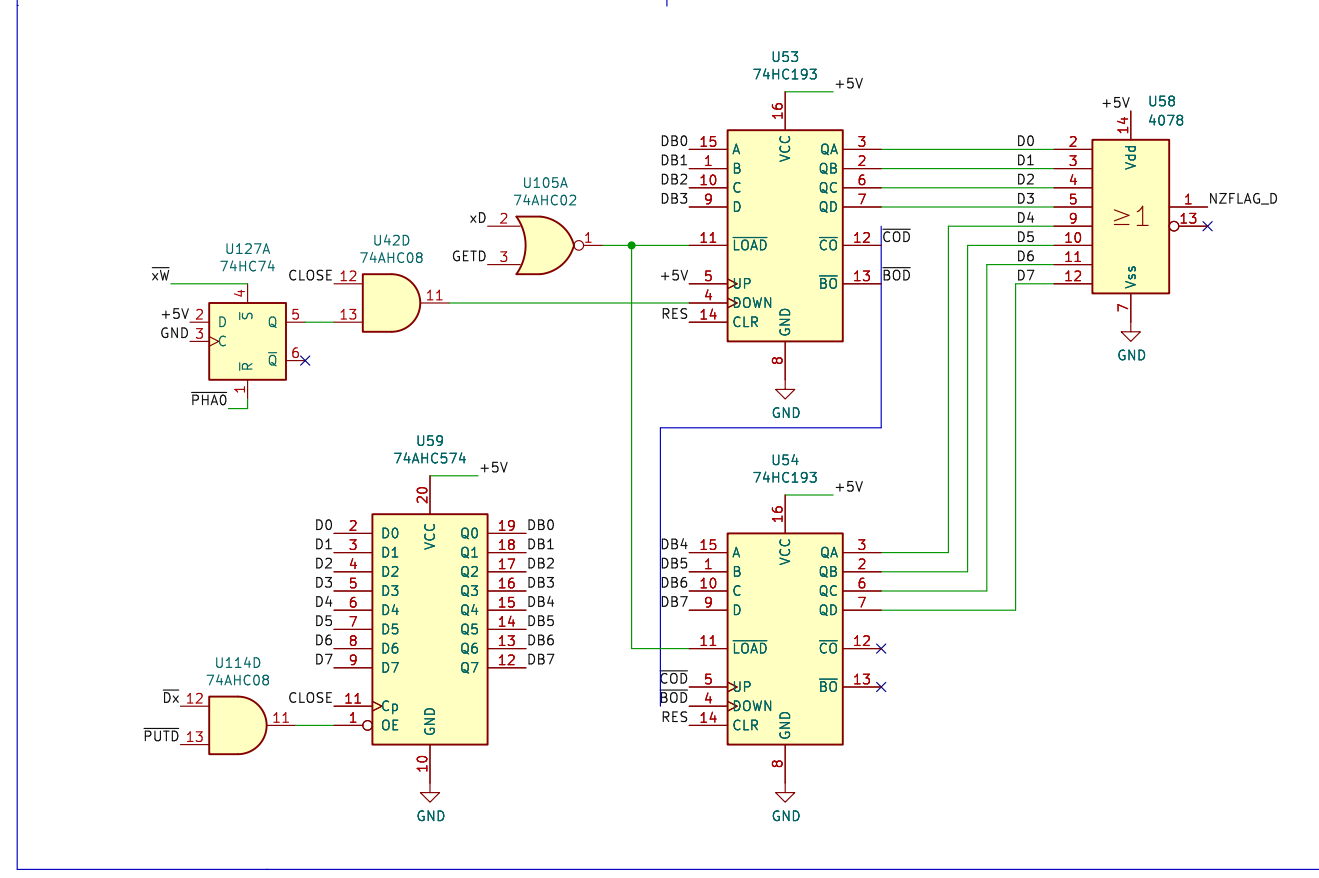
Rev. Myth

ALU Instructions

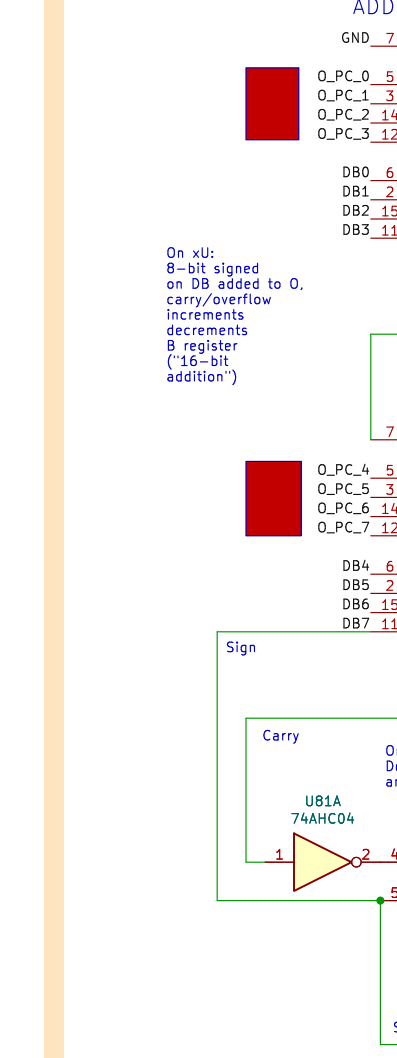
- 0 ADD Set A to sum of complement of A, B unchanged
- 1 ADD Flag (add) to A (0001 if true, 0 if false), X unchanged
- 2 ADD Flag (add) to A (0001 if true, 0 if false), X unchanged
- 3 ADD Set A to sum of A, B unchanged
- 4 ADD Set A to sum of A, X unchanged
- 5 ADD Set A to sum of A, Y unchanged
- 6 ADD Set A equal to X, X unchanged
- 7 ADD Set A equal to Y, Y unchanged
- 8 SWAP Swap A and B
- 9 SWAP Swap A and X
- 10 SWAP Swap A and Y
- 11 SWAP Swap A and B, result in A, set X to previous MSB of A as SWAP (0 or 1)
- 12 SWAP Swap A and X, result in A, set X to previous MSB of A as SWAP (0 or 1)
- 13 SWAP Swap A and Y, result in A, set Y to previous MSB of A as SWAP (0 or 1)
- 14 SWAP Swap A to X, result in A, set X to previous MSB of A as SWAP (0 or 1)
- 15 SWAP Swap A to Y, result in A, set Y to previous MSB of A as SWAP (0 or 1)

D(OWN) COUNTER

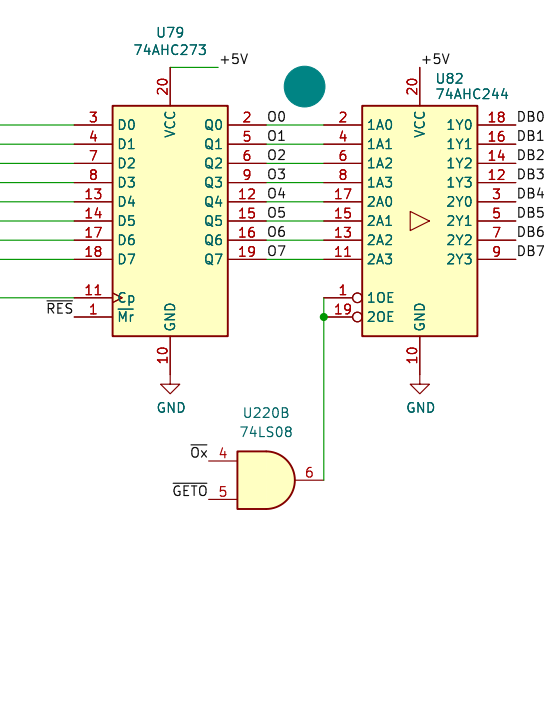
Inner-loops



Pointer low



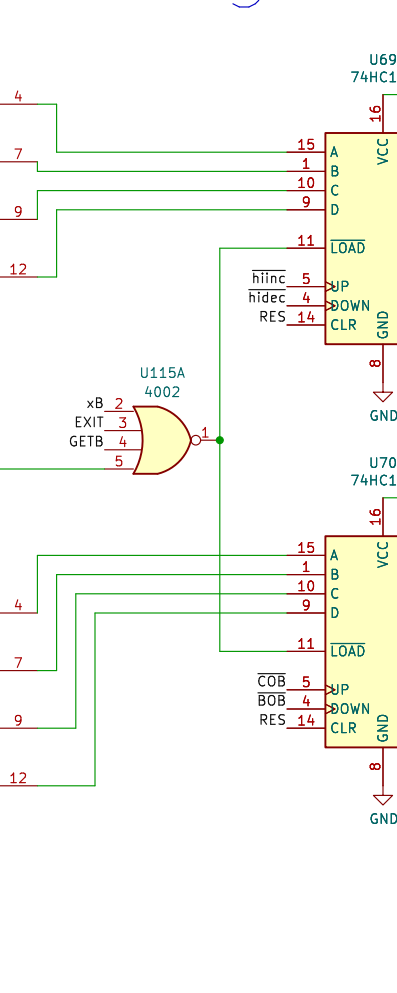
O (Page Offset Register)



BO Pointer Registers

- Saves offset of current instruction byte during call/trap/cor
- Outputs return offset during RET
- Is the (only) implied address offset for memory read-write, with the corresponding page index stored in B (Base)
- Together with B forms 16-bit address pointers subject to the xU instruction
- The B:O pointer can be loaded from/saved into the pointer registers

Pointer high



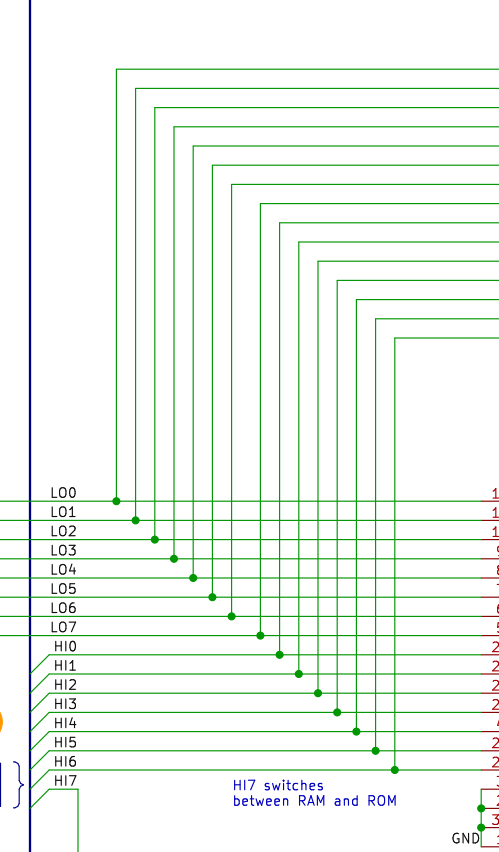
B (Base) Page Index

- Saves page index of current instruction byte during call/trap/cor
- Outputs return page index during RET
- Is the (only) implied page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
- The B:O pointer can be loaded from/saved into the pointer registers

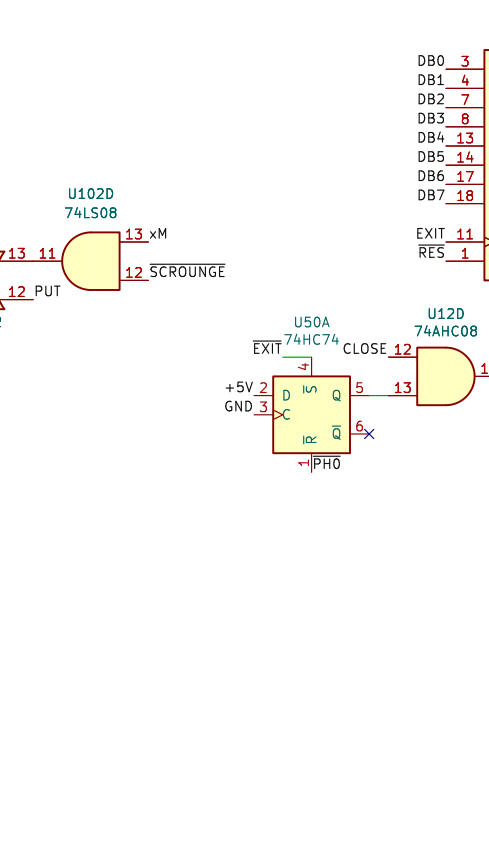
Guest-Page Index

- Saves guest page index of current instruction byte during call/trap/cor
- Outputs return guest page index during RET
- Is the (only) implied guest page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
- The B:O pointer can be loaded from/saved into the pointer registers

RAM/ROM



C (Code) Page Index

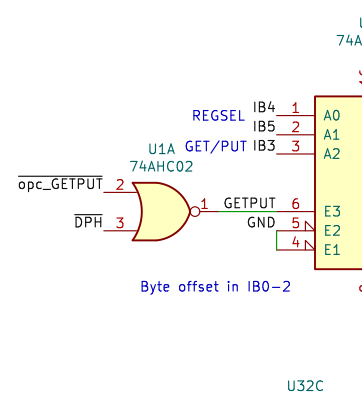


Guest-Page Index

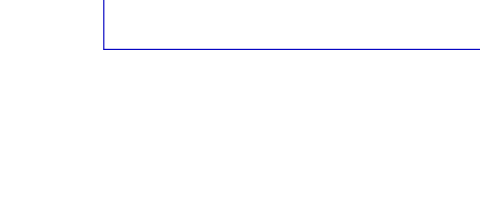
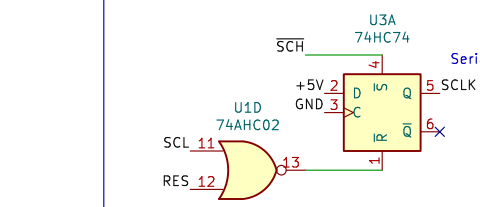
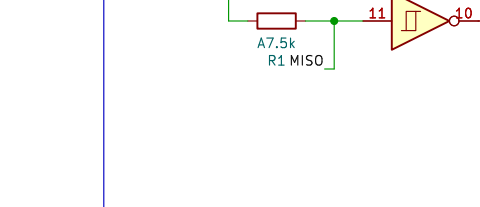
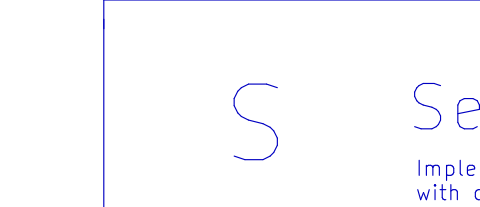
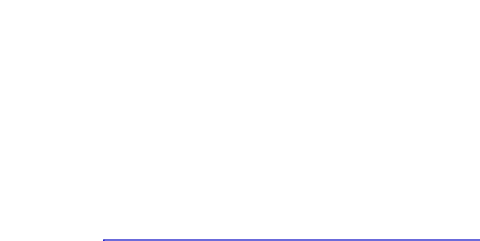
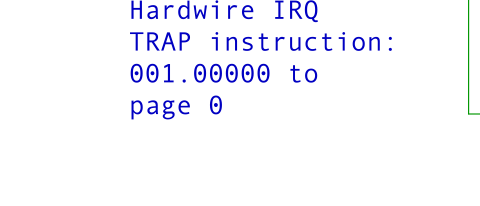
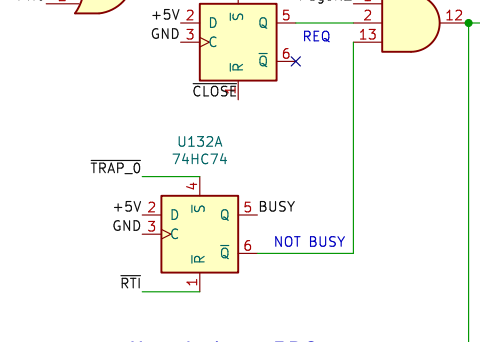
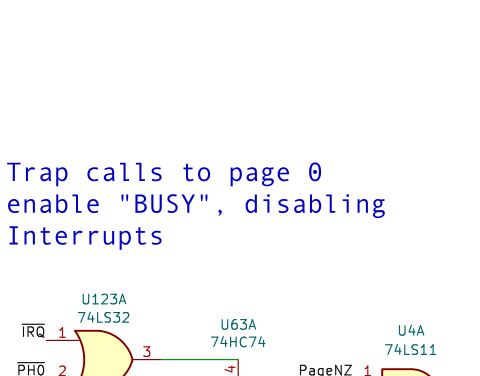
- Saves guest page index of current instruction byte during call/trap/cor
- Outputs return guest page index during RET
- Is the (only) implied guest page index for memory read-write, with the corresponding byte offset stored in O (Offset)
- Together with O forms a 16-bit address pointers subject to the xU instruction
- The B:O pointer can be loaded from/saved into the pointer registers

Instruction Decoder

GETPUT Decoder



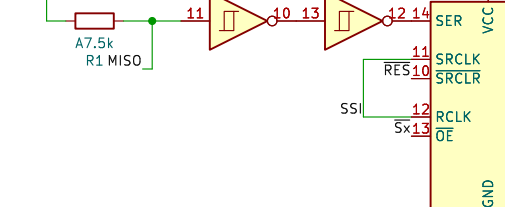
Start, latch instruction or interrupt vector



Input/Output

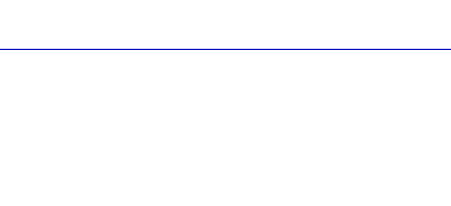
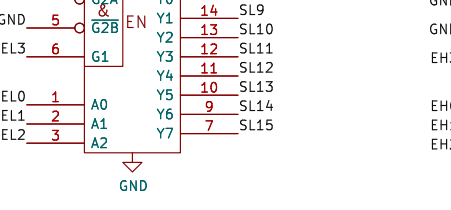
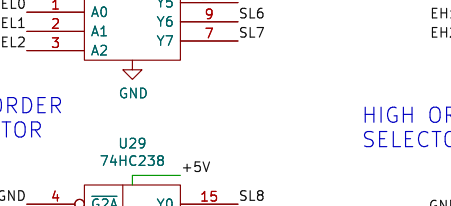
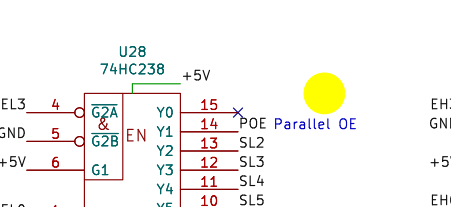
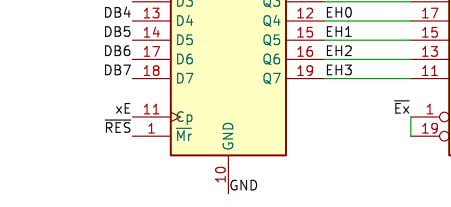
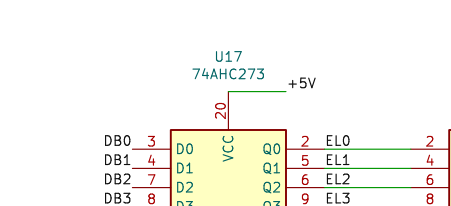
S Serial IO

Implements SPI functionality with dedicated SER/DES registers



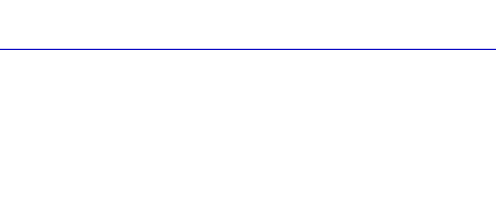
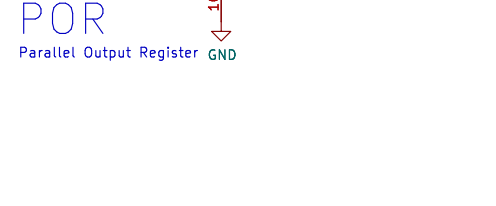
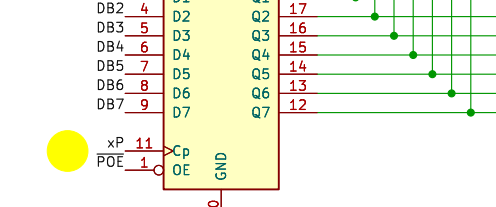
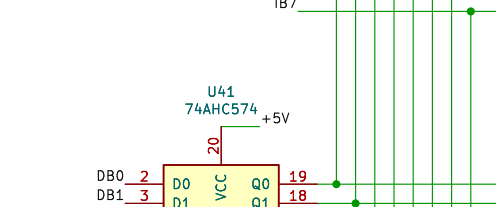
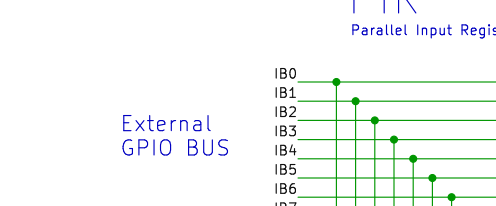
E Device Enable Register

Two independent 4-bit groups (high/low) feed into x:SE decoders for device selection



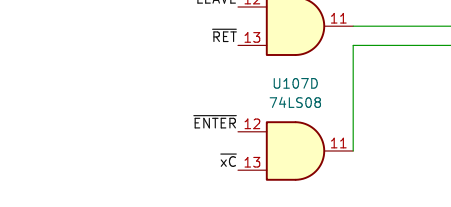
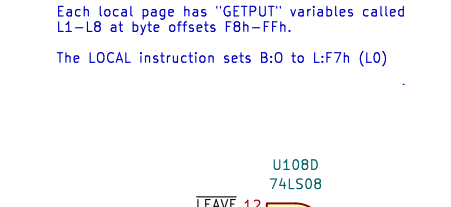
P Parallel IO

External GPB BUS

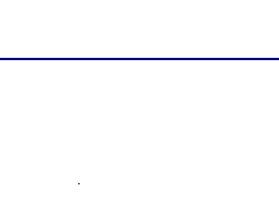
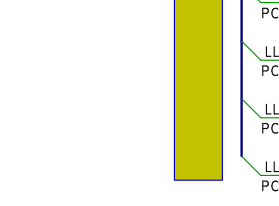
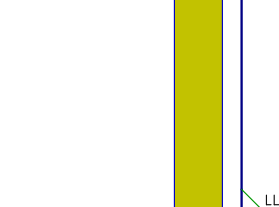
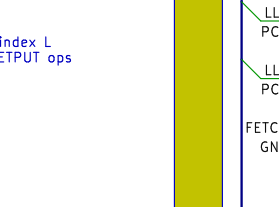
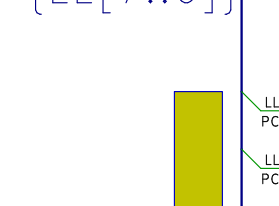


(Local Page Index Register)

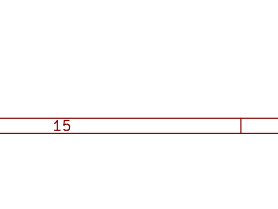
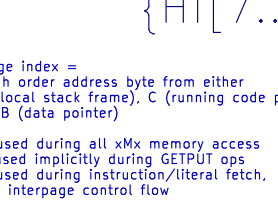
The L register is decremented during CALL/Trap/ENTER and incremented during RET/EXIT



{LL[7..0]}



{Lo[7..0]}



{Hi[7..0]}

