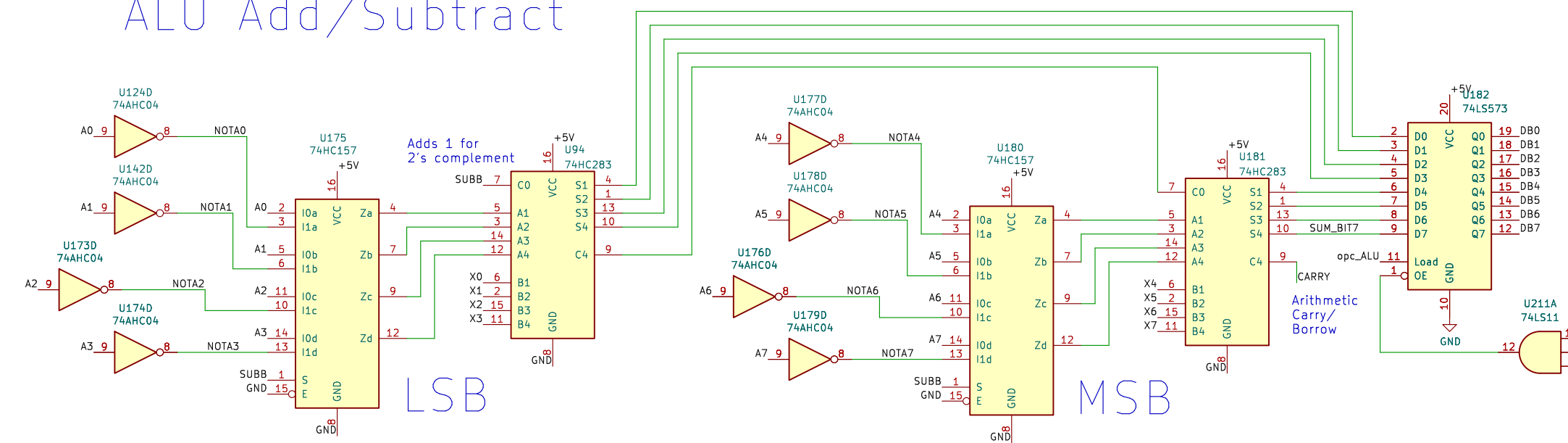
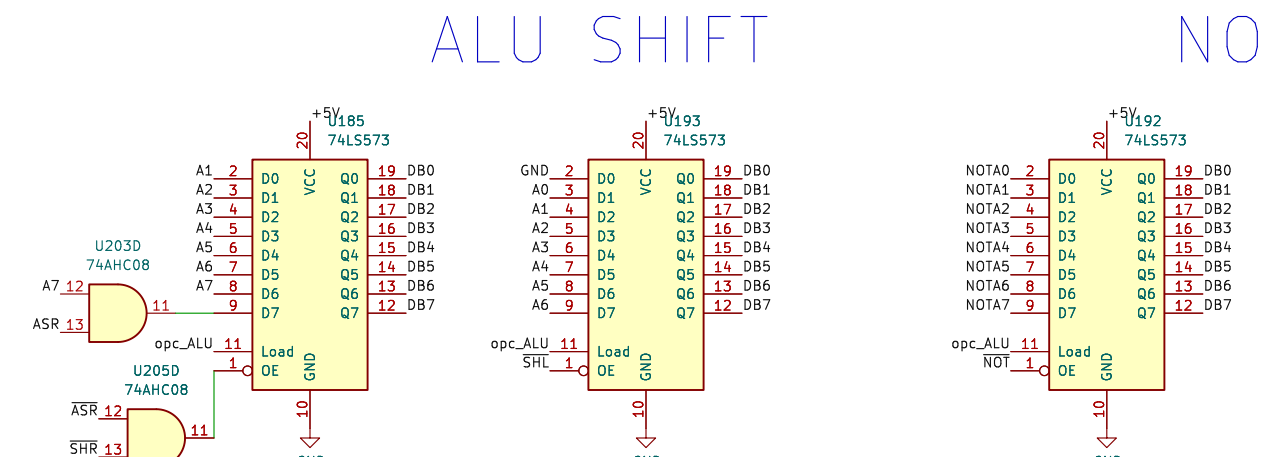


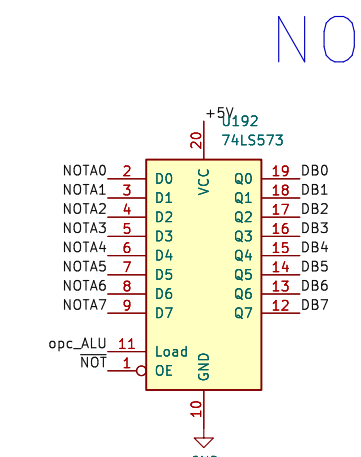
ALU Add/Subtract



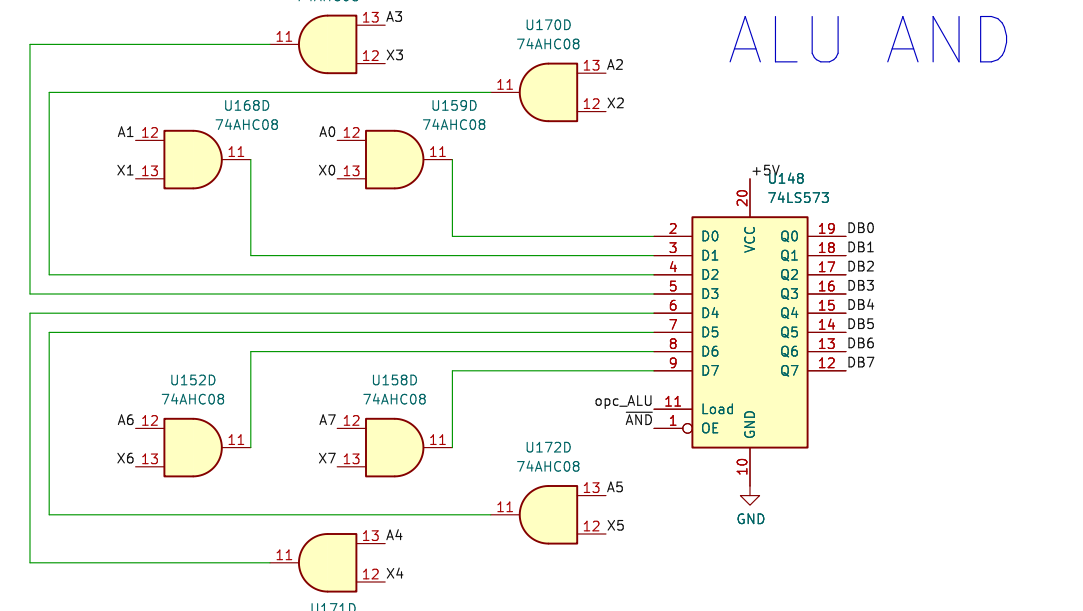
ALU SHIFT



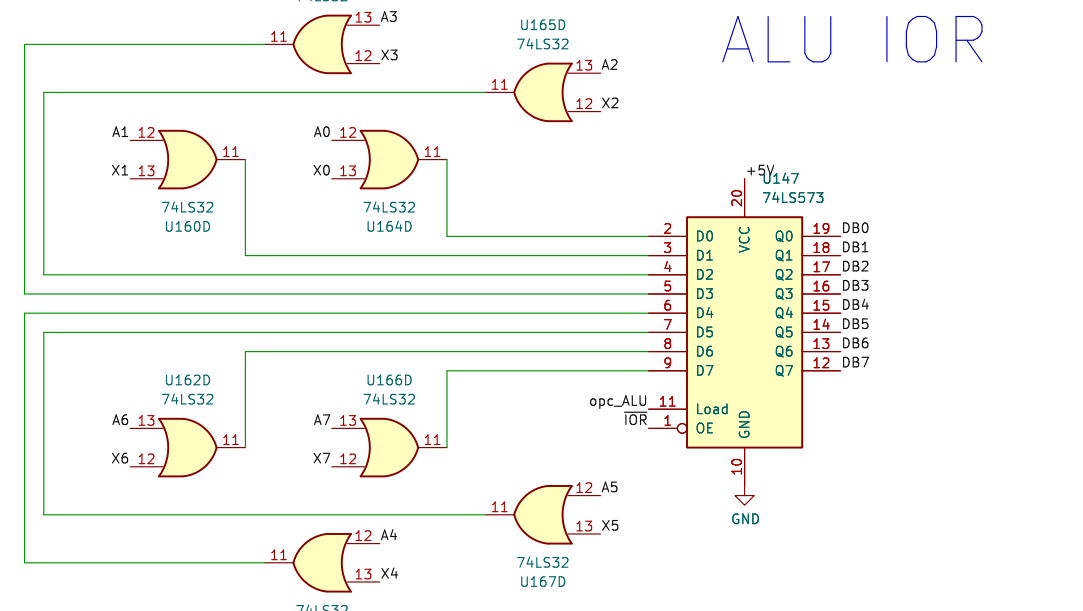
NOT



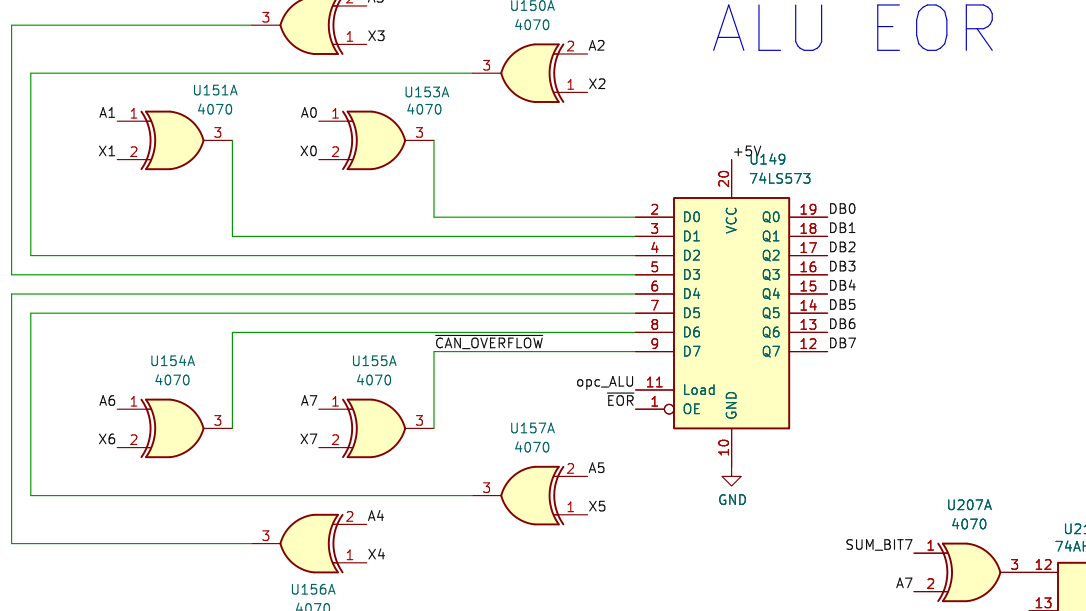
ALU AND



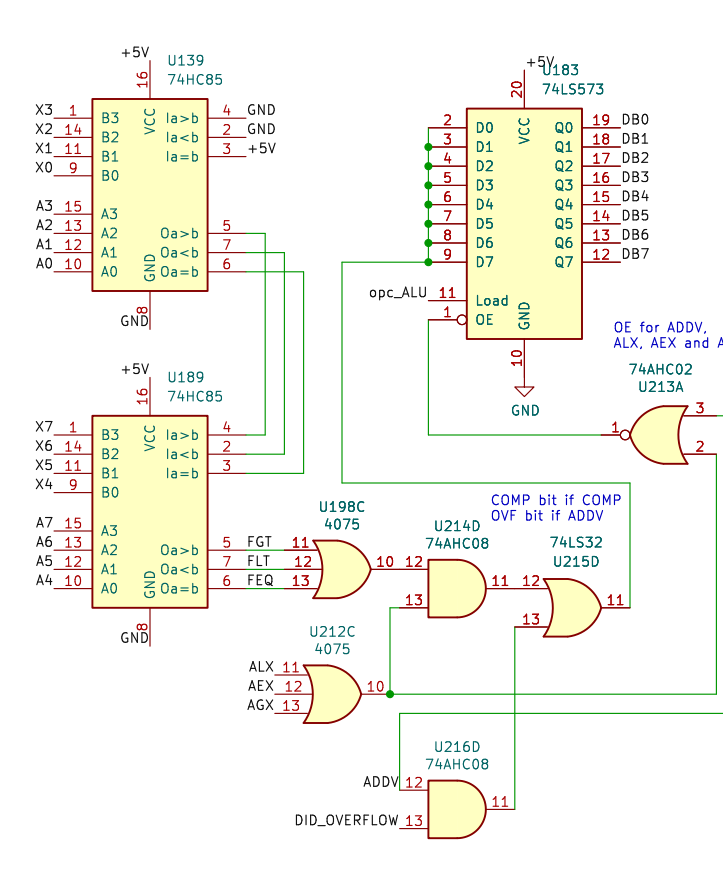
ALU IOR



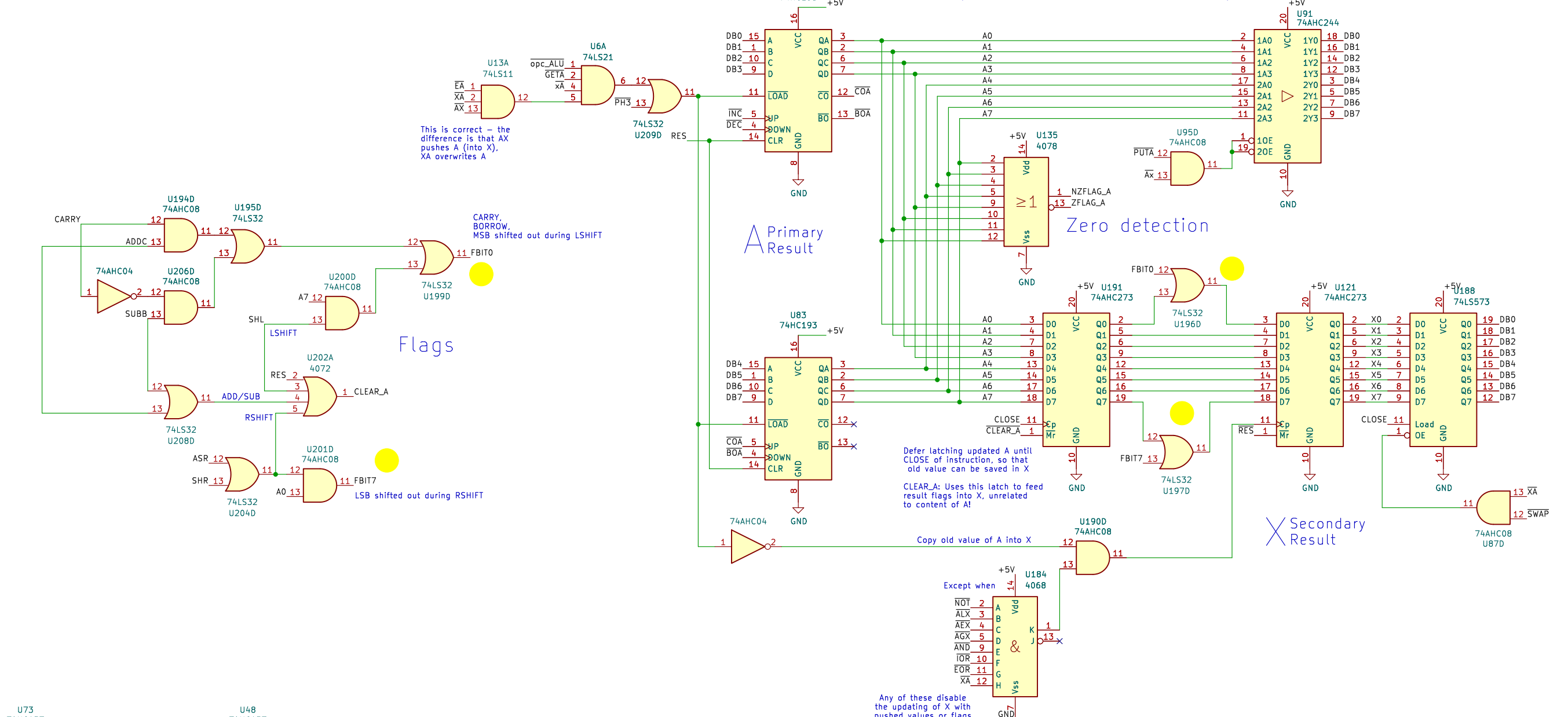
ALU EOR



ALU COMPARATOR



AX (Accumulator)

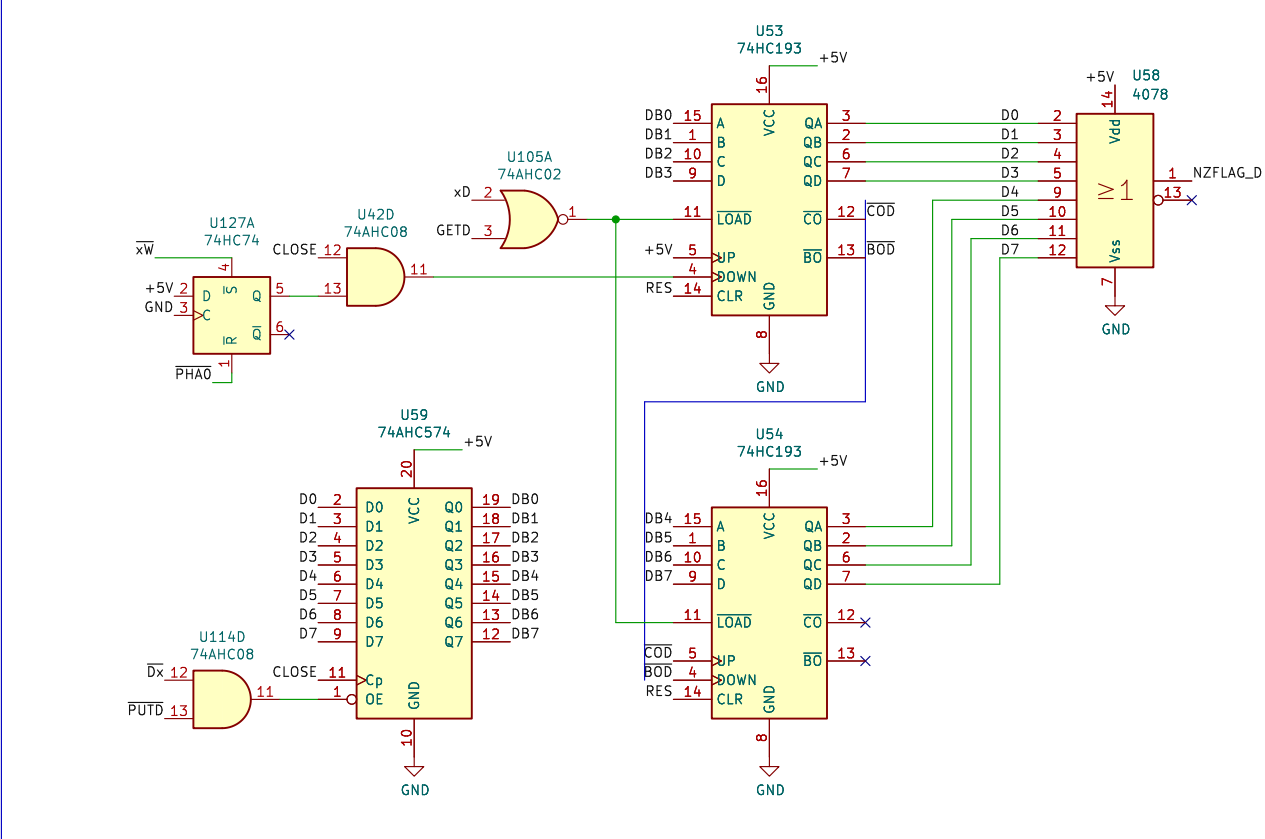


Myth Microcontroller Reference Schematic

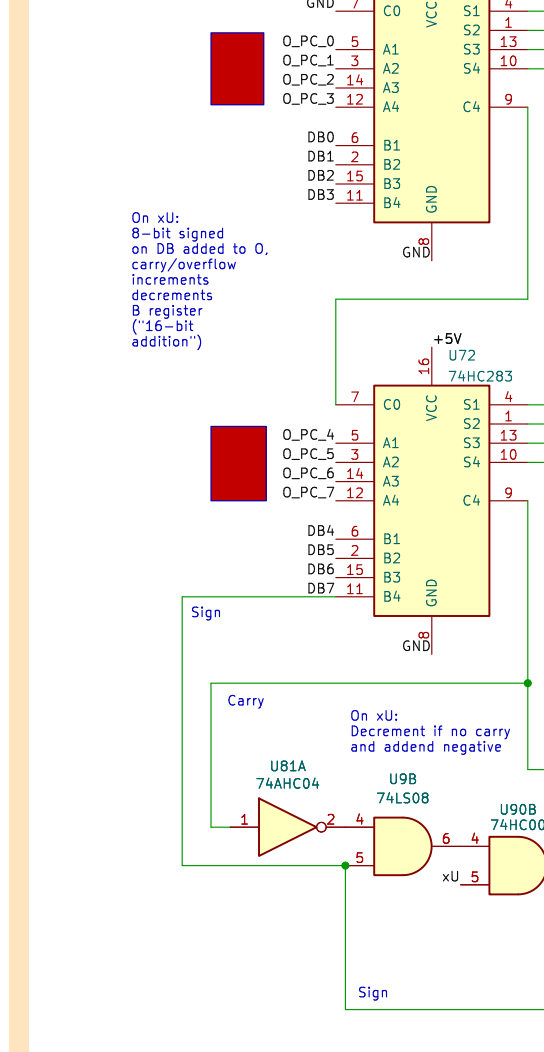
ALU Instructions

0 NOT Set A to not's complement of A, X unchanged
1 ADD Play above in A, L255 if true, 1 if false, X unchanged
2 SUB Play above in A, L255 if true, 1 if false, X unchanged
3 AND Play above in A, L255 if true, 1 if false, X unchanged
4 OR Play above in A, L255 if true, 1 if false, X unchanged
5 XOR Play above in A, L255 if true, 1 if false, X unchanged
6 SHL Shift A left arithmetically, set A to previous MSB of A as MSB (0 or 255)
7 SHR Shift A right arithmetically, set A to previous MSB of A as MSB (0 or 255)
8 ROL Shift A left circularly, set A to previous MSB of A as MSB (0 or 255)
9 ROR Shift A right circularly, set A to previous MSB of A as MSB (0 or 255)
10 DADD Add A to A, result in A, OVERFLOW flag to X (255 if overflow, else 0)
11 DDOR Add A to A, result in A, OVERFLOW flag to X (255 if overflow, else 0)
12 DDOR Add A to A, result in A, OVERFLOW flag to X (255 if overflow, else 0)
13 DDOR Add A to A, result in A, OVERFLOW flag to X (255 if overflow, else 0)
14 DDOR Add A to A, result in A, OVERFLOW flag to X (255 if overflow, else 0)
15 DDOR Subtract A from A, result in A, OVERFLOW flag to X (0 or 1)

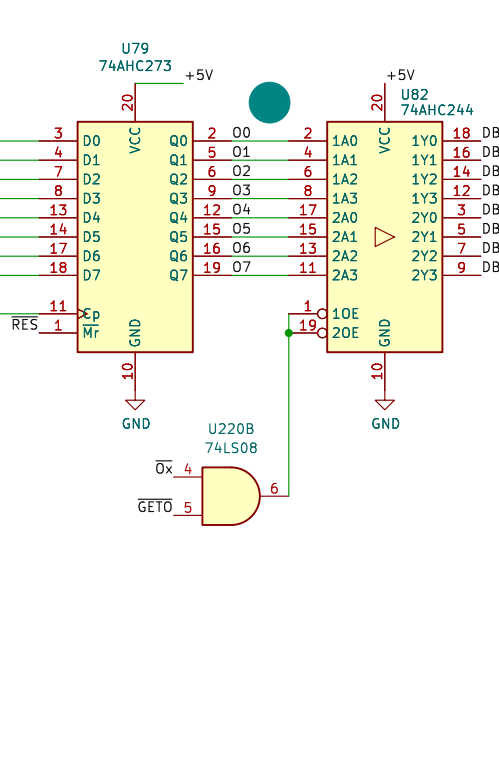
D(OWN) COUNTER Inner-loops



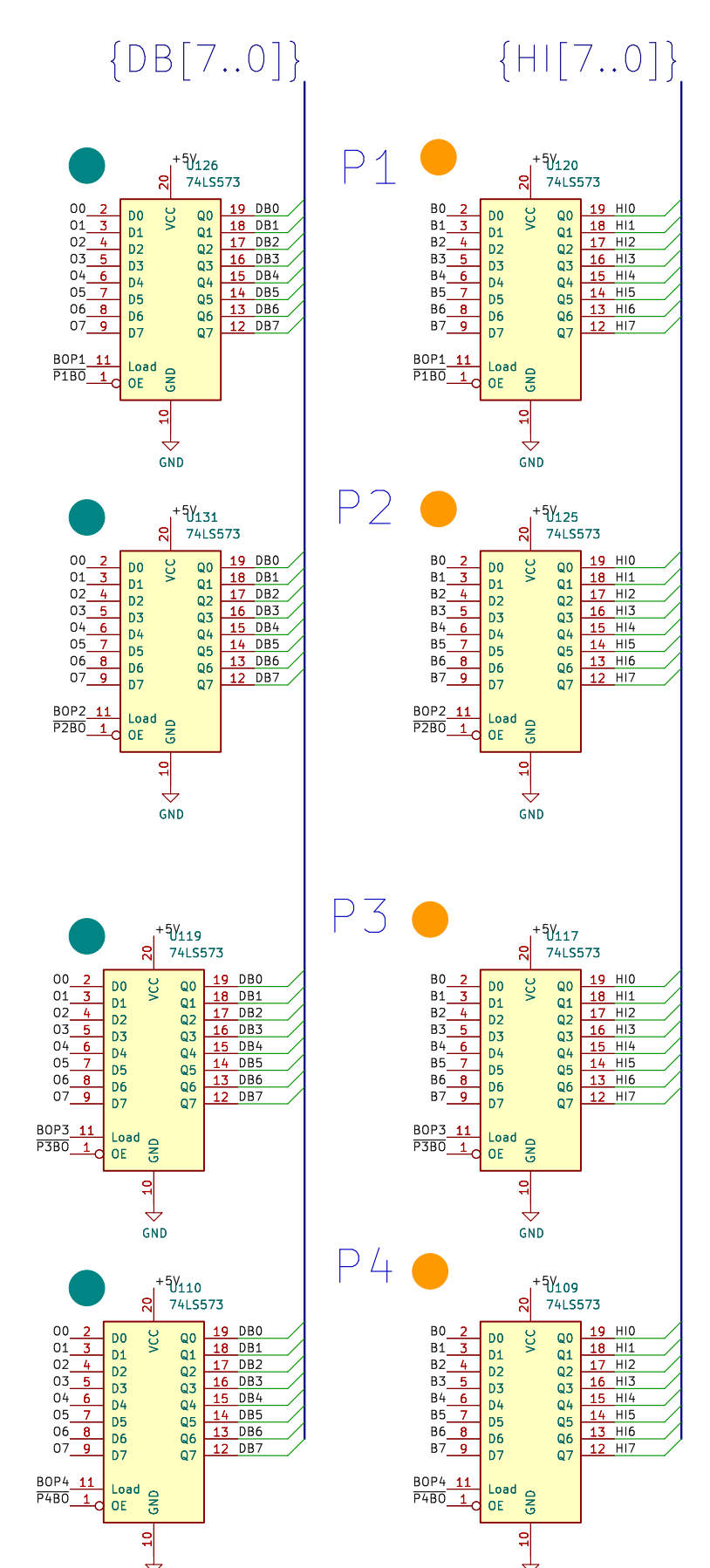
Pointer low



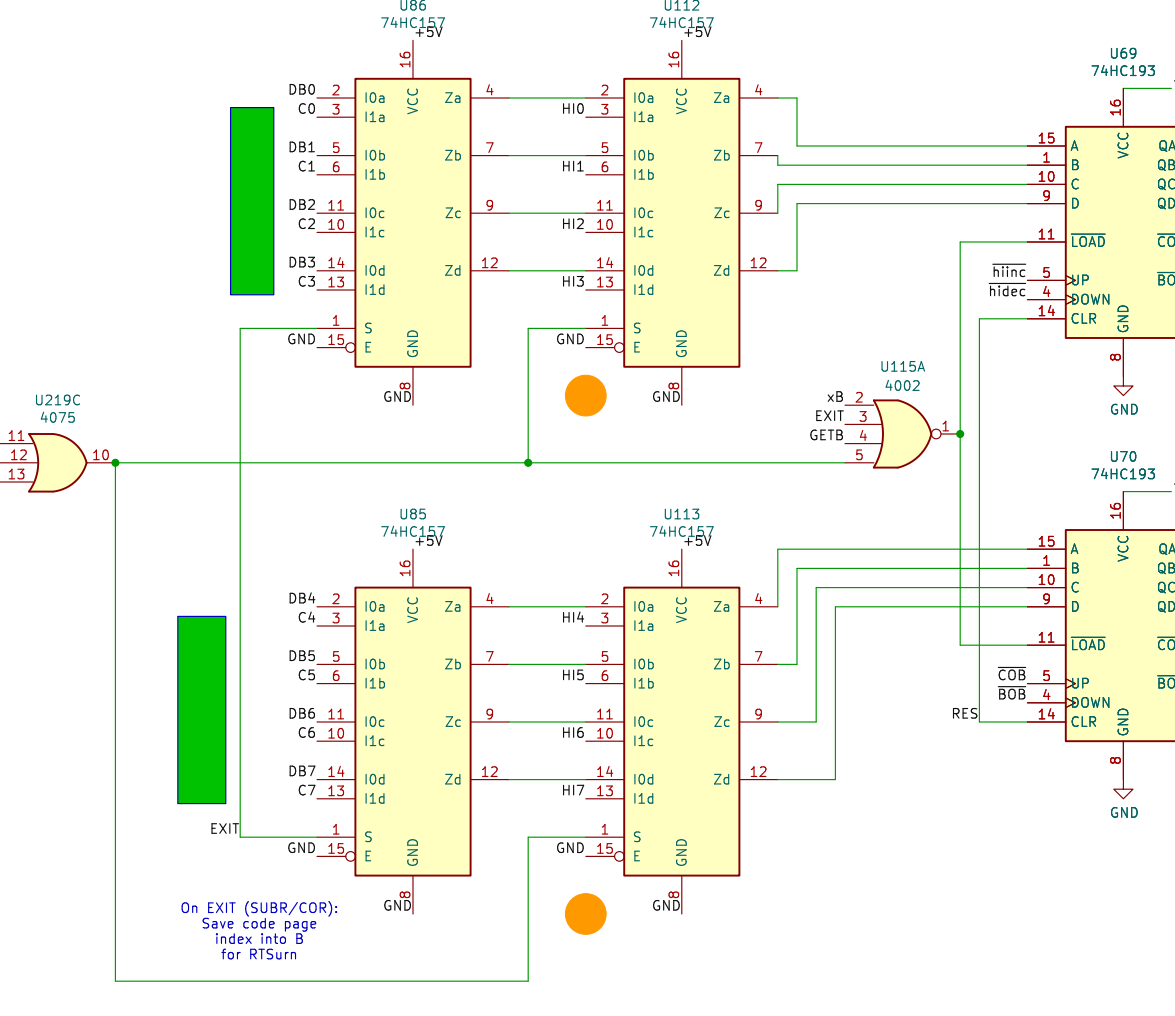
O (Page Offset Register)



B0 Pointer Registers



Pointer high

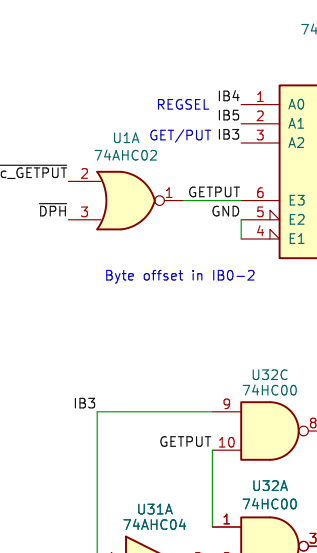


B (Base) Page Index

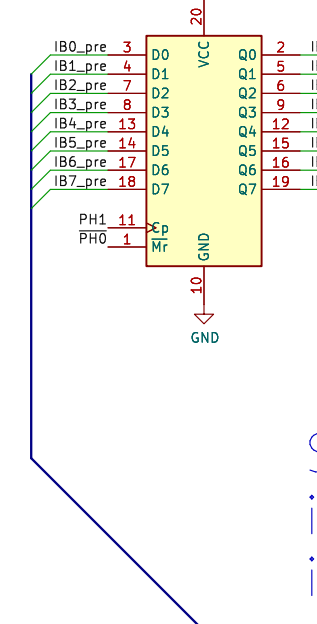


Instruction Decoder

GETPUT Decoder



Instruction-Word Latch



Start, latch instruction or interrupt vector

Trap calls to page 0 enable "BUSY", disabling interrupts

On instruction fetch: If IRQ and not BUSY, inject "TRAP 0" opcode, else fetch opcode from memory at C-PC

BUSY state removed by RTI instruction

Hardware IRQ TRAP instruction: 001.00000 to page 0

Trap calls to page 0 enable "BUSY", disabling interrupts

On instruction fetch: If IRQ and not BUSY, inject "TRAP 0" opcode, else fetch opcode from memory at C-PC

BUSY state removed by RTI instruction

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Trap calls to page 0 enable "BUSY", disabling interrupts

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Trap calls to page 0 enable "BUSY", disabling interrupts

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BUSY state removed by RTI instruction

Hardware IRQ TRAP instruction: 001.00000 to page 0

Trap calls to page 0 enable "BUSY", disabling interrupts

On instruction fetch: If IRQ and not BUSY, inject "TRAP 0" opcode, else fetch opcode from memory at C-PC

BUSY state removed by RTI instruction

Hardware IRQ TRAP instruction: 001.00000 to page 0

Input/Output

S Serial IO

Implements SPI functionality with dedicated SER/DES registers

SIR Serial Input Register

SOR Serial Output Register

E Device Enable Register

Two independent 4-bit groups (high/low) feed into 4-bit decoders for device selection

LOW ORDER SELECTOR

HIGH ORDER SELECTOR

P Parallel IO

Parallel Input Register

Parallel Output Register

LOW ORDER SELECTOR

HIGH ORDER SELECTOR

LOW ORDER SELECTOR

HIGH ORDER SELECTOR

LOW ORDER SELECTOR

HIGH ORDER SELECTOR

LOW ORDER SELECTOR

(Local) Page Index Register

Low order address bits after from A02 up to A01. These bits are used to select the local page index. The local page index is used to select the local page index.

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{LL[7..0]}

Low order address bits after from A02 up to A01. These bits are used to select the local page index. The local page index is used to select the local page index.

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RAM/ROM

RAM/ROM circuit diagram showing an 8-bit input A and an output. It uses a 74VHC00 (NAND), 74VHC04 (inverter), and 74VHC10 (monostable) to implement the RAM/ROM. The output is an 8-bit result.

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C (Code) Page Index

Code page index circuit diagram showing an 8-bit input A and an output. It uses a 74VHC00 (NAND), 74VHC04 (inverter), and 74VHC10 (monostable) to implement the code page index. The output is an 8-bit result.

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