Sonne-8 Microcontroller
Reference Schematics
Rev. Myth
Clock Phases
Chip "Footprint" External Connections
A (Accumulator)
Zero detection
ALU Instructions
0 IDA ("Identity A") A := A
1 IDT ("Identity T") A := T
2 OCA ("One's Complement T") A := ~A
3 OCT ("One's Complement T") A := ~T
4 SLA ("A shifted left") A := A << 1
5 SLT ("T shifted left") A := T << 1
6 SRA ("A shifted right") A := A >> 1
7 SRT ("T shifted right") A := T >> 1
8 AND ("A boolean-and T") A := A & T
9 IOR ("A inclusive-or T") A := A | T
10 EOR ("A exclusive-or T") A := A ^ T
11 ADD ("Add T to A) A := A + T, bits 0-7
12 CAR ("Carry bit of: A plus T") A := 9th bit of: A + T, 0 or 1
13 AL_ ("Is A less than T") A := (A<T)? 0xFF:0
14 AE_ ("Is A equal to T") A := (A==T)? 0xFF:0
15 AG_ ("Is A greater than T") A := (A>T)? 0xFF:0
ALU
D(OWN COUNTER) Inner-loops
Branching
Instruction Decoder
Scrounger
Pair DST Decoder
Pre-Decoders PAIR Target
Instruction byte:
all0: OPC_SYS 00000 xxx See table @ SYS decoder
else: OPC_STASH 00001 xxx See table @ STASH decoder
OPC_ALU 0001 xxxx See table @ ALU
OPC_TRAP 001 xxxxx b0-4: DEST PAGE
OPC_GETPUT 01 xx x xxx b0-2 OFFS, b3:GET/PUT, B4-5:REG(GETPUT)
OPC_PAIR 1 xxx xxxx b0-3 DST, b4-6 SRC
Instruction-Word Latch
Start, latch instruction or interrupt vector
Pair SRC Decoder
Pre-Decoder PAIR Source
SYS Decoder
TRAP decoder
BOPs Decoder
Opcode Type Decoder
GETPUT Decoder
(PC Program Counter)
Control Tree
Pointer low
O (Page Offset Register)
Pointer high
B (Base) Page Index
{PTRB[7..0]}
{DB[7..0]}
BO Pointer Registers
Input/Output
S
SIR
SOR
Serial IO
E
Device Enable
P
PIR
POR
Parallel IO
L (Local Page Index reg)
{LL[7..0]}
{LO[7..0]}
{HI[7..0]}
{DB[7..0]}
RAM/ROM
C (ODE) Page index
Based on working prototype PCB: https://github.com/michaelmangelsdorf/sonne8
Rev. Step "ToV"
Project homepage: https://github.com/michaelmangelsdorf/Myth
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Sheet: /
File: myth.kicad_sch
Title: Sonne-8 Micro-Controller
Size: A0
Date: 2025-06-04
Rev: Myth
KiCad E.D.A. 9.0.1
Id: 1/1