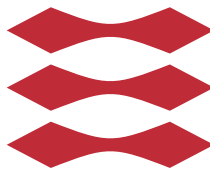


FPGA Implementation of a RISC-V processor

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Summary (English)

The goal of the thesis is to ...

Summary (Danish)

Målet for denne afhandling er at ...

Preface

This thesis was prepared at DTU Compute in fulfilment of the requirements for acquiring an M.Sc. in Engineering.

The thesis deals with ...

The thesis consists of ...

Lyngby, 17-January-2018

A handwritten signature in black ink that reads "Not Real". The word "Not" is written in a cursive style, and "Real" is written in a more upright, slightly cursive style.

Michael Mortensen

Acknowledgements

I would like to thank my....

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1.1 Project plan

CHAPTER 2

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Performance analysis

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Discussion

CHAPTER 6

Conclusion and Future Work

APPENDIX A

RISC-V Single-cycle Processor Overview and Chisel Description

This appendix is full of stuff ...

APPENDIX B

RISC-V Pipelined Processor Chisel Description

This appendix is full of stuff ...

APPENDIX C

Benchmarks C-code

This appendix is full of stuff ...

Bibliography
