ID	Task Name	Start	Finish	Duration
1	**Project description, plan and litterature search etc.**	01-Sep-17	28-Sep-17	4w
2	**Learn RISV-V**	01-Sep-17	14-Sep-17	2w
3	**Learn Chisel 2.2**	**01-Sep-17**	**11-Oct-17**	**5w 6d**
4	Reading and basic exercises	01-Sep-17	14-Sep-17	2w
5	Modularized single-stage design	14-Sep-17	11-Oct-17	4w
6	**5-stage pipelined design**	**13-Oct-17**	**01-Dec-17**	**7w 1d**
7	Plan and preparation	13-Oct-17	19-Oct-17	1w
8	Execution stage	20-Oct-17	26-Oct-17	1w
9	Instruction decode stage	27-Oct-17	02-Nov-17	1w
10	Instruction fetch stage	02-Nov-17	08-Nov-17	1w
11	Memory and write back stages	08-Nov-17	14-Nov-17	1w
12	Tests without hazards	14-Nov-17	15-Nov-17	2d
13	EX forwarding unit	16-Nov-17	16-Nov-17	1d
14	Hazard detection unit	17-Nov-17	17-Nov-17	1d
15	Comprehensive testing and debugging	18-Nov-17	01-Dec-17	2w
16	**5-stage pipelined FPGA implementation**	**18-Dec-17**	**05-Jan-18**	**2w 5d**
17	Plan and preparation	18-Dec-17	24-Dec-17	1w
18	Implementation and testing	25-Dec-17	31-Dec-17	1w
19	Performance and ressource analysis	01-Jan-18	05-Jan-18	5d
20	**Write repport**	01-Dec-17	17-Jan-18	6w 6d
21	**Hand in repport**	17-Jan-18	17-Jan-18	1d
22	**Prepare presentation**	17-Jan-18	31-Jan-18	2w 1d
23	**Present**	31-Jan-18	31-Jan-18	1d