FPGA Implementation of a RISC-V processor

Michael Mortensen

Kongens Lyngby 2018

Technical University of Denmark
Department of Applied Mathematics and Computer Science
Richard Petersens Plads, building 324,
2800 Kongens Lyngby, Denmark
Phone +45 4525 3031
compute@compute.dtu.dk
www.compute.dtu.dk

Summary (English)

The goal of the thesis is to ...

Summary (Danish)

Målet for denne afhandling er at ...

Preface

This thesis was prepared at DTU Compute in fulfilment of the requirements for acquiring an M.Sc. in Engineering.

The thesis deals with ...

The thesis consists of ...

Lyngby, 17-January-2018

Michael Mortensen

Acknowledgements

I would like to thank my....

Contents

Chapter 1

Introduction

1.1 Project plan

Chapter 2

Background

2.1 RISC-V in Embedded Systems and IoT

2.2 The RISC-V Instruction Set Architecture

2.2.1 ISA Variants

2.2.2 Standard Extensions

2.3 The RISC-V 5-stage Pipelined Processor

2.4 FPGA Technology

2.5 Hardware Design Flow

2.6 The Altera DE2-115 FPGA

2.6.1 General Overview

2.6.2 Integration of a RISC-V Core

Chapter 3

Design and Implementation

3.1 General Overview

3.2 Datapath

3.2.1 Instruction Fetch

3.2.2 Instruction Decode

3.2.3 Execution

3.2.4 Data Memory and Write Back

3.3 Control Logic

3.3.1 Main Control Logic

3.3.2 Hazard Detection Logic

3.3.3 Forwarding Logic

3.4 Chisel Testing and Simulation

3.5 Hardware Implementation

3.6 Ressource Utilization

3.7 Ressource Optimizations

3.7.1 Control

3.7.2 Datapath

Chapter 4

Performance analysis

4.1 Overview and Methodology

4.2 Benchmark Testing

4.2.1 Quicksort

4.2.2 Matrix Multiplication

Chapter 5

Discussion

Chapter 6

Conclusion and Future Work

Appendix A

RISC-V Single-cycle Processor Overview and Chisel Description

This appendix is full of stuff ...

Appendix B

RISC-V Pipelined Processor Chisel Description

This appendix is full of stuff ...

Appendix C

Benchmarks C-code

This appendix is full of stuff ...

Bibliography