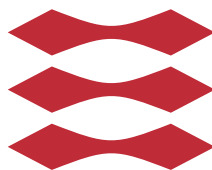


# FPGA Implementation of a RISC-V processor

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# Summary (English)

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The goal of the thesis is to ...



# Summary (Danish)

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Målet for denne afhandling er at ...



# Preface

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This thesis was prepared at DTU Compute in fulfilment of the requirements for acquiring an M.Sc. in Engineering.

The thesis deals with ...

The thesis consists of ...

Lyngby, 17-January-2018

A handwritten signature in black ink that reads "Not Real". The word "Not" is written in a cursive style, and "Real" is written in a more upright, slightly cursive style.

Michael Mortensen





# Acknowledgements

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I would like to thank my....



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# CHAPTER 1

## Introduction

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### 1.1 Project plan



## CHAPTER 2

# Background

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## 2.1 RISC-V in Embedded Systems and IoT

## 2.2 The RISC-V Instruction Set Architecture

### 2.2.1 ISA Variants

### 2.2.2 Standard Extensions

## 2.3 The RISC-V 5-stage Pipelined Processor

## 2.4 FPGA Technology

## 2.5 Hardware Design Flow

## 2.6 The Altera DE2-115 FPGA

### 2.6.1 General Overview

### 2.6.2 Integration of a RISC-V Core



## CHAPTER 3

# Design and Implementation

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## 3.1 General Overview

## 3.2 Datapath

### 3.2.1 Instruction Fetch

### 3.2.2 Instruction Decode

### 3.2.3 Execution

### 3.2.4 Data Memory and Write Back

## 3.3 Control Logic

### 3.3.1 Main Control Logic

### 3.3.2 Hazard Detection Logic

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## 3.7 Ressource Optimizations

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## CHAPTER 4

# Performance analysis

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### 4.1 Overview and Methodology

### 4.2 Benchmark Testing

#### 4.2.1 FIR Filter

#### 4.2.2 Matrix Multiplication



## CHAPTER 5

# Discussion

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## CHAPTER 6

# Conclusion and Future Work

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## APPENDIX A

# RISC-V Single-cycle Processor Overview and Chisel Description

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This appendix is full of stuff ...



## APPENDIX B

# RISC-V Pipelined Processor Chisel Description

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This appendix is full of stuff ...



## APPENDIX C

# Benchmarks C-code

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This appendix is full of stuff ...





# Bibliography

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