02205: Lab 3 Assignment

The purpose of this exercise is to design a power efficient simple numerical processor, make its layout, and estimate its power consumption under several processing patterns.

The circuit chosen for the exercise is a computation kernel used in the Singular Value Decomposition (SVD) algorithm. The kernel implements a single Jacobi's rotation:

$$\begin{aligned} x_R &= x \cdot cos(\theta) + y \cdot sin(\theta) \\ y_R &= y \cdot cos(\theta) - x \cdot sin(\theta) \end{aligned} \tag{1}$$

Assume that $sin(\theta)$ and $cos(\theta)$ are input to the unit: i.e., the computation of the trigonometric functions is not part ot this assignment. The four inputs, x, y, $w = cos(\theta)$, and $v = sin(\theta)$, are 20-bit fixed point numbers with range $[-1.0, 1.0]$. For example, the largest positive number 1.0 is represented in binary as `01.00 0000 0000 0000 0000`$|_2$ with 18 fractional bits, 1 integer bit, and 1 sign bit.

The two outputs, x_R and y_R, are also 20-bit fixed point numbers with range $(-2.0, 2.0)$. For example, for $x = 1.0$, $y = 1.0$, and $\theta = \frac{\pi}{4}$:

$$x_R = x \cdot cos(\theta) + y \cdot sin(\theta) = 1.0 \cdot \frac{\sqrt{2}}{2} + 1.0 \cdot \frac{\sqrt{2}}{2} = \sqrt{2} = 01.01\ 1010\ 1000\ 0010\ 0111|_2$$

The unit is also used to compute the single operation (dot-product)

$$s = x \cdot w + y \cdot v \tag{2}$$

and the weighted difference

$$d = y \cdot w - x \cdot v \tag{3}$$

both with the same precision as (1).

The design tasks to be performed are the following:

1. RTL-level design: design the unit, creating the top level and the testbench.
2. Pipeline the unit to meet the target clock frequency/period.
3. Place&route the unit and estimate the power consumption.

In the rest of this assignment, we assume the same tools set-up and library used in the tutorials.

Design Task 1: RTL-level Design

The starting point is 20×20 multiplier. The VHDL can be downloaded from `/apps/misc/02205/labs/lab3` .

Four multipliers have to be connected to one adder and one subtractor to implement (1). Make sure that the 40-bit output of the multipliers is matched to the 20-bit unit outputs.

Build the testbench and make sure the unit computes correctly the operations in (1), (2) and (3).

Design Task 2: Pipeline the Unit

The second step is to pipeline the unit of Design Task 1 to achieve a throughput of 1.0 GOPS[1] (clock frequency $f_C = 1.0\ GHz \ \rightarrow\ T_C = 1\ ns$).

Then, you have to modify the test-bench and run functional simulations to make sure the applied pipelining does not generate errors.

Design Task 3: Layout and Power Efficient Design

Task 3.1: Layout

For the layout, you can use the scripts of the tutorial, but you have to apply some modifications. These are

1. In the floorplanning step you might need to make the power grid larger (more horizontal and vertical straps) if the IR drop il too large.

   To check the floorplan look at file `pna_output/floorplan.PNS.log`.

   If the IR drop > 200 mV you have to add more power straps. This is done by editing the lines

   ```
   set_fp_rail_constraints -add_layer -layer M6 -direction horizontal
         -max_strap 128 -min_strap 12 -min_width 0.2 -spacing minimum
   set_fp_rail_constraints -add_layer -layer M5 -direction vertical
         -max_strap 128 -min_strap 12 -min_width 0.2 -spacing minimum
   ```

   in the file `scripts/floorplanning.tcl` and by running it again.

   To increase the number of straps, modify the value of `min_strap`. There is no rule about how to set `min_strap`, and it is a trial & error process.

2. After placement and routing, check in the log file for any error messages, or use the following command

   ```
   icc_shell> report_design_physical -all
   ```

3. If you cannot reach timing closure, you can relax the timing constraints (larger clock period) by editing the file `scripts/place.tcl` and adding the following command

   ```
   create_clock -name "CLK" -period 1.2 -waveform {0.0 0.6} {CLOCK}
   ```

   after the line "`open_mw_cel place`".

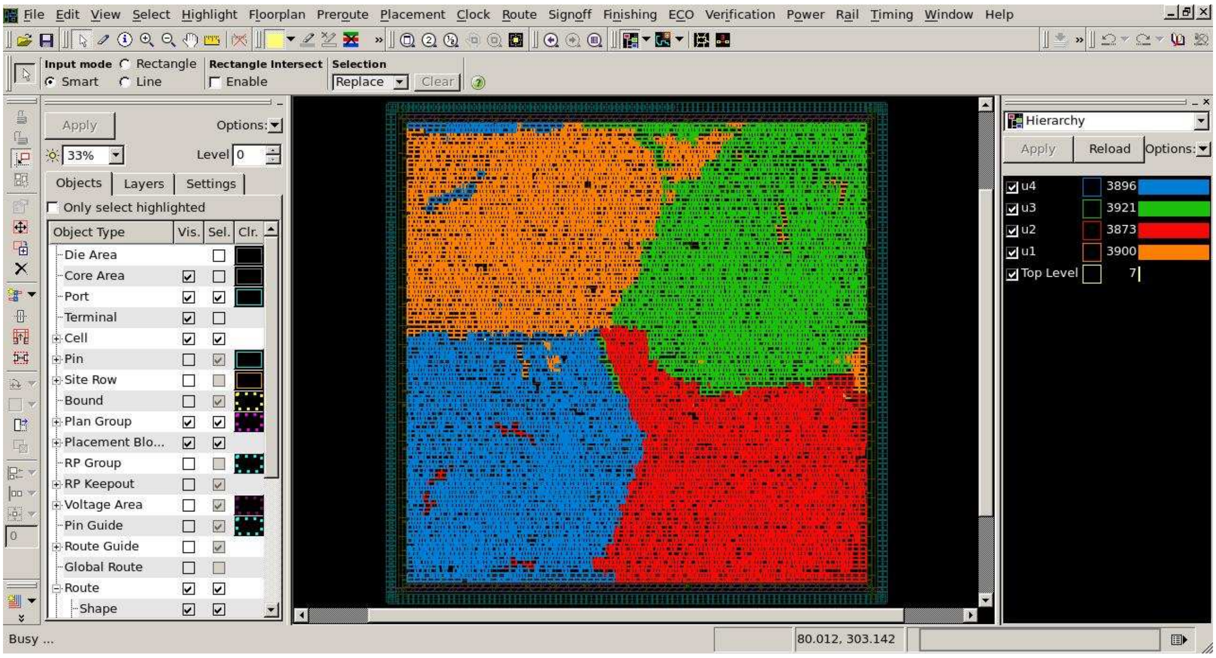
   Then, run the script `scripts/place.tcl` again.

To highlight the different multipliers in different colors, similarly to Figure 1, in the menu bar of the layout window, select

View → **Visual Mode**.

A sub-window should appear at the right of the layout. Select **Hierarchy** from the list in the sub-window, then click **Reload**, then click **OK** in the pop-up window.

[1] Giga Operations Per Second.


File Edit View Select Highlight Floorplan Preroute Placement Clock Route Signoff Finishing ECO Verification Power Rail Timing Window Help
Input mode
Rectangle Intersect
Selection
Replace
Clear
Apply
Options:
Objects
Layers
Settings
Hierarchy
Apply
Reload
Options:
Busy ...

Input mode: ● Smart ○ Rectangle ○ Line

Rectangle Intersect: □ Enable

33% Level 0

□ Only select highlighted

Object Type	Vis.	Sel.	Clr.
Die Area		□	■
Core Area	☑	□	■
Port	☑	☑	■
Terminal	☑	□	
Cell	☑	☑	
Pin	□	☑	■
Site Row	□	□	■
Bound	□	☑	▨
Plan Group	☑	☑	▨
Placement Blo...	☑	☑	
RP Group	□	□	▨
RP Keepout	□	☑	
Voltage Area	□	☑	■
Pin Guide	□	☑	▨
Route Guide	□	☑	
Global Route	□	□	
Route	☑	☑	
Shape	☑	☑	

☑ u4	□	3896	🟦
☑ u3	□	3921	🟩
☑ u2	□	3873	🟥
☑ u1	□	3900	🟧
☑ Top Level	□	7	

80.012, 303.142

Figure 1: Example of floorplan with four identical cores.

Task 3.2: Power Estimation

After the layout is built without errors, the next step is to estimate the power when executing the three operations in (1), (2) and (3).

Modify the testbench to create the patterns to activate only the two relevant multipliers and adder/subtractor when executing operation (2) and (3).

Design Task 4 (Optional): Thermal analysis

Once you have completed Task 3, you can create the thermal maps for the execution of the three operations in (1), (2) and (3), by following the instructions in Tutorial T6 `http://people.compute.dtu.dk/alna/eda/tutorial/T6_thermalMaps.html`.

This task is optional.

Report for Lab 3

You must write a report (max. 15 pages) of the work performed. The report must include, figures, diagrams, tables, etc.

In particular, you have to answer the following questions in the report.

1. What are the number of stages, latency and area for the unit you designed?
2. Where are the pipeline registers placed? Show it with a figure.
3. What is the power dissipation for the three operations in (1), (2) and (3)?

4. Did you use any low power design method?
5. After the layout, can the unit still sustain the 1.0 GOPS throughput? Explain.
6. If you performed the thermal analysis, what are the average and highest chip temperatures? For which operaration is the highest temperature obtained?

The report, only PDF format is accepted, must be uploaded on Campusnet by the deadline.

As an appendix to the report, all the VHDL code and test patterns must be included in a separate file (ZIP format) and uploaded on Campusnet as well.