Technical University of Denmark

Laboratory Exercise 3

Course:
02205 - F18

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Introduction

In this report, we document our efforts in designing a power efficient simple numerical processor for Singular Value Decomposition (SVD), making its layout and estimating its power consumption under several processing patterns. The computational kernel implements a simple Jacobi's rotation:

$$x_r = x \cdot \cos(\theta) + y \cdot \sin(\theta) \tag{1}$$

$$y_r = y \cdot \cos(\theta) - x \cdot \sin(\theta) \tag{2}$$

The four inputs x, y, $w = \cos(\theta)$ and $v = \sin(\theta)$ are 20-bit fixed point numbers (Q1.18) with the allowed range [-1.0,1.0]. The processing unit is also used to compute the single operation (dot-product)

$$s = x \cdot w + y \cdot v \tag{3}$$

and the weighted difference

$$d = y \cdot w - x \cdot v \tag{4}$$

Where the outputs s and d has a range of]-2.0,2.0[.

RTL Design

The circuit for the kernel used in the SVD algorithm was described at register-transfer level. This required the connection of four multipliers to one adder and one subtractor in order to compute (1) and (2). The VHDL code for the 20×20 multiplier was provided for this lab, however, we were required to construct the VHDL for the other components of the circuit which included the 20-bit fixed-point adder and subtractor. The top level RTL design of this circuit can be seen in Figure 1.

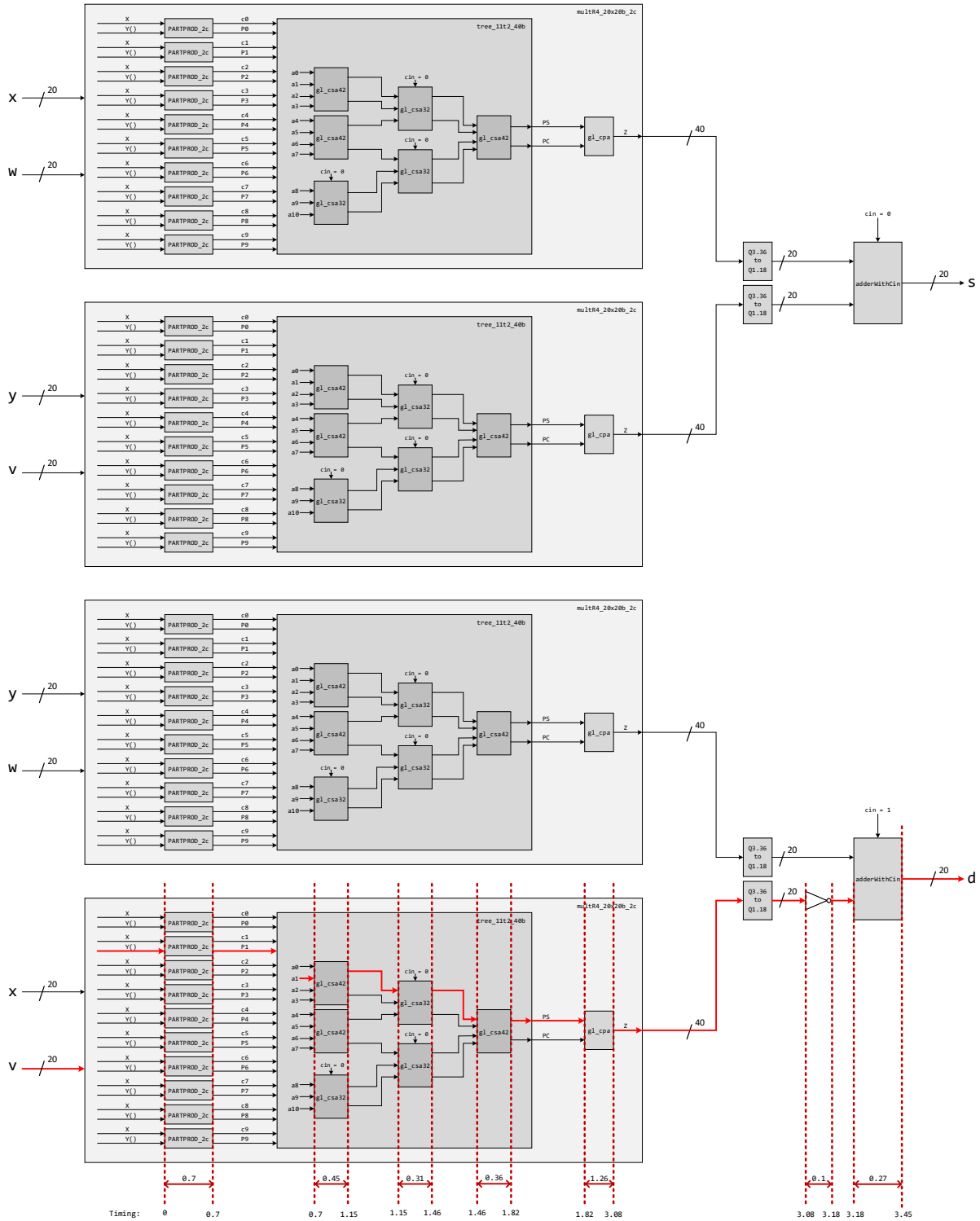


FIGURE 1: Diagram for the SVD circuit showing delays for the components in nanoseconds with no optimization applied.

Pipelined Circuit

The synthesis of the non-pipelined version did not meet the timing constraint $T_c = 1ns$. It was therefore necessary to pipeline the design to meet this constraint. This was done by converting the design to a two stage pipelined circuit as shown in Figure 2. This design introduced a pipeline stage at the inputs and another stage inside the multipliers.

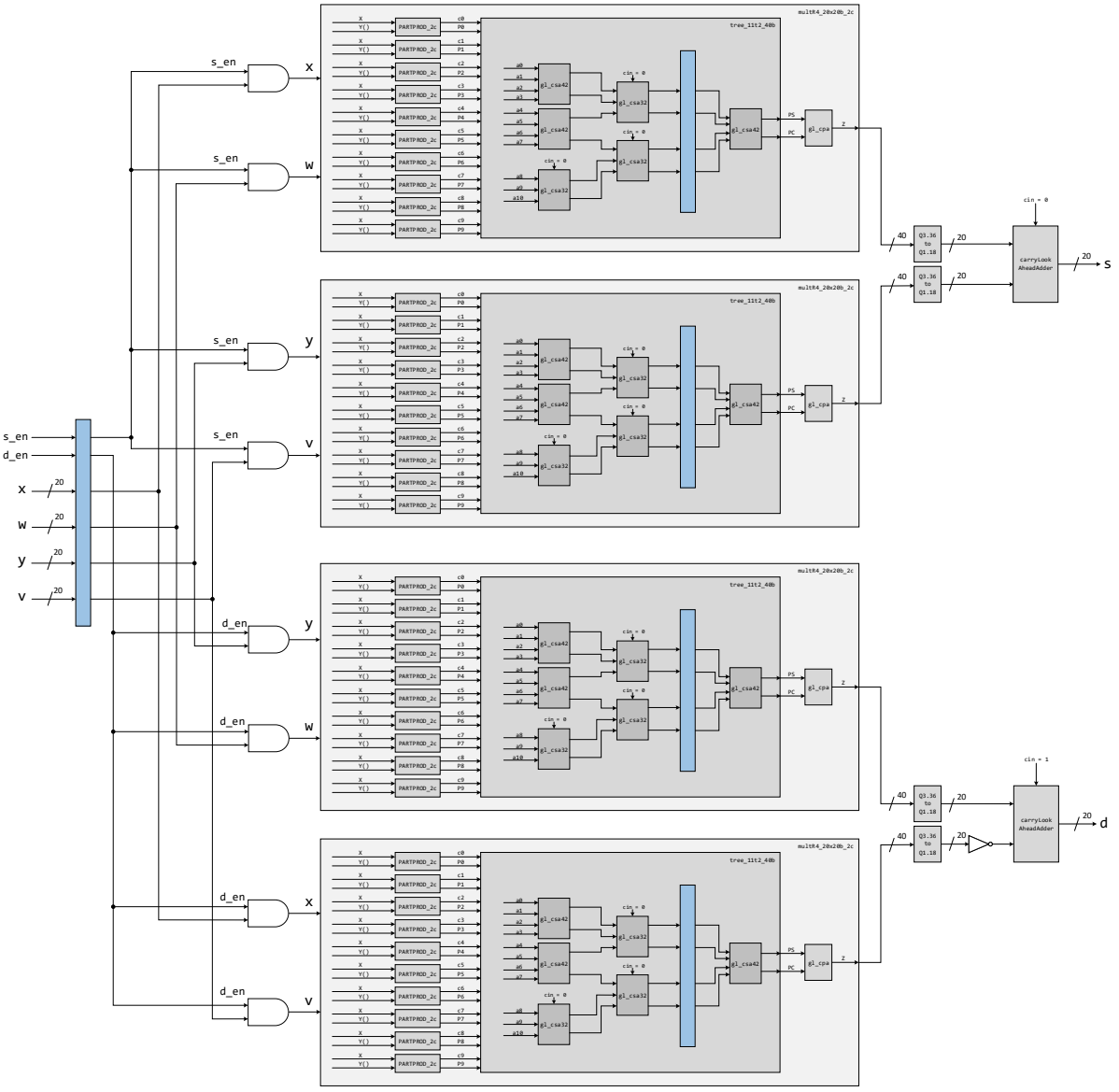


FIGURE 2: Diagram for the Singular Value Decomposition circuit with the pipeline registers shown (blue).

Power Optimization Using Enable

In the pipelined circuit shown in Figure 2, it can be seen that four multipliers are required to implement the numerical processor. The calculation for the single operation (dot-product) and the weighted difference only requires 2 multipliers each, therefore, 2 multipliers are unused during either of these calculations. This leads to the unnecessary dissipation of power in the 2 unused multipliers. To solve this, the four multipliers are controlled with an enable signal using AND-gates with `s_en` and `d_en` signals, ensuring that the internals of the multipliers only switch when required, thus greatly decreasing the power dissipated doing dot-product or weighted difference computation.

Layout and Power Efficient Design

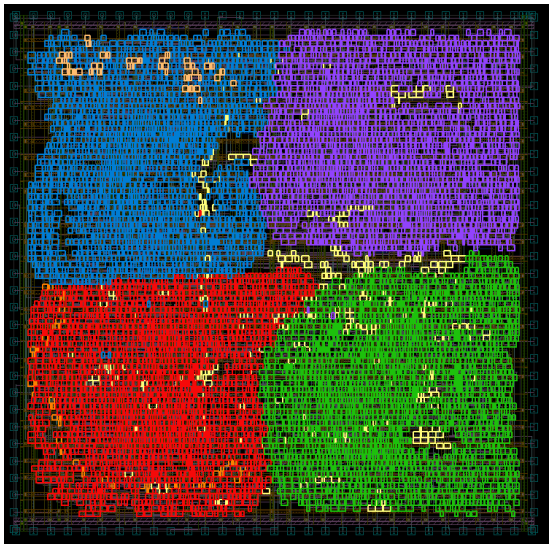
After the layout, the unit can still sustain the timing constraint. From a timing analysis we found the critical path to be from the input register to the register in the adder tree of the second multiplier that gives a slack of $0.001967ns$. With the timing constraint of $T_c = 1ns$ met it was now possible to examine layout and power efficiency of the design.

Floor-plan

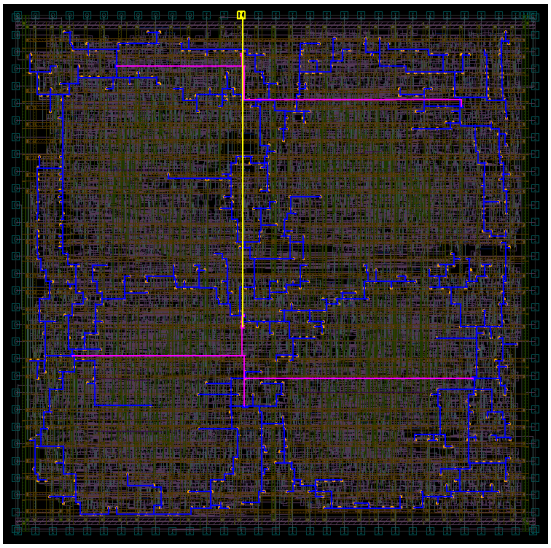
The floor-plan process is used to determine the shape and size of the design cell and create a power plan. The process places standard cells to initially determine the core area which it places the pins and power rings around. These power rings are connected to the standard cells using vertical straps in metal 5 and horizontal straps in metal 6. To construct the required power grid layer horizontal and vertical straps were used. To determine the number of straps to implement in order to obtain the desired IR drop, an iterative method is used. It was sought to obtain an IR drop less than 200mV. In order to reduce the IR drop below this threshold, more power straps could be added to make the power grid larger. The 200mV target was met with a max straps of 128 and min straps of 8.

Placement and Routing

With the completion of the floor planning we have achieved the layout of the design with power rings and straps. It is now necessary to determine the placement and routing of the signals. The routing process connects all the signals including the pin signals. The result of the routing is shown in Figure 3



(A) Layout (placed and routed) screenshot showing each of the multipliers in a distinct colour.



(B) The clock distribution network highlighted.

FIGURE 3: Layout results for the multipliers and the clock distribution network.

Power Results

Table 1 provides the power dissipation results for each of the Jacobi, dot product and weighted difference computation circuits. The table shows the switching, internal, leakage and total power dissipation for each of them.

TABLE 1: Power results for the pipelined with enable versions of the Jacobi, dot-product and weighted difference computations.

Block	Switching [µW]	Internal [µW]	Leakage [µW]	Total [µW]
Jacobi	1 390.7	2 547.4	106.91	4 045.0
Dot-product	854.6	1 751.4	106.27	2 712.2
Weighted difference	825.0	1 689.6	106.37	2 621.0

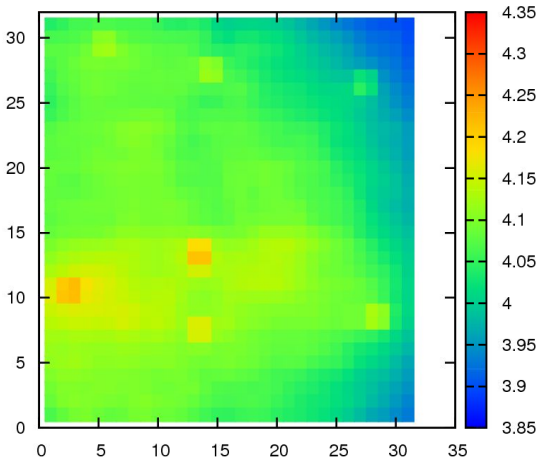
Table 2 provides the area results for the circuits. We observe that the pipelined version with enable is significantly larger than the non-pipelined version. This is expected because of the enable logic and registers, which takes up around 30% of the area.

TABLE 2: Area results for synthesis at a 1 ns clock period with optimizations applied for low dynamic and leakage power.

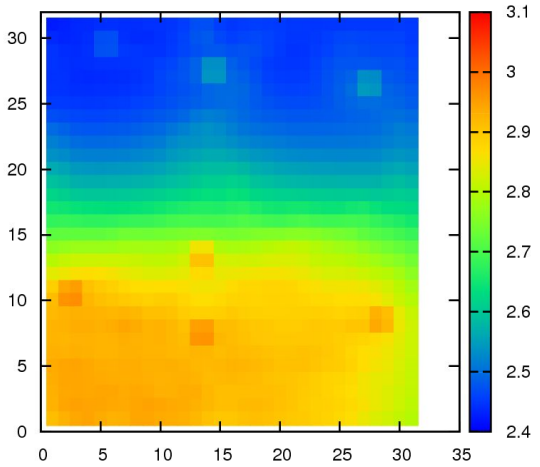
	Non-pipelined	Pipelined with Enable
Area [µm^2]	52 874	81 059

Thermal Analysis

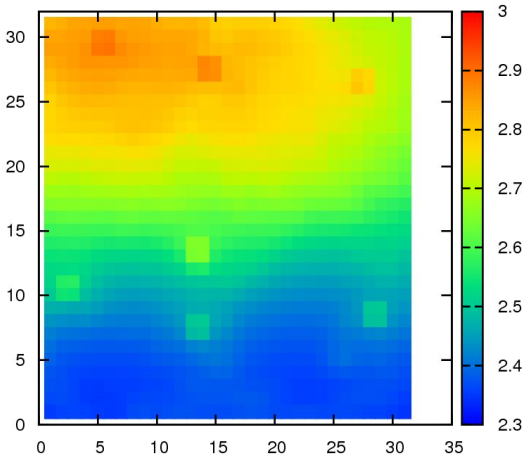
Running a post layout simulation in VCS allowed for the heating of the chip to be analyzed. This thermal analysis was computed with a test-bench clock period of $T_c = 10ns$. The results from this analysis can be seen illustrated in Figure 4.



(A) Thermal map of the design doing the jacobi computation.



(B) Thermal map of the design doing only the dot-product computation (s).



(C) Thermal map of the design doing only the weighted difference computation (d).

FIGURE 4: Thermal maps for the design computing Jacobi's rotation, dot-product, and weighted difference respectively. The resolution is set to 32x32 and a scaling factor of 10 have been used to scale the $10ns$ clock-cycle on the simulation to a $1ns$ clockcycle.

It is evident from the findings in Figure 4 that the greatest heating of the chip was incurred by the Jacobi computation, this is a result of the computation requiring almost the entirety of the chip's area. In contrast, both the dot-product computation and the weighted difference computation each used separate halves of the chip which explains their results from the thermal analysis being almost the inverse of each other thus inducing far less heating of the chip.

Conclusion

A fixed-point Singular Value Decomposition processing unit was pipelined to meet timing constraints and its power consumption optimized by enabling the multiplier blocks. Area results showed that the pipelining incurred a significant overhead in area, compared to a non-pipelined version. Furthermore, a layout of the system was done using IC compoiler, which for this design met the IR droop requirements. Moreover, the clock of 1 GHz was met for the layout. Finally, the temperature of the placed layout was tested.