EECS 168 Lab 4.1

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Lab 4, Week 1 CheckOff Video: Simulation result of example counter, The result of gate-level for 4-bit full adder, fa_4bit_synthesized.v, Final layout in Fig 49 for 4-bit full adder:

https://drive.google.com/file/d/1Gfcjyek2pv3z3xdi0ATqr1SYgyYxOCKm/view?usp=sharing

Summary

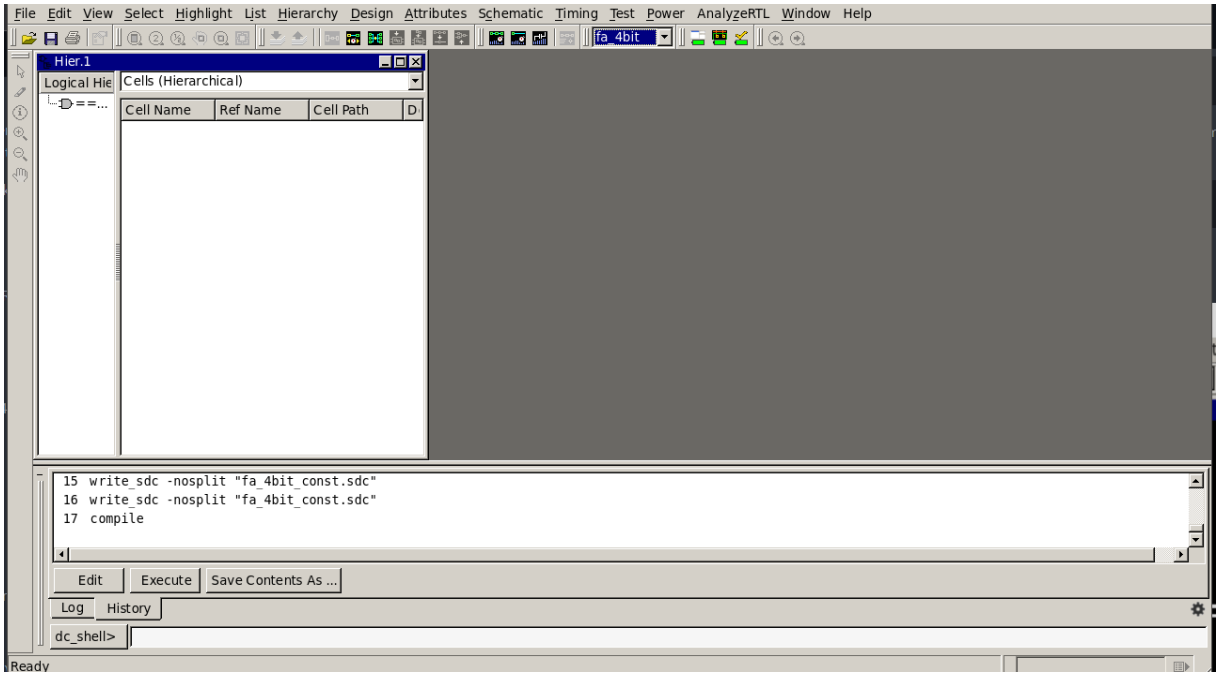
_____In this part of the lab, I gained experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design. I also gained experience transforming a gate-level netlist into a placed and routed layout using Synopsys IC Compiler (ICC). ICC takes a synthesized gate-level netlist and a standard cell library as input, then produces layout as an output. This was done with my 4 bit full adder.

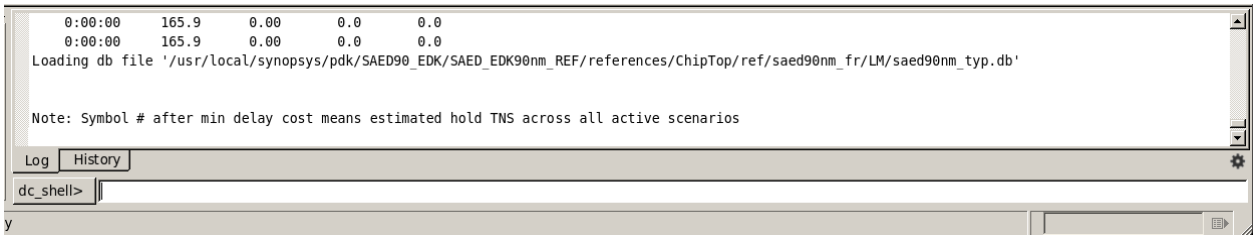
Simulation result of example counter:

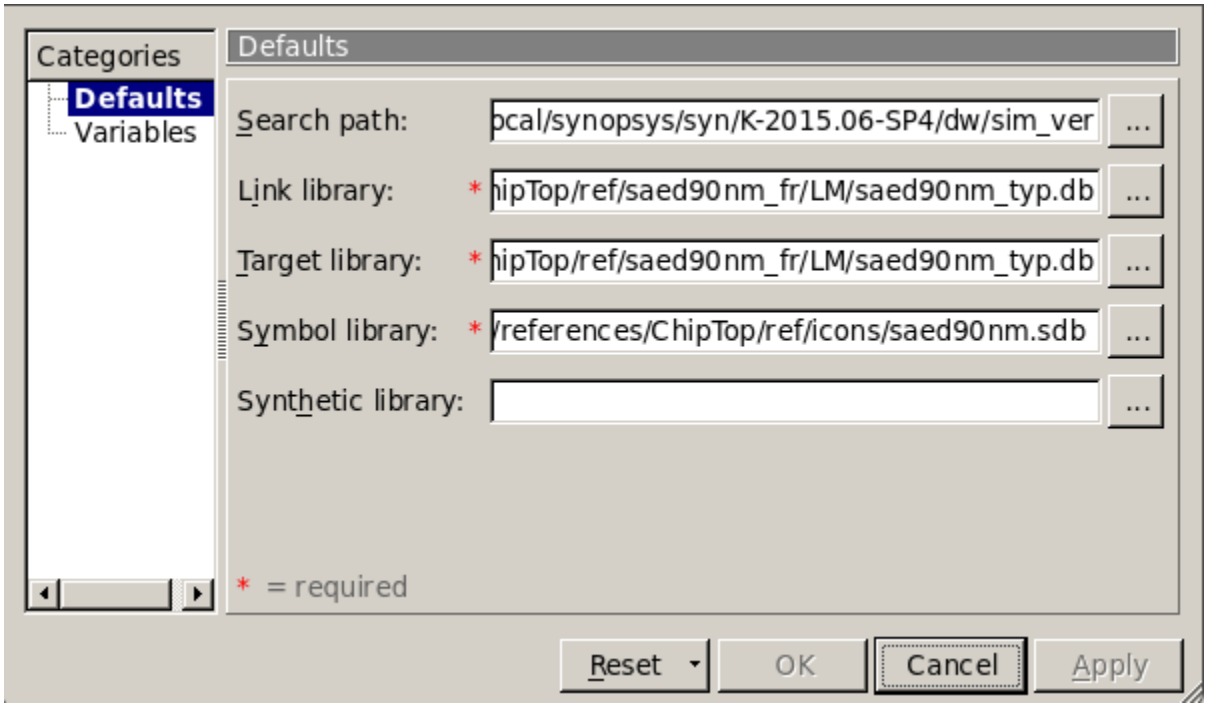
```
Contains Synopsys proprietary information.
Compiler version K-2015.09-SP1-1; Runtime version K-2015.09-SP1-1;  Mar  1 17:57
 2022
time=    0 ns, clk=0, reset=0, out=xxxx
time=   10 ns, clk=1, reset=0, out=xxxx
time=   11 ns, clk=1, reset=1, out=xxxx
time=   20 ns, clk=0, reset=1, out=xxxx
time=   30 ns, clk=1, reset=1, out=xxxx
time=   31 ns, clk=1, reset=0, out=0000
time=   40 ns, clk=0, reset=0, out=0000
time=   50 ns, clk=1, reset=0, out=0000
time=   51 ns, clk=1, reset=0, out=0001
time=   60 ns, clk=0, reset=0, out=0001
time=   70 ns, clk=1, reset=0, out=0001
time=   71 ns, clk=1, reset=0, out=0010
time=   80 ns, clk=0, reset=0, out=0010
time=   90 ns, clk=1, reset=0, out=0010
time=   91 ns, clk=1, reset=0, out=0011
time=  100 ns, clk=0, reset=0, out=0011
time=  110 ns, clk=1, reset=0, out=0011
time=  111 ns, clk=1, reset=0, out=0100
time=  120 ns, clk=0, reset=0, out=0100
time=  130 ns, clk=1, reset=0, out=0100
time=  131 ns, clk=1, reset=0, out=0101
time=  140 ns, clk=0, reset=0, out=0101
time=  150 ns, clk=1, reset=0, out=0101
time=  151 ns, clk=1, reset=0, out=0110
time=  160 ns, clk=0, reset=0, out=0110
time=  170 ns, clk=1, reset=0, out=0110
All tests completed sucessfully


$finish called from file "counter_tb.v", line 55.
$finish at simulation time  171.0 ns
          V C S   S i m u l a t i o n   R e p o r t
Time: 171000 ps
CPU Time:      0.300 seconds;       Data structure size:   0.0Mb
Tue Mar  1 17:57:42 2022
bender /home/cemaj/modea/eecs168/lab4-rtl/counter $ \
```

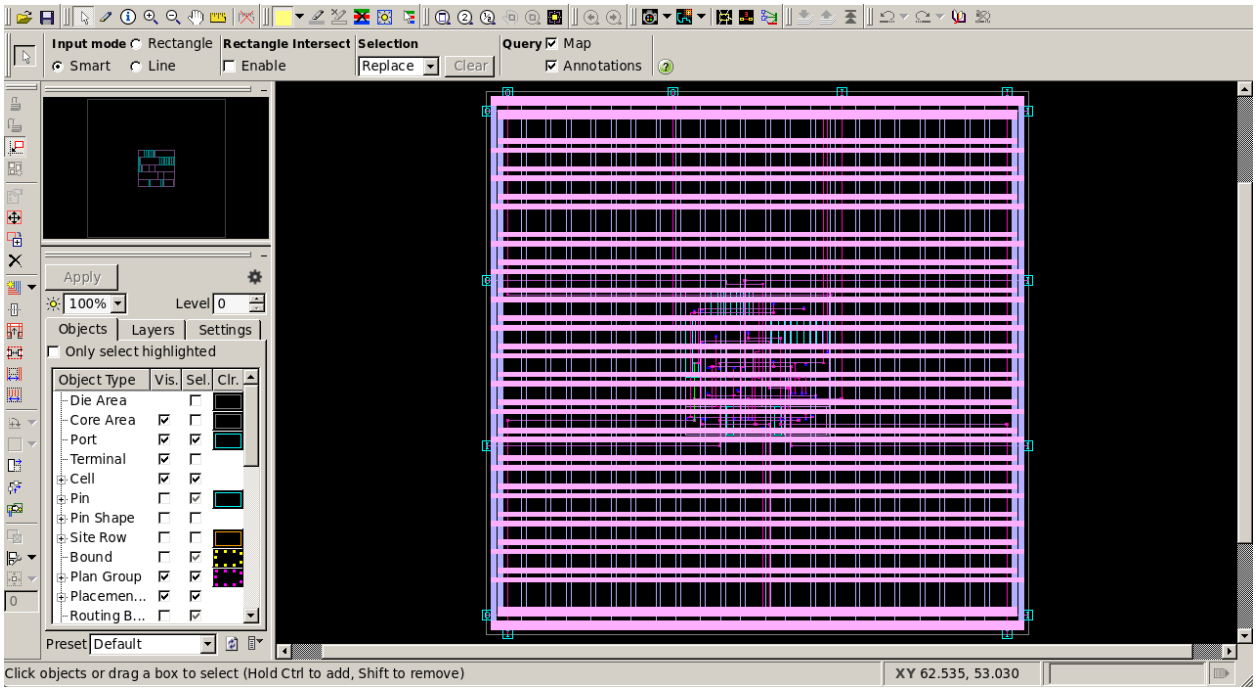
The result of gate-level for 4-bit full adder:


File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
fa_4bit
Hier.1
Logical Hie
Cells (Hierarchical)
Cell Name
Ref Name
Cell Path
D
15 write_sdc -nosplit "fa_4bit_const.sdc"
16 write_sdc -nosplit "fa_4bit_const.sdc"
17 compile
Edit
Execute
Save Contents As ...
Log
History
dc_shell>
Ready


0:00:00 165.9 0.00 0.0 0.0
0:00:00 165.9 0.00 0.0 0.0
Loading db file '/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db'
Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios
Log
History
dc_shell>


Categories
Defaults
Variables
Defaults
Search path:
pcal/synopsys/syn/K-2015.06-SP4/dw/sim_ver
Link library:
hipTop/ref/saed90nm_fr/LM/saed90nm_typ.db
Target library:
hipTop/ref/saed90nm_fr/LM/saed90nm_typ.db
Symbol library:
/references/ChipTop/ref/icons/saed90nm.sdb
Synthetic library:
* = required
Reset
OK
Cancel
Apply

Final layout in Fig 49 for 4-bit full adder:



Issues

The only issue that I had in this lab was trying to view my synthesized 4 bit full adder. It wouldn't output and display the schematic even though I had no errors in setting it up after multiple tries. My final layout also differs from the example, but this is most likely the case of my 4 bit adder being different from the example setup one in lab 3. Other than that this lab was fine and I was able to run it without errors.