EECS 168 Lab 1

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Session 21
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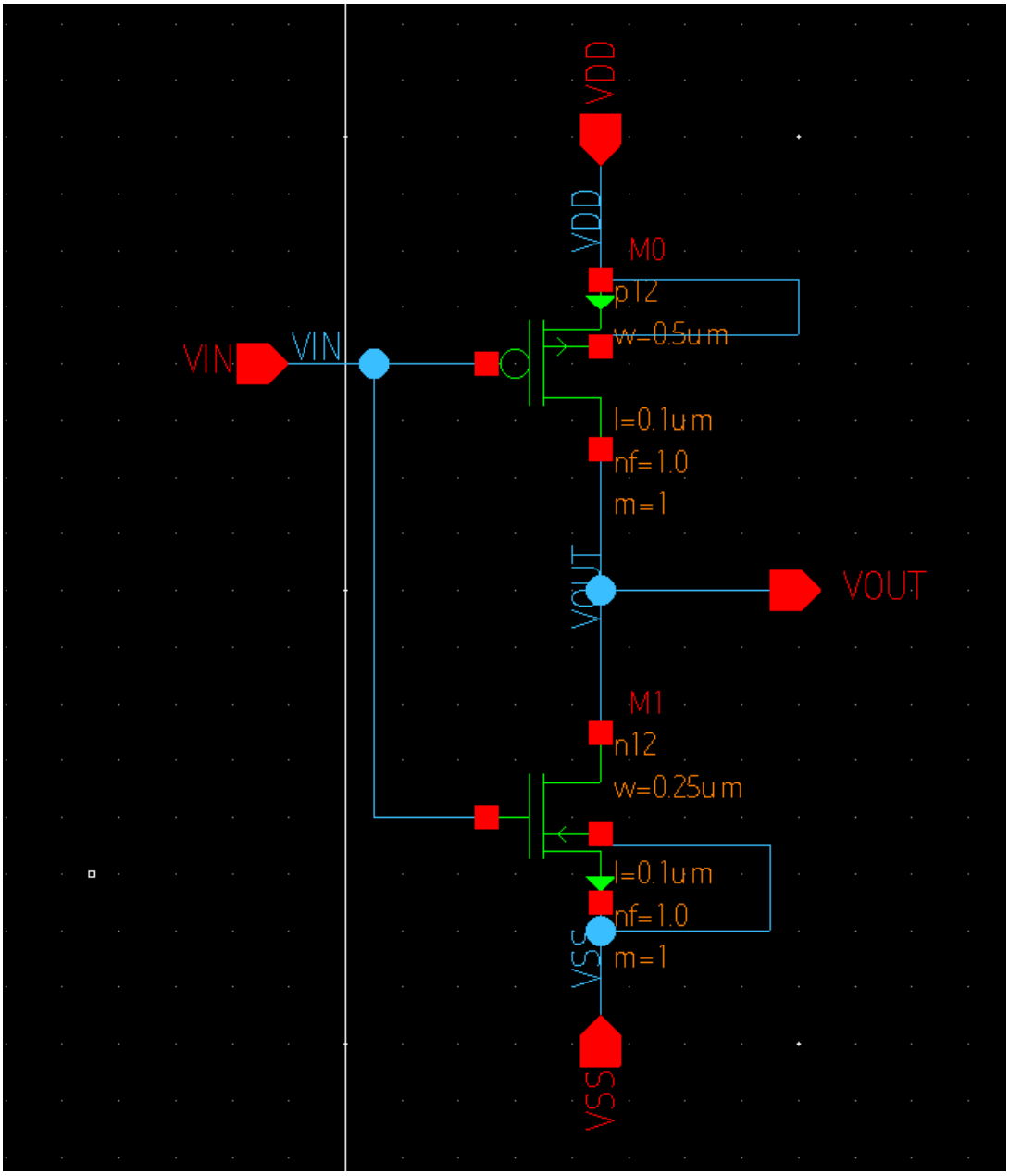
Video Link:
https://drive.google.com/file/d/1-_TIx5cbv3tWvmDh0EtP_Y78-d6h3RU7/view?usp=sharing

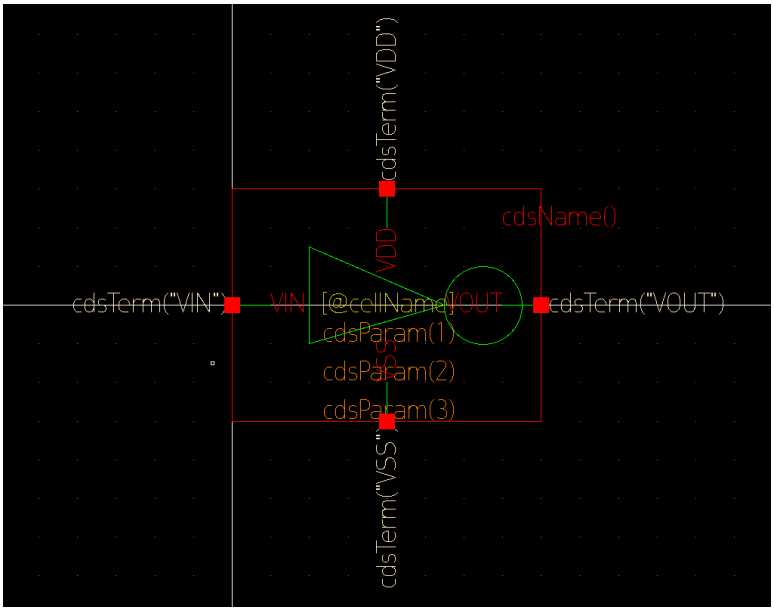
Summary

In this lab, I learned how to design circuits in CDesigner, how to generate netlist, and also how to simulate the given netlist to view various outputs in order to work on Lab 2's layout design. I also learned how to use three IC design tools (Custom Designer, Waveform View, HSPICE) in this lab. I learned how to group and ungroup waveforms together in Waveview and how to measure the various voltages and currents. Through the simulations and design tools, I was able to change the input and output signals accordingly and through application, was able to see first hand what the rise and fall measurement tool does. This lab also taught myself how to run a DC sweep and transient analysis from the Simulation and Analysis (SAE) environment.

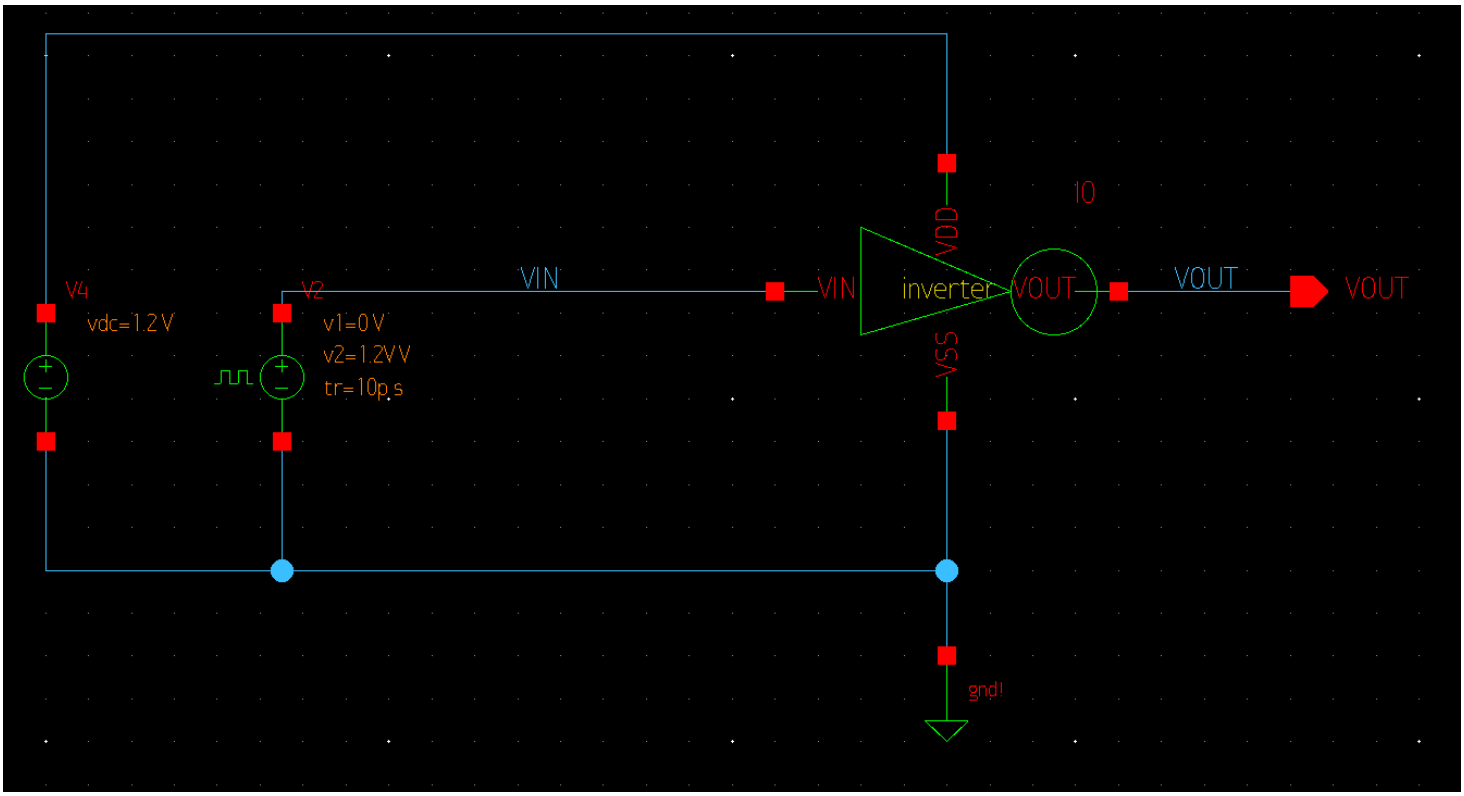
An inverter schematic view



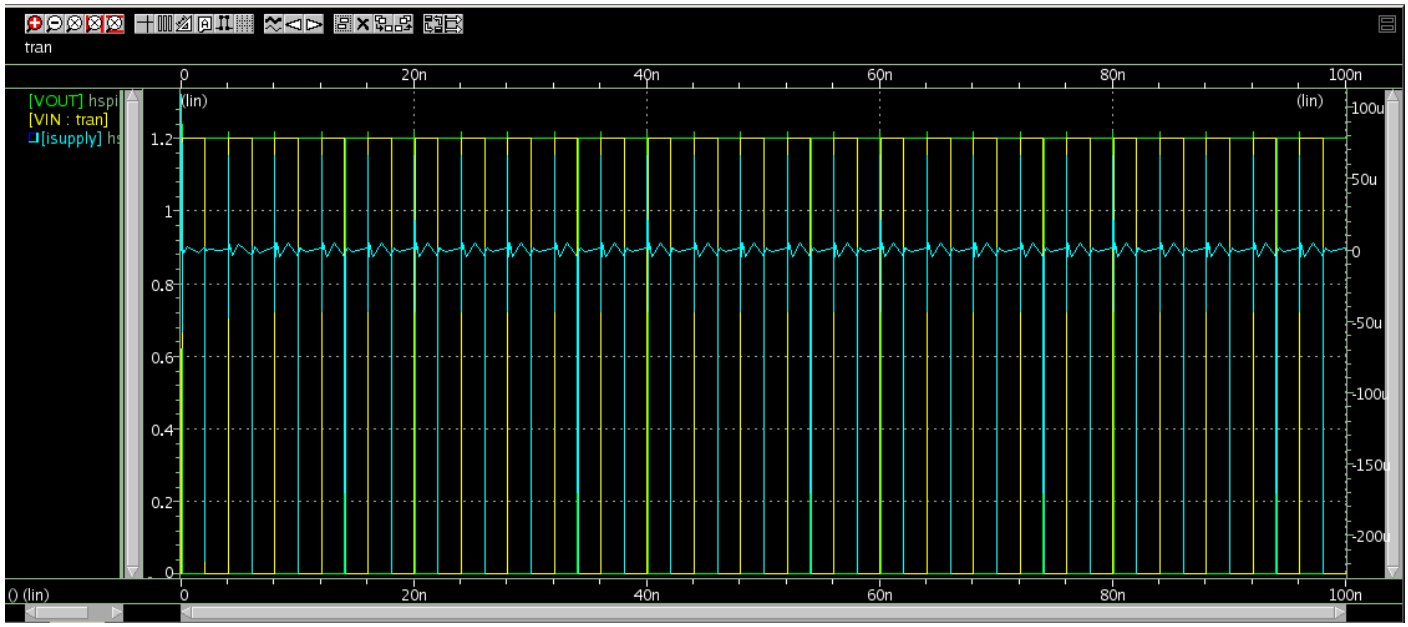
An inverter symbol view



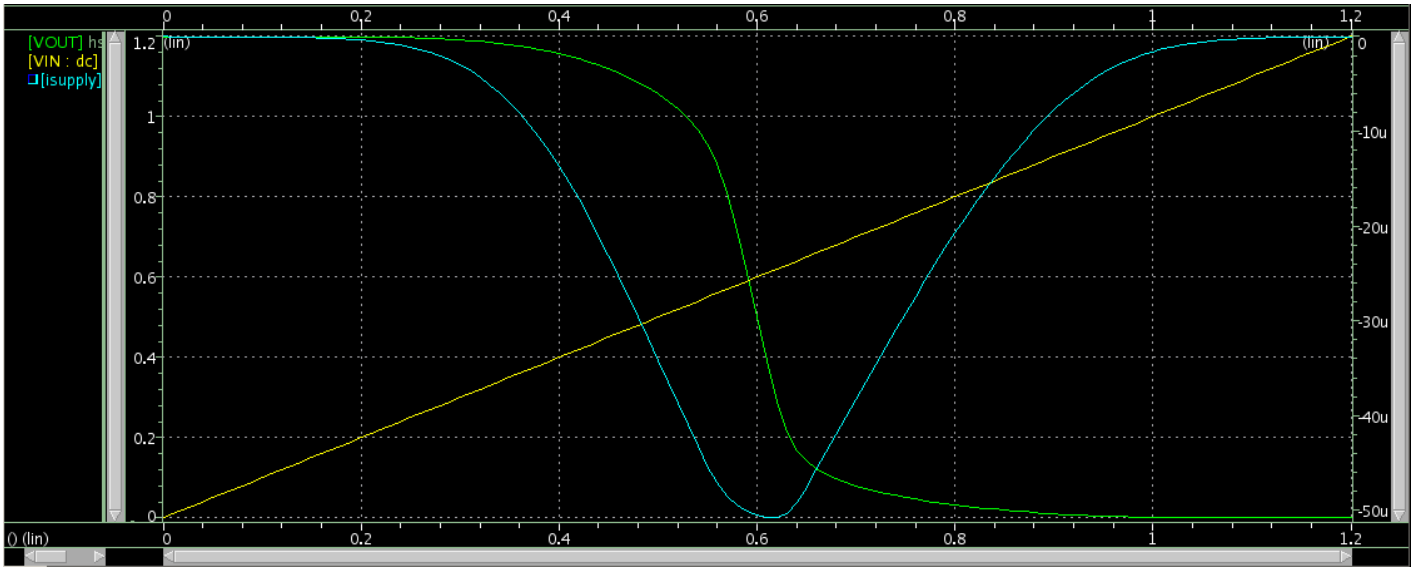
A test-bench for my inverter design



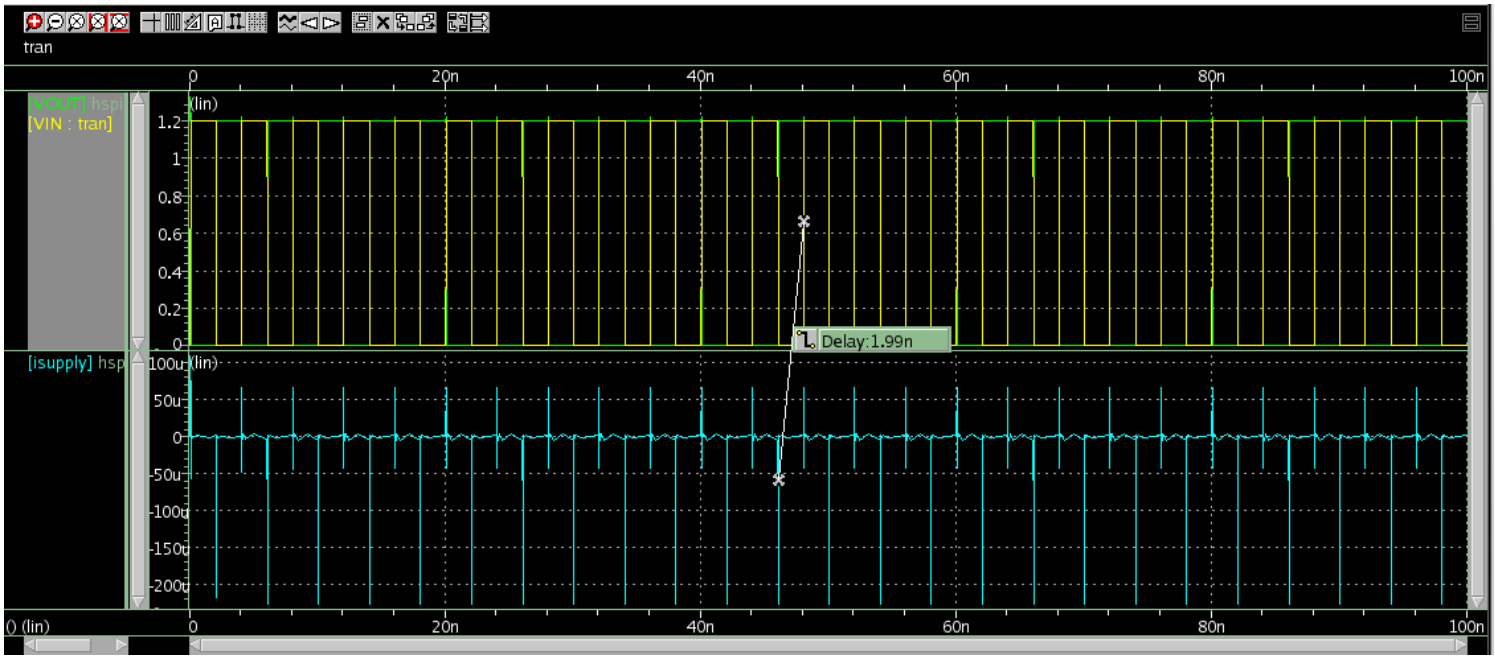
Transient analysis waveform



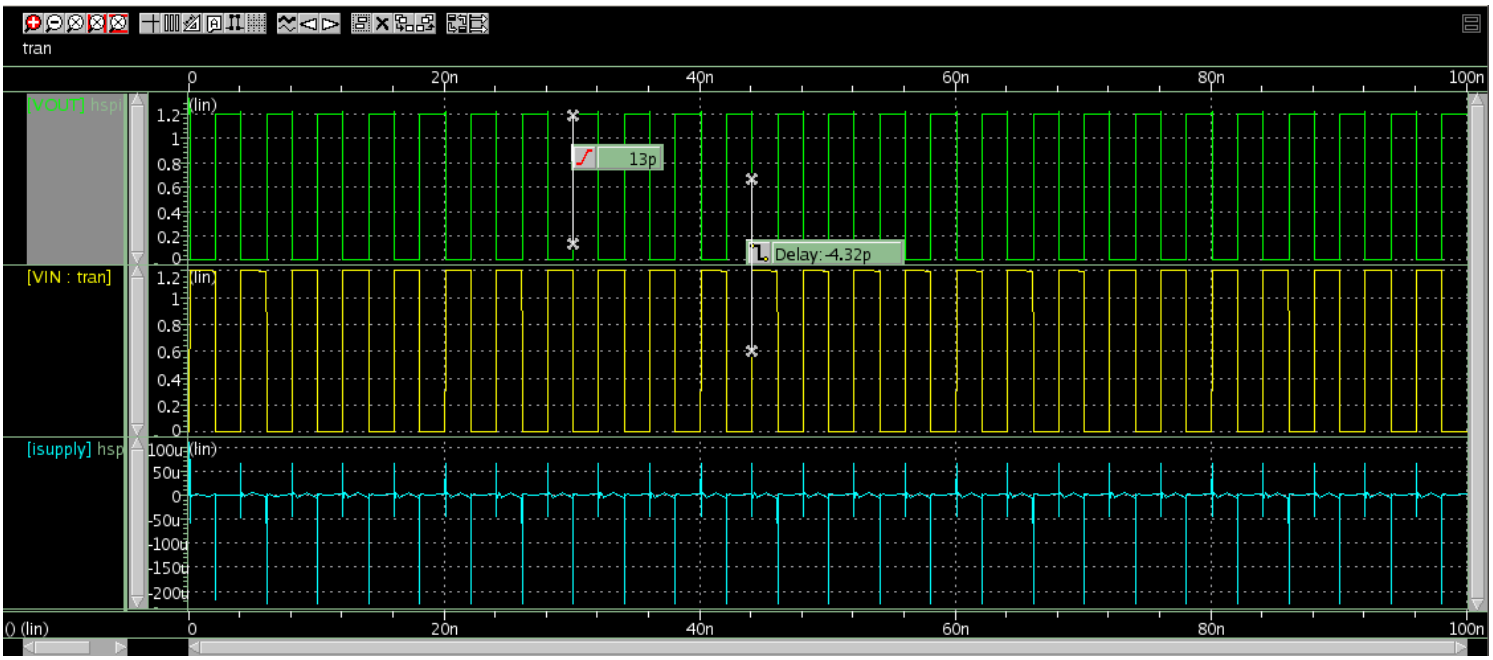
DC Sweep analysis waveform



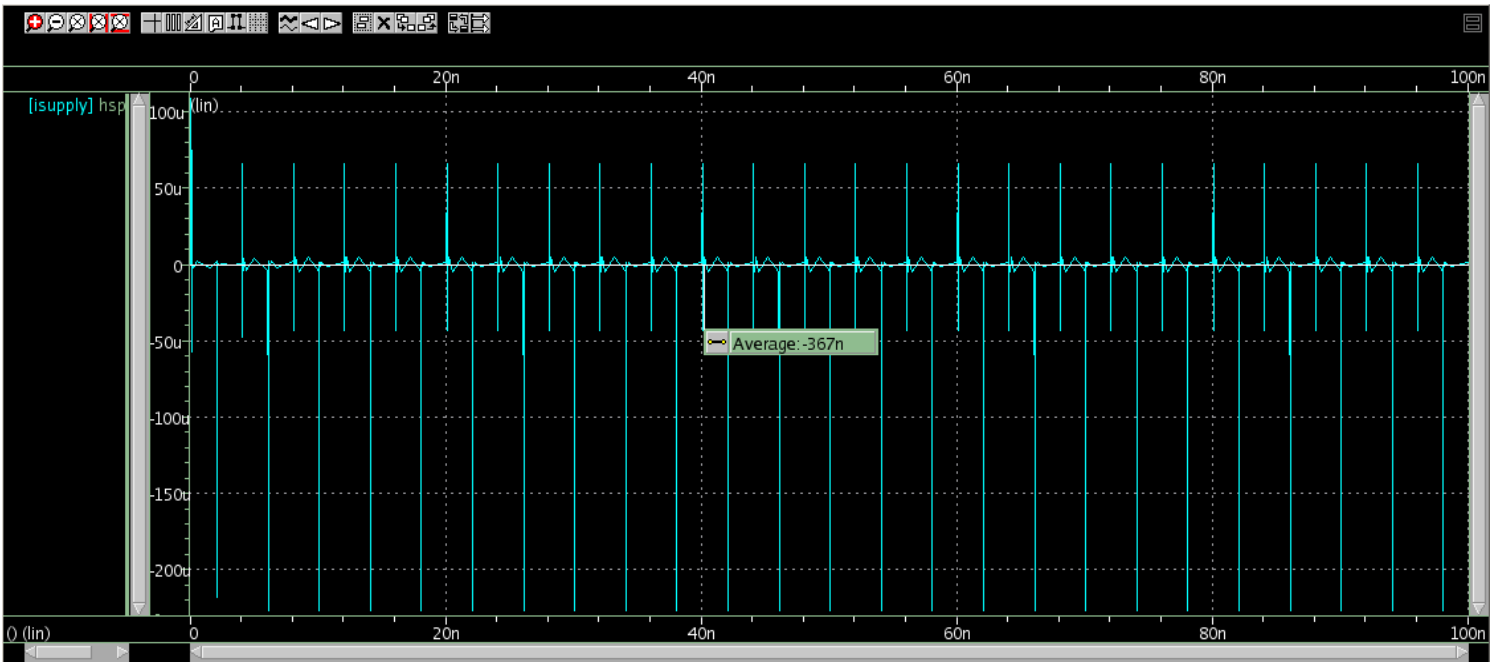
A delay measurement of VOUT and VIN at 50% to 50%



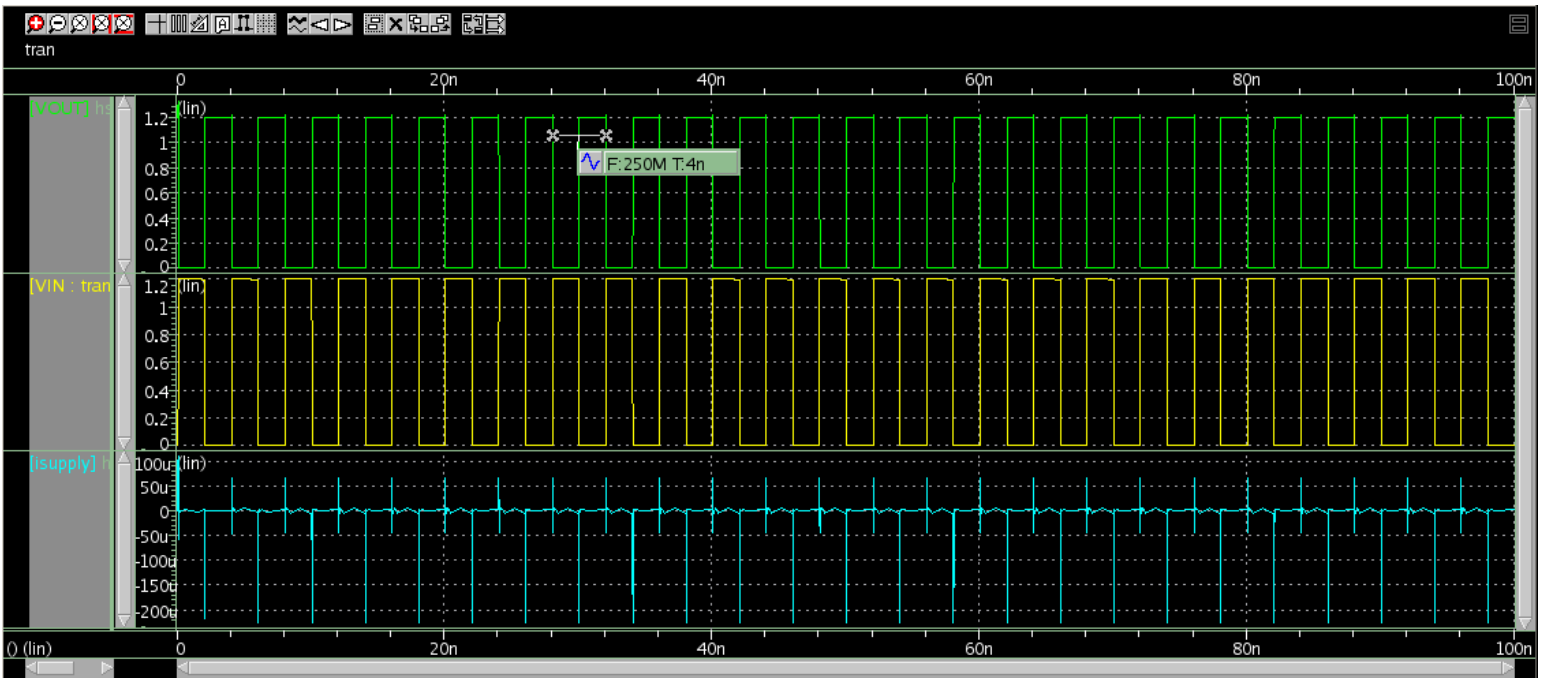
A rise AND fall measurement at 90% and 10% for VOUT



An average current measurement



A frequency measurement for VOUT



Issues

One of the main issues that I had in this lab was interacting with the pins in order to make sure that the type of pin was output. It was a weird error where even though I would label the pin as output, and set its type to output, the error would state that the pin is mismatched, which doesn't really make sense to me. Other than that, I had no major issues with the lab itself and was able to take measurements accordingly and apply what was requested in the lab, to my CDesigner and SAE.