EECS 168 Lab 4.2

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Lab 4, Week 2 CheckOff Video: 5 design compiler report (timing, power, area, reference, and resource), Final Layout in Figure 51

https://drive.google.com/file/d/1Im2hVrskMgWgcv2kAnpuDuLTJRq-gVX5/view?usp=sharing

Summary

_____In this part of the lab, I gained experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design. I also gained experience transforming a gate-level netlist into a placed and routed layout using Synopsys IC Compiler (ICC). ICC takes a synthesized gate-level netlist and a standard cell library as input, then produces layout as an output. This was done with a GCD design.

5 design compiler report (timing, power, area, reference, and resource):

dc_shell> report_timing -transition_time -nets -attributes -nosplit
Information: Updating design information... (UID-85)

****
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 1
        -transition_time
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Wed Mar 2 22:55:09 2022
****

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

Startpoint: GCDdpath0/A_reg_reg[4]
(rising edge-triggered flip-flop clocked by ideal_clock1)
Endpoint: GCDdpath0/A_reg_reg[9]
(rising edge-triggered flip-flop clocked by ideal_clock1)
Path Group: ideal_clock1
Path Type: max

Attributes:
d - dont_touch
u - dont_use
mo - map_only
so - size_only
i - ideal_net or ideal_network
inf - infeasible path

Point	Fanout	Trans	Incr	Path	Attributes
clock ideal_clock1 (rise edge)			0.00	0.00	
clock network delay (ideal)			0.00	0.00	
GCDdpath0/A_reg_reg[4]/CLK (DFFARX1)			0.00	0.00	0.00 r
GCDdpath0/A_reg_reg[4]/Q (DFFARX1)			0.04	0.24	0.24 f
result_bits_data[4] (net)	5		0.00	0.24 f	
U153/QN (NAND2X1)			0.04	0.03	0.28 r
n294 (net)	2		0.00	0.28 r	
U251/QN (INVX0)			0.03	0.03	0.31 f
n183 (net)	2		0.00	0.31 f	
U133/QN (NAND2X0)			0.06	0.04	0.35 r
n149 (net)	1		0.00	0.35 r	
U252/QN (NAND2X1)			0.05	0.04	0.39 f
n314 (net)	3		0.00	0.39 f	
U253/QN (NAND2X2)			0.03	0.02	0.41 r
n153 (net)	1		0.00	0.41 r	
U258/QN (NAND2X1)			0.03	0.03	0.44 f
n154 (net)	1		0.00	0.44 f	
U259/Q (AO21X1)			0.04	0.08	0.52 f
n227 (net)	4		0.00	0.52 f	
U177/Q (LSDNX1)			0.04	0.08	0.60 f
n308 (net)	2		0.00	0.60 f	
U320/Q (AO21X1)			0.03	0.09	0.69 f
n233 (net)	1		0.00	0.69 f	

```
  U322/Q (XOR2X1)                                 0.04      0.12       0.81 r
  n234 (net)                              1       0.00       0.81 r
  U140/QN (NAND2X0)                               0.05      0.04       0.84 f
  n238 (net)                              1       0.00       0.84 f
  U324/QN (NAND4X0)                               0.07      0.04       0.88 r
  n91 (net)                               1       0.00       0.88 r
  GCDdpath0/A_reg_reg[9]/D (DFFARX1)                        0.07       0.00       0.88 r
  data arrival time                                         0.88

  clock ideal_clock1 (rise edge)                          1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  GCDdpath0/A_reg_reg[9]/CLK (DFFARX1)                                0.00       1.00 r
  library setup time                                     -0.12       0.88
  data required time                                                 0.88
  ---------------------------------------------------------------------------------------------------
  data required time                                                 0.88
  data arrival time                                                 -0.88
  ---------------------------------------------------------------------------------------------------
  slack (MET)                                                        0.00


1
dc_shell> report_area -nosplit -hierarchy

****************************************
Report : area
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Wed Mar  2 22:57:52 2022
****************************************

Library(s) Used:

    saed90nm_typ (File:
/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/s
aed90nm_fr/LM/saed90nm_typ.db)

Number of ports:                 54
Number of nets:                 384
Number of cells:                317
```

```
Number of combinational cells:           283
Number of sequential cells:              34
Number of macros/black boxes:            0
Number of buf/inv:                       34
Number of references:                    30

Combinational area:            1995.864012
Buf/Inv area:                   199.999007
Noncombinational area:         1081.958015
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:               3077.822028
Total area:                 undefined

Hierarchical area distribution
------------------------------

                           Global cell area          Local cell area
                           ------------------  ----------------------------
Hierarchical cell                Absolute   Percent  Combi-     Noncombi-  Black-
                           Total      Total    national   national   boxes   Design
------------------------------  ---------  -------  ---------  ---------  ------  ---------
gcdGCDUnit_rtl                   3077.8220    100.0  1995.8640  1081.9580  0.0000
gcdGCDUnit_rtl
------------------------------  ---------  -------  ---------  ---------  ------  ---------
Total                                                1995.8640  1081.9580  0.0000

1
dc_shell> report_power -nosplit -hierarchy

****************************************
Report : power
        -hier
        -analysis_effort low
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Wed Mar  2 22:58:26 2022
****************************************
```

Library(s) Used:

    saed90nm_typ (File:
/usr/local/synopsys/pdk/SAED90_EDK/SAED_EDK90nm_REF/references/ChipTop/ref/saed90nm_fr/LM/saed90nm_typ.db)

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: top

Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW   (derived from V,C,T units)
    Leakage Power Units = 1pW

Hierarchy	Switch Power	Int Power	Leak Power	Total Power	%
gcdGCDUnit_rtl	0.128	1.124	9.51e+06	1.262	100.0

1
dc_shell> report_reference -nosplit -hierarchy

****
Report : reference
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date   : Wed Mar 2 22:58:37 2022
****

Attributes:
    b - black box (unknown)
   bo - allows boundary optimization
    d - dont_touch

mo - map_only
h - hierarchical
n - noncombinational
r - removable
s - synthetic operator
u - contains unmapped logic

Reference	Library	Unit Area	Count	Total Area	Attributes
AND2X1	saed90nm_typ	7.445000	1	7.445000	
AO21X1	saed90nm_typ	10.138000	2	20.275999	
AO222X1	saed90nm_typ	14.746000	16	235.936005	
AOINVX1	saed90nm_typ	6.451000	1	6.451000	
AOINVX2	saed90nm_typ	6.451000	1	6.451000	
DFFARX1	saed90nm_typ	32.256001	32	1032.192017	n
DFFX1	saed90nm_typ	24.882999	2	49.765999	n
INVX0	saed90nm_typ	5.530000	28	154.840006	
INVX2	saed90nm_typ	6.451000	1	6.451000	
INVX8	saed90nm_typ	14.746000	1	14.746000	
ISOLANDX1	saed90nm_typ	7.373000	1	7.373000	
ISOLORX1	saed90nm_typ	7.387000	4	29.548000	
LSDNX1	saed90nm_typ	5.530000	1	5.530000	
NAND2X0	saed90nm_typ	5.443000	88	478.983986	
NAND2X1	saed90nm_typ	5.501000	9	49.508999	
NAND2X2	saed90nm_typ	8.798000	4	35.192001	
NAND2X4	saed90nm_typ	14.501000	1	14.501000	
NAND3X0	saed90nm_typ	7.373000	2	14.746000	
NAND4X0	saed90nm_typ	8.294000	16	132.703995	
NBUFFX2	saed90nm_typ	5.530000	1	5.530000	
NOR2X0	saed90nm_typ	5.530000	71	392.630015	
NOR2X1	saed90nm_typ	6.005000	6	36.030001	
NOR2X2	saed90nm_typ	9.216000	2	18.431999	
NOR2X4	saed90nm_typ	14.731000	2	29.462000	
NOR3X0	saed90nm_typ	8.294000	1	8.294000	
OA21X1	saed90nm_typ	9.216000	5	46.079998	
OA22X1	saed90nm_typ	11.059000	1	11.059000	
OR4X1	saed90nm_typ	10.152000	2	20.304001	
XNOR2X1	saed90nm_typ	13.824000	8	110.592003	
XOR2X1	saed90nm_typ	13.824000	7	96.768003	

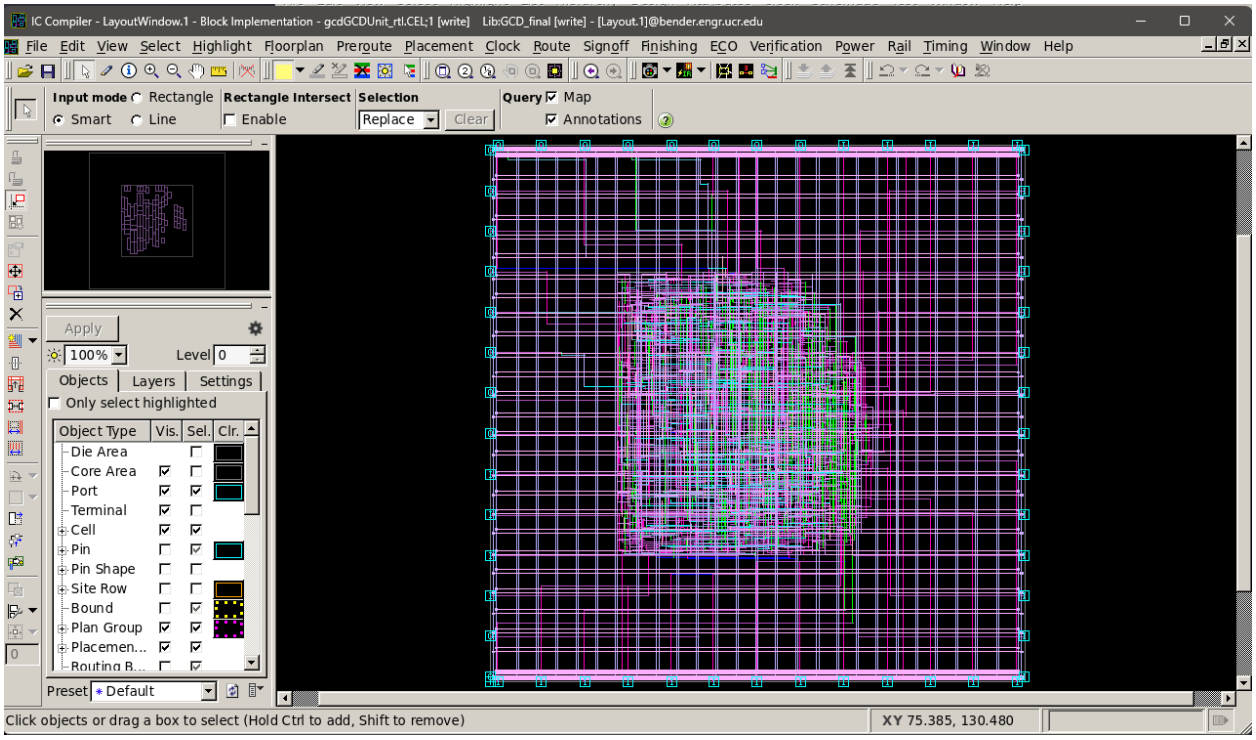
Total 30 references 3077.822028
1
dc_shell> report_resources -nosplit -hierarchy

****
Report : resources
Design : gcdGCDUnit_rtl
Version: K-2015.06-SP4
Date : Wed Mar 2 22:58:49 2022
****

Resource Report for this hierarchy in file ./gcd_dpath.v
==
==========
| Cell | Module | Parameters | Contained Operations |
==
==========
| sub_x_2 | DW01_sub | width=16 | GCDdpath0/sub_45 (gcd_dpath.v:45) |
| lt_x_3 | DW_cmp | width=16 | GCDdpath0/lt_51 (gcd_dpath.v:51) |
==
==========

Implementation Report
==
=============
| | | Current | Set |
| Cell | Module | Implementation | Implementation |
==
=============
| sub_x_2 | DW01_sub | pparch (area,speed) | |
| lt_x_3 | DW_cmp | pparch (area,speed) | |
==
=============

Final Layout in Figure 51:



Issues

This lab was fine and I was able to run it without errors.