EECS 168 Lab 2

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Session 21
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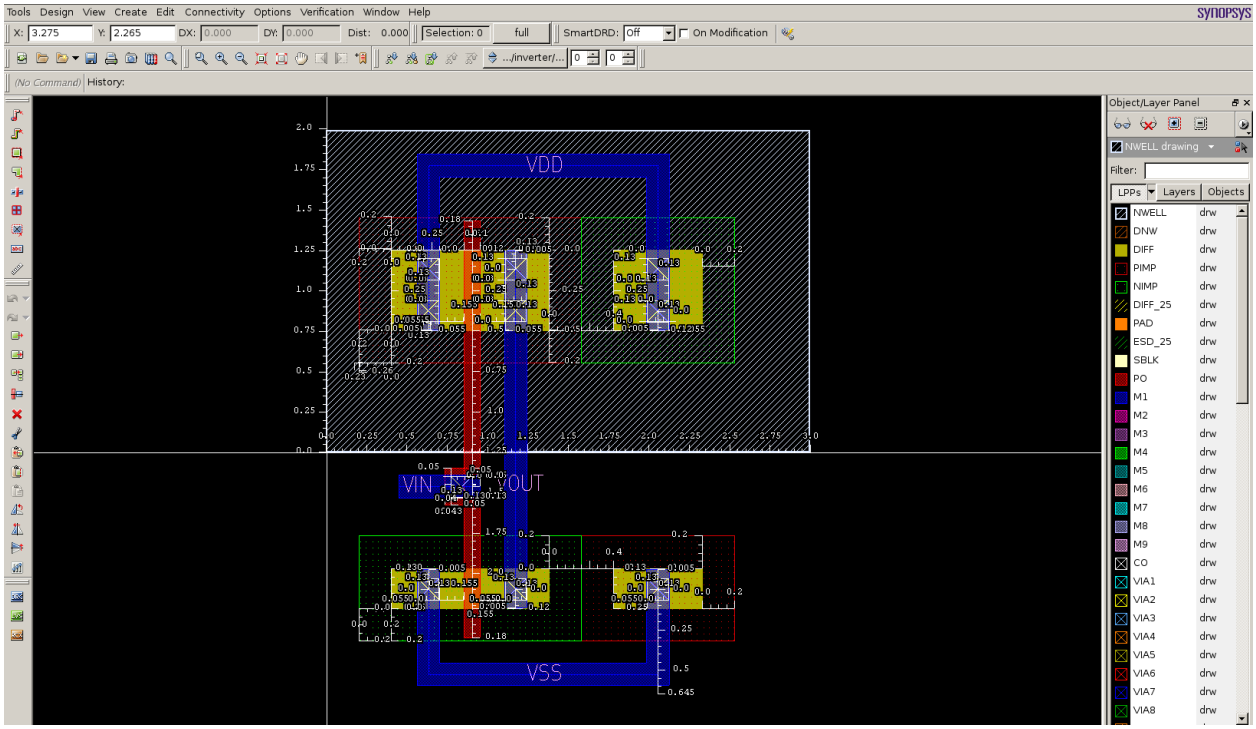
Inverter Layout, DRC, LVS Video Link:
https://drive.google.com/file/d/15eMFVOJNr17o5rEyTA2176RGB9NddJb-/view?usp=sharing

NAND gate schematic, testbench, layout, DRC and LVS video link:
https://drive.google.com/file/d/15dhsLMdNzgPM7tAWxyDI2-ooGXjE2SNG/view?usp=sharing

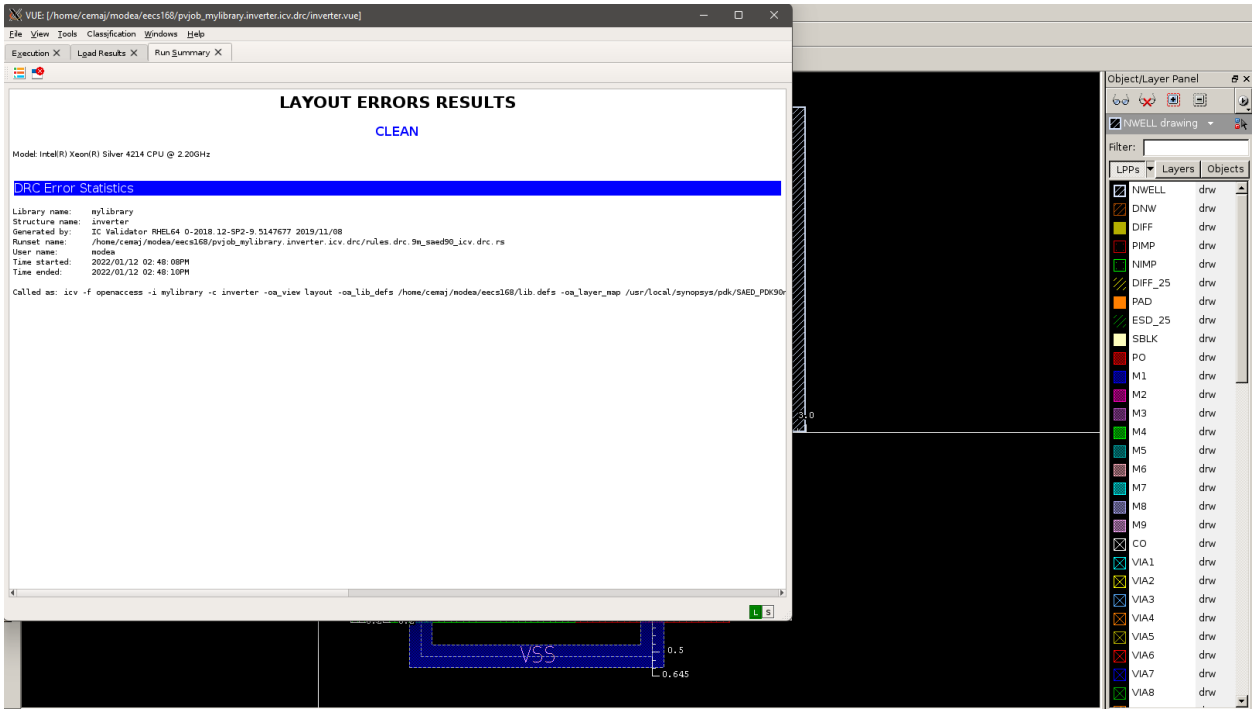
Summary

_____In this lab, I learned how to design layouts, and validate with DRC and LVS tests. I also learned three IC design tools (Custom Designer, IP Validator) and I also designed both inverter and NAND gates. There were also many layers and tools within the layout part of the lab that I had to familiarize myself with by constructing the inverter layout, and then using my knowledge to build a NAND layout. I also learned how to test the layouts with both the DRC and LVS tests. The many parameters and different tools that I used enabled me to build an almost successful NAND gate, however I ran into an unexplainable error that I unfortunately wasn't able to solve..

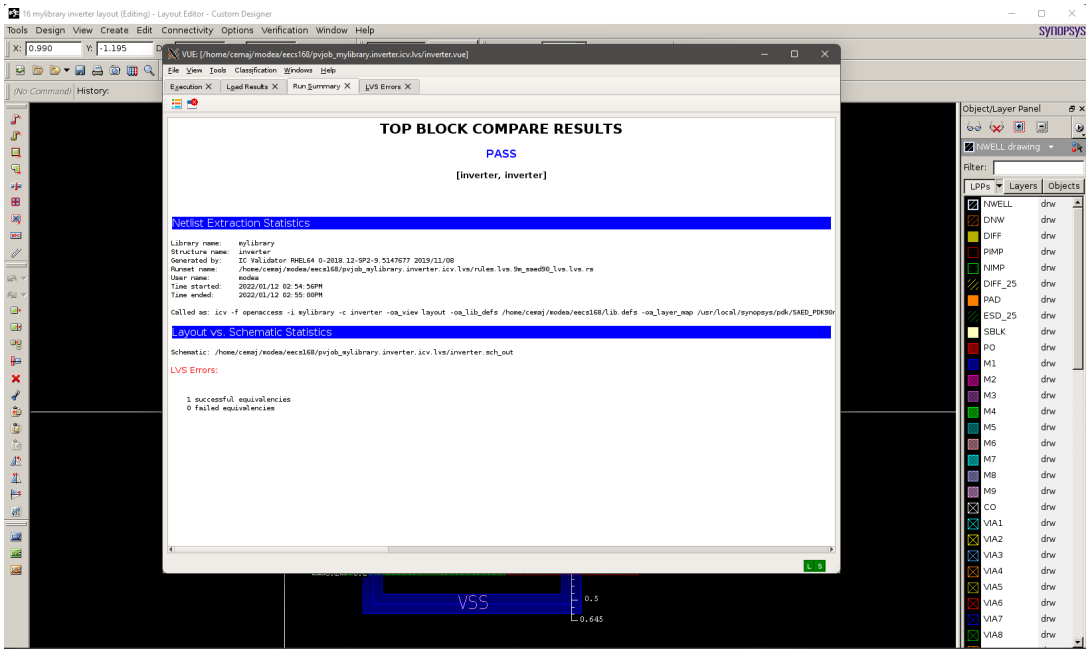
Inverter Layout



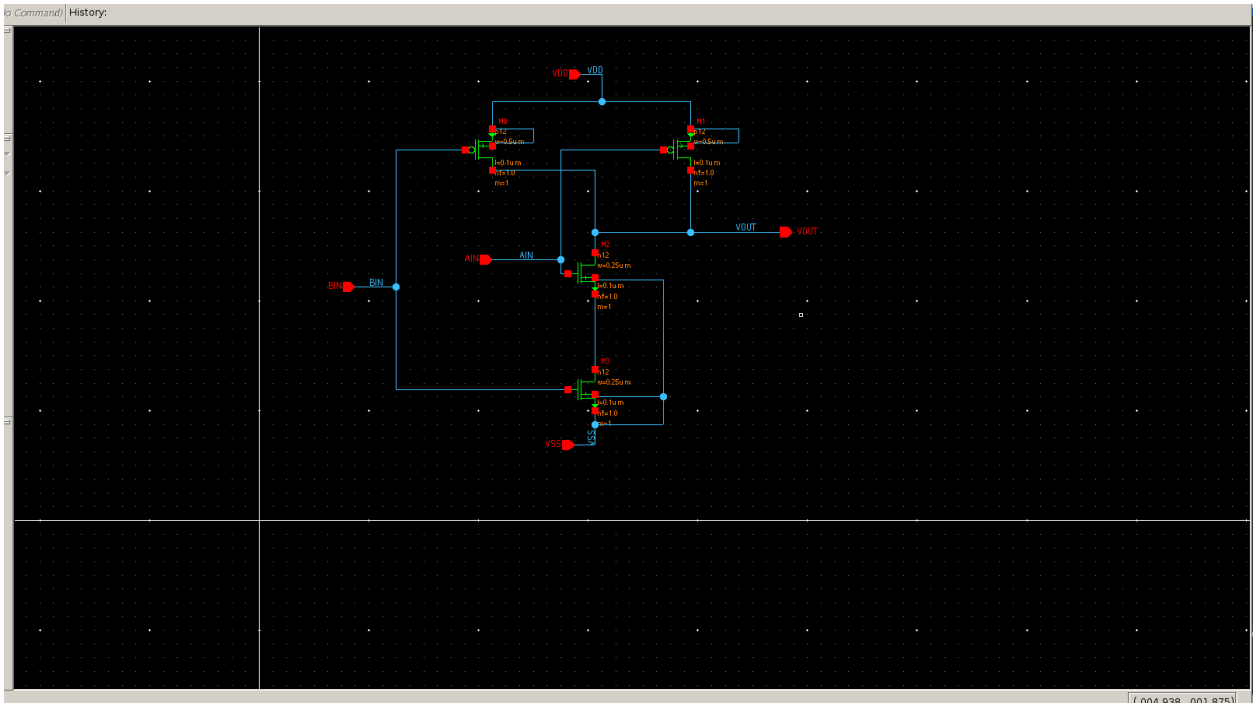
A DRC Result with CLEAN for inverter layout



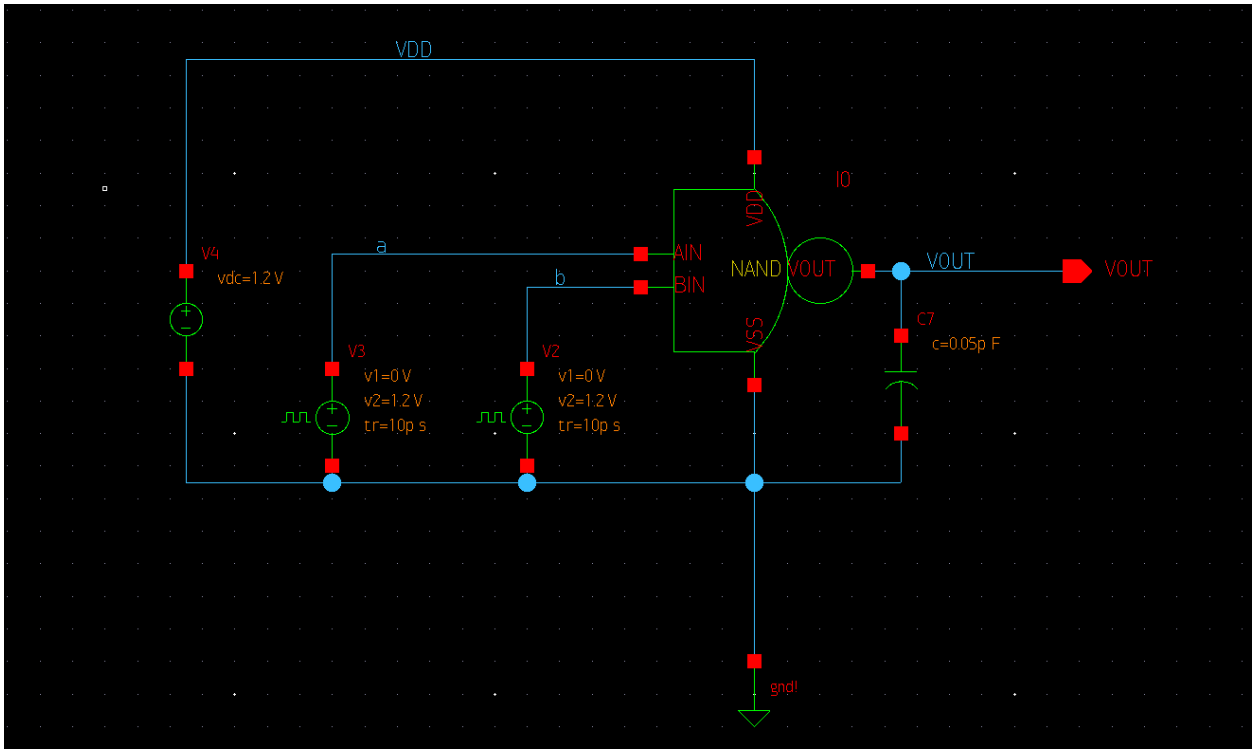
A LVS Result with PASS for inverter layout



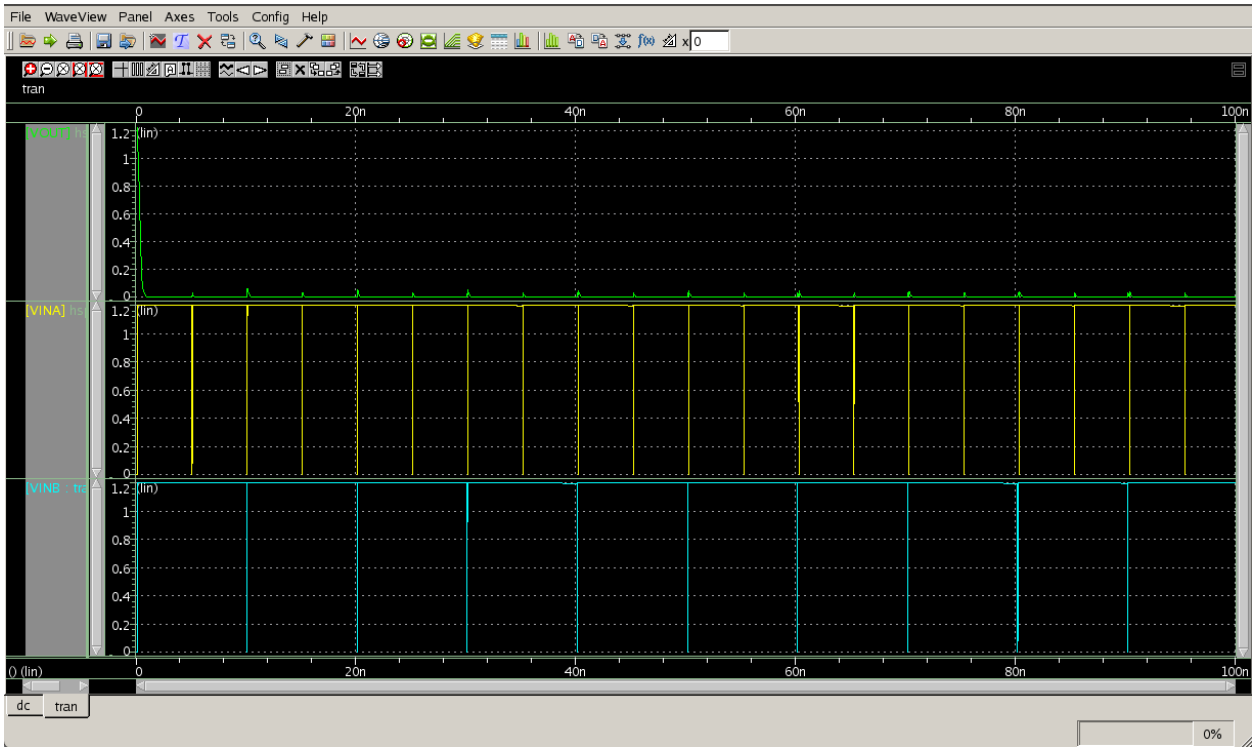
NAND gate schematic



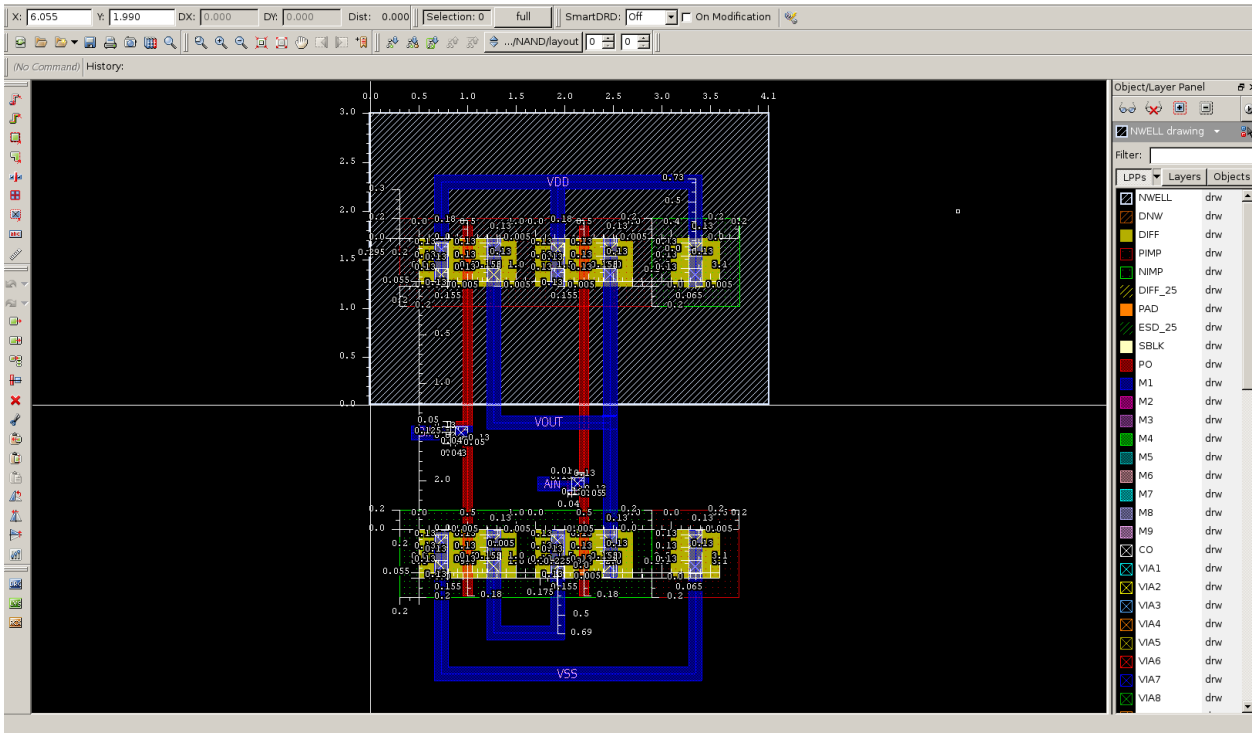
NAND gate test bench schematic



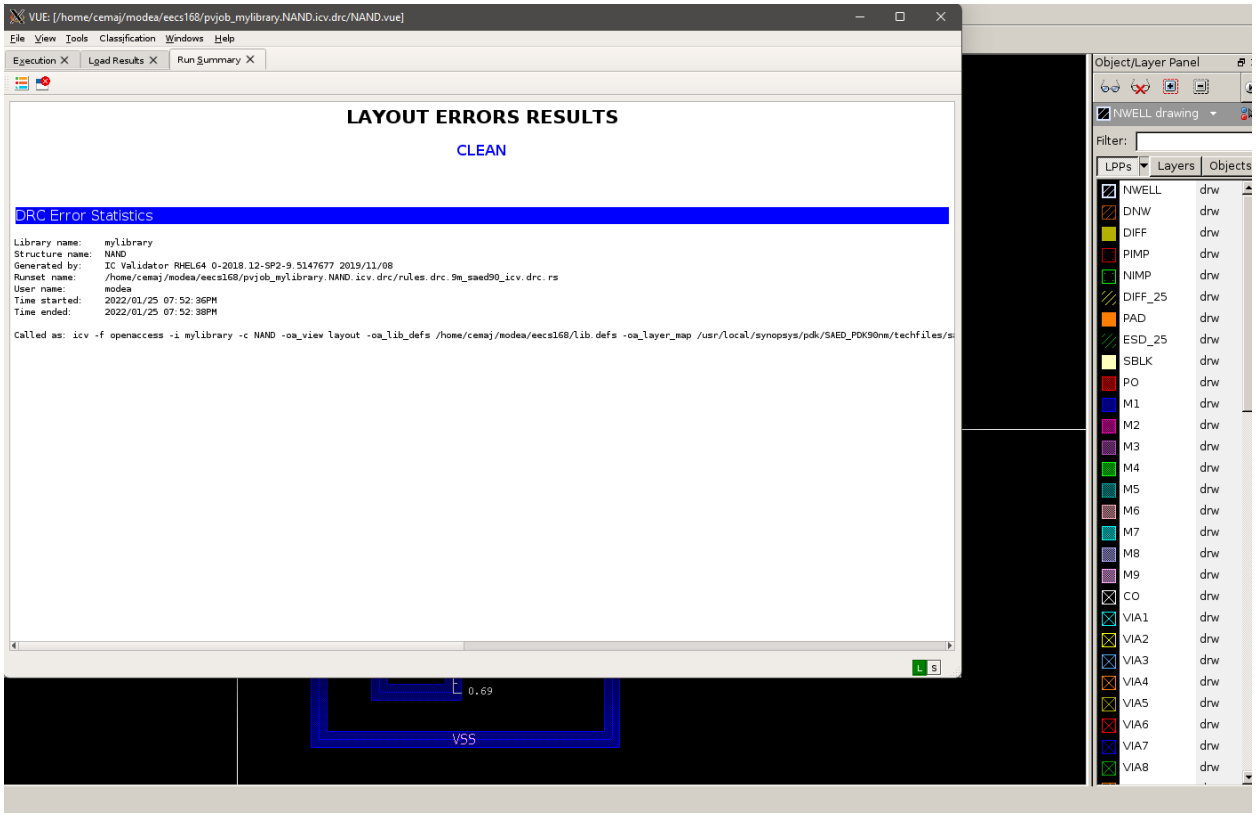
Waveform View result



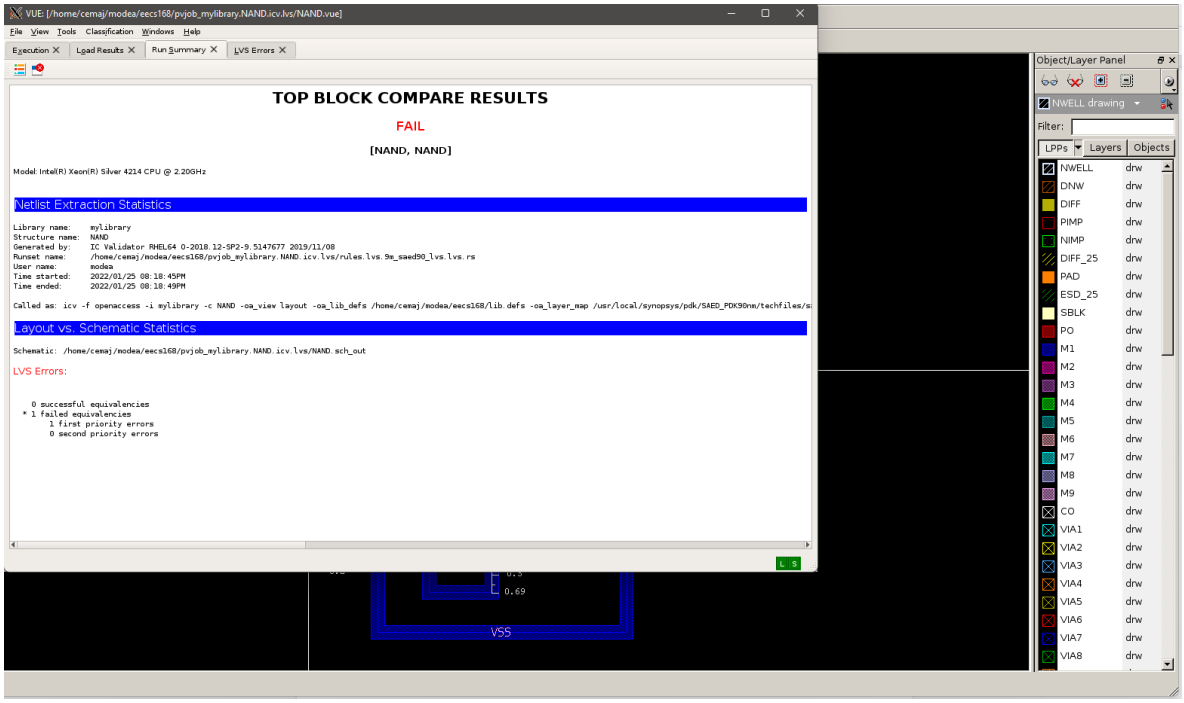
NAND gate layout

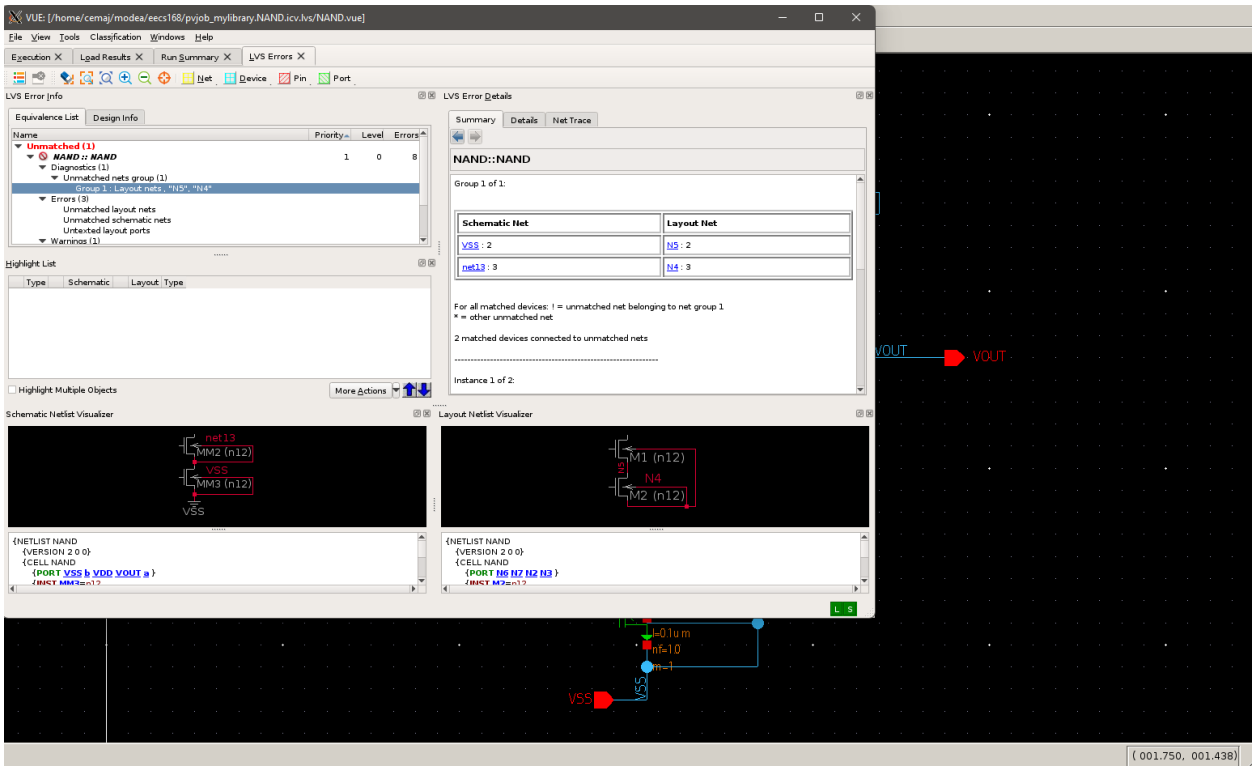


An DRC Result with CLEAN for NAND gate layout



An LVS Result with PASS for NAND gate layout





Issues

There were two main issues that I had with this lab, that unfortunately, I wasn't able to solve and figure out what was causing the errors after basically running trial and error on the program. The first main issue was that while my testbench and schematic for my NAND gate was accurate, at least according to me and basing it off of lab 1, I ended up getting a different waveform than what was requested in the lab manual. I double and triple checked my values and measurements, but couldn't figure out what was causing the issue.

The second main issue I had was with the LVS Test for the NAND gate. I knew that the layout was accurate, as well as my schematic, however I kept getting this weird error about how terminals were misnamed, even though they were named the same name. I tried different variations of the schematic, yet kept running into this problem unfortunately.