EECS 168 Lab 3.2-3.3

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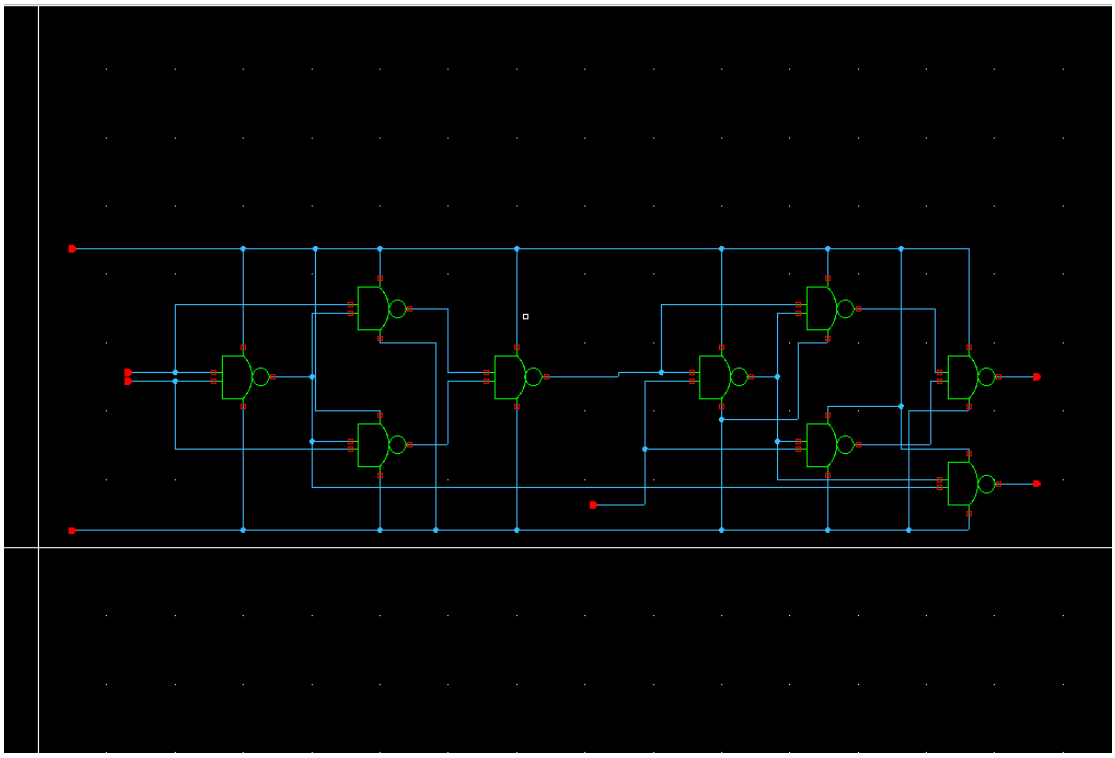
Lab 3, Week 2 CheckOff Video: 1-bit full adder schematic, simulation, stick diagram, layout, DRC, LVS, POST (Layout) SIMULATION result (with parasitic extraction)

https://drive.google.com/file/d/1Ec1Sx9iluLtDPyDzbe4azfeytAjzthcr/view?usp=sharing

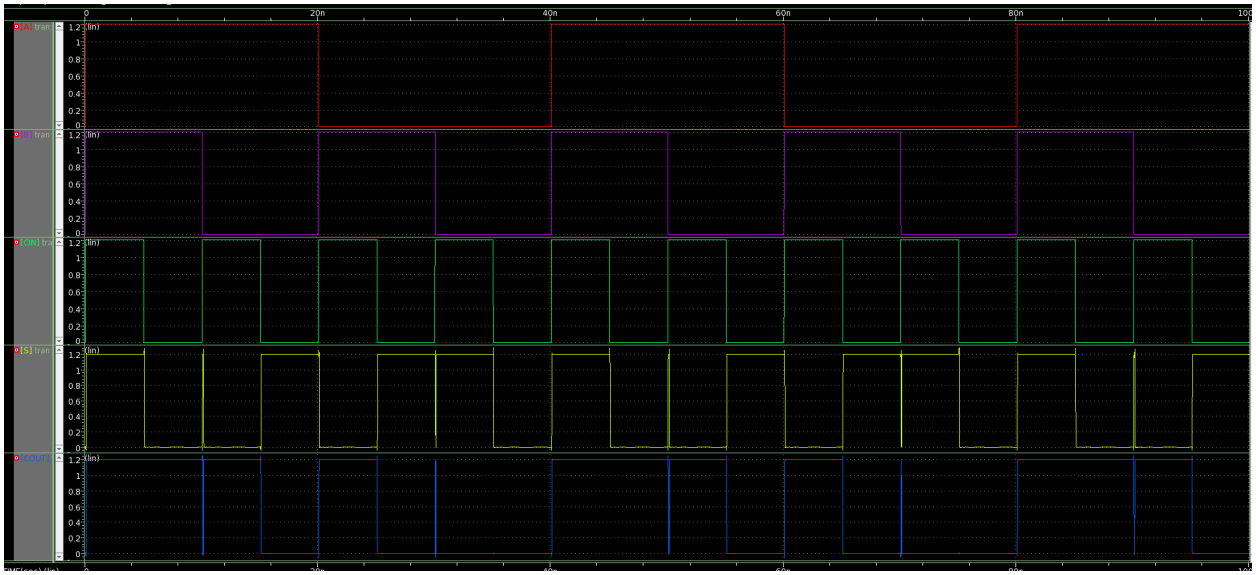
Summary

_____In this part of the lab, I learned how to do parasitic extraction/ post layout simulation and hierarchical design for 1 bit and 4 bit adders. I used my inverter design for my first parasitic extraction and post layout simulation. For my hierarchical designs, I designed a 1 bit adder and a 4 bit adder that was able to pass all three tests, LVS, LPE, and DVR. During these two weeks, I also familiarized myself with the new interface since the system got updated last week and it is a massive improvement from the previous system. It was a lot easier and simpler for me to access the tools and functions, and it also allowed me to fix the LVS from lab 2 for my NAND gate.

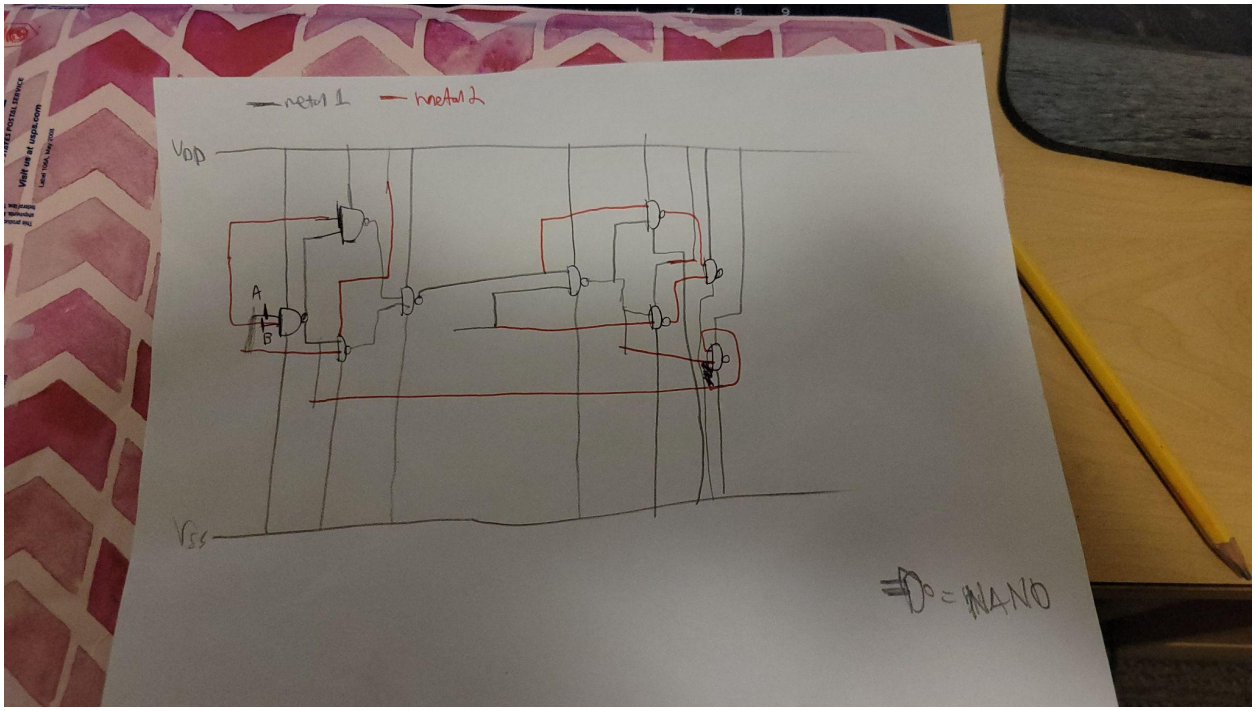
1-bit full adder schematic



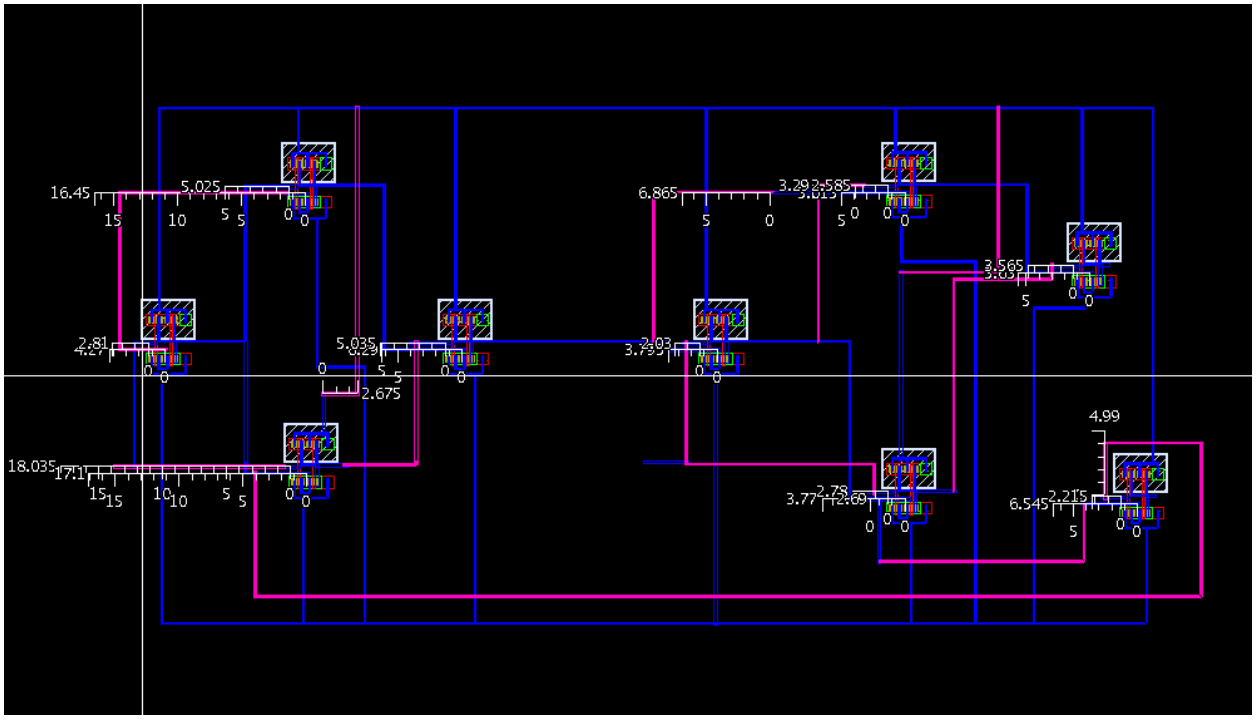
1-bit full adder simulation



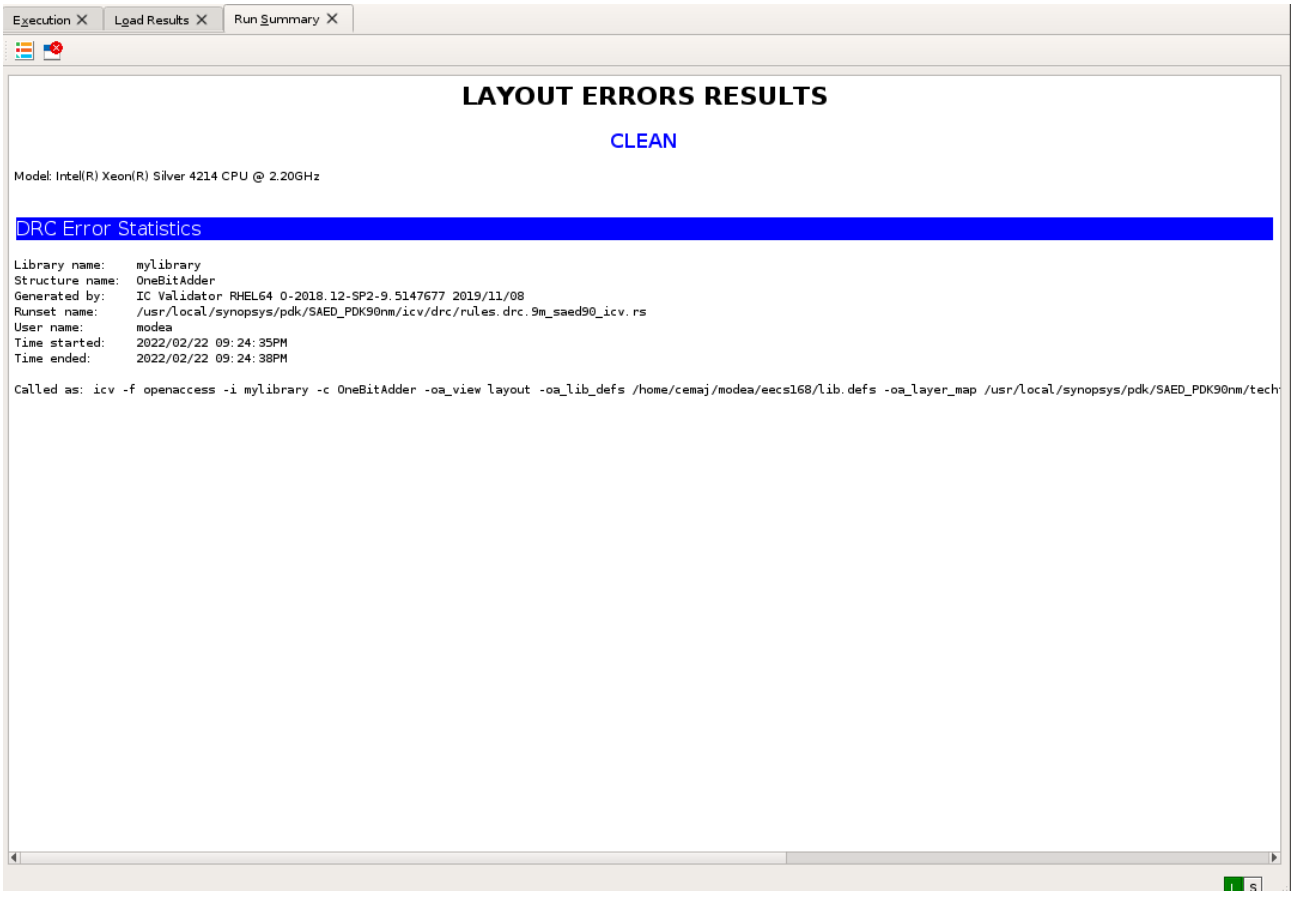
1-bit full adder stick diagram



1-bit full adder layout



An DRC Result with CLEAN for your 1-bit full adder



An LVS Result with PASS for your 1-bit full adder

TOP BLOCK COMPARE RESULTS

PASS

[OneBitAdder, OneBitAdder]

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

Netlist Extraction Statistics

```
Library name:     mylibrary
Structure name:   OneBitAdder
Generated by:     IC Validator RHEL64 O-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /usr/local/synopsys/pdk/SAED_PDK90nm/icv/lvs/rules.lvs.9m_saed90_lvs.rs
User name:        modea
Time started:     2022/02/22 09:25:13PM
Time ended:       2022/02/22 09:25:18PM

Called as: icv -f openaccess -i mylibrary -c OneBitAdder -oa_view layout -oa_lib_defs /home/cemaj/modea/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDK90nm/tech
```

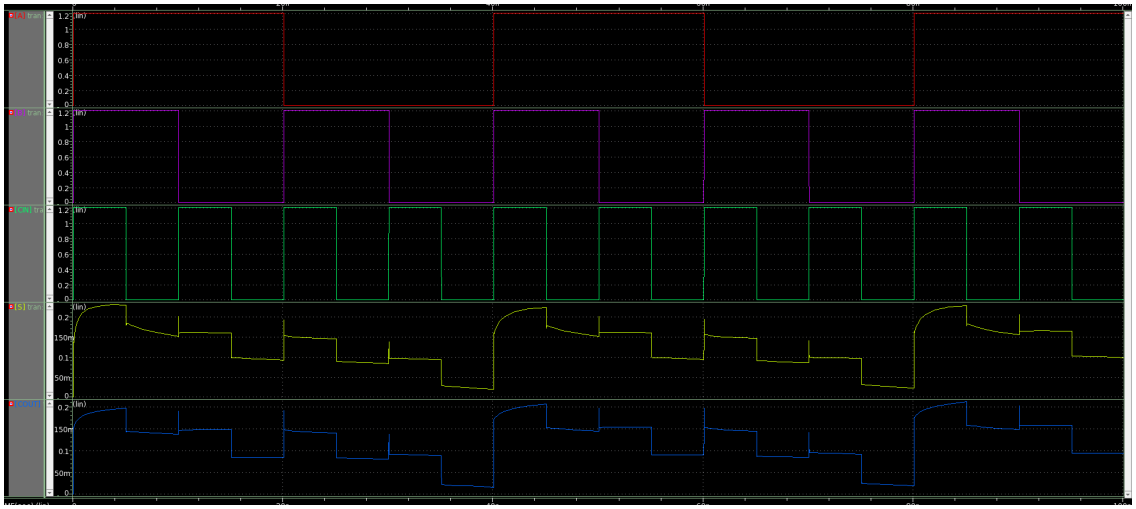
Layout vs. Schematic Statistics

```
Schematic:  /home/cemaj/modea/eecs168/synopsys_custom/pvjob_mylibrary.OneBitAdder.icv.lvs/OneBitAdder.sch_out
```

LVS Errors:

```
    1 successful equivalencies
    0 failed equivalencies
```

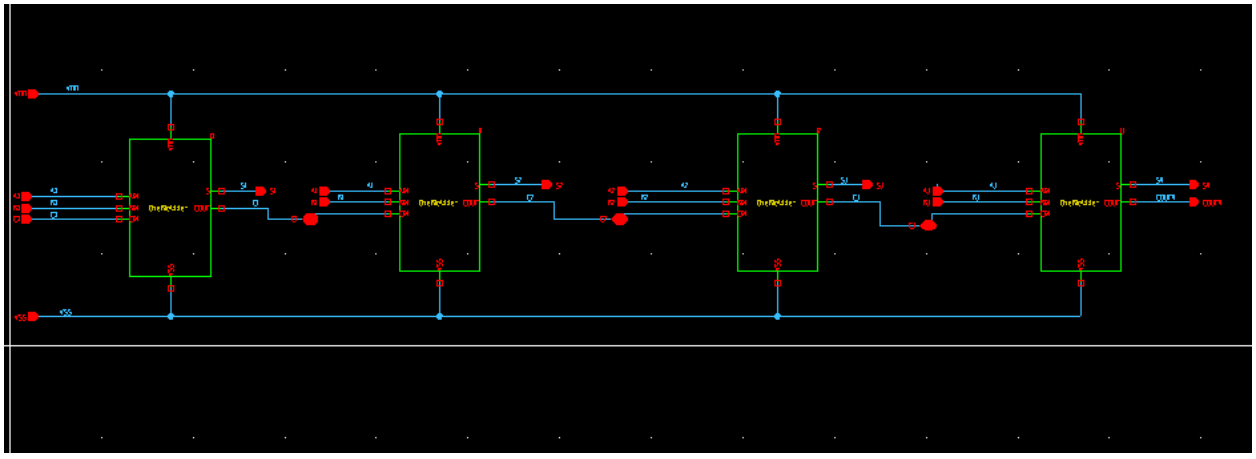
POST (Layout) SIMULATION result (with parasitic extraction)



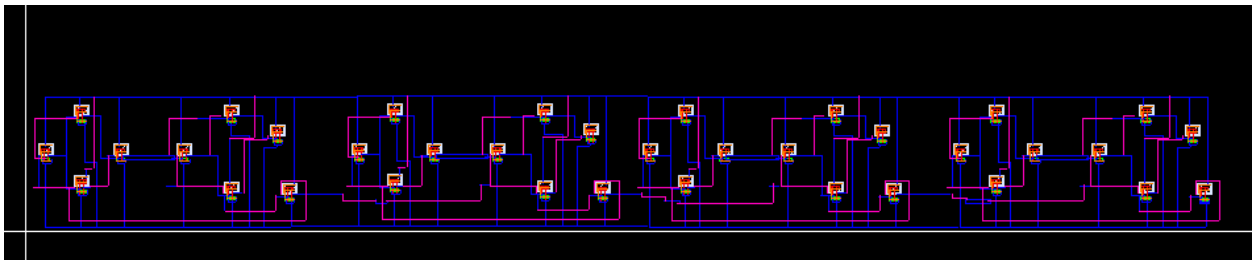
Lab 3, Week 3 CheckOff Video: 4-bit full adder schematic, 4-bit full adder layout, DRC, LVS, 4-bit full adder PRE (Schematic) SIMULATION, 4-bit full adder POST (Layout) SIMULATION:

https://drive.google.com/file/d/1EuPVgreREUX2GFGGCCEO31dzwi2i89wU/view?usp=sharing

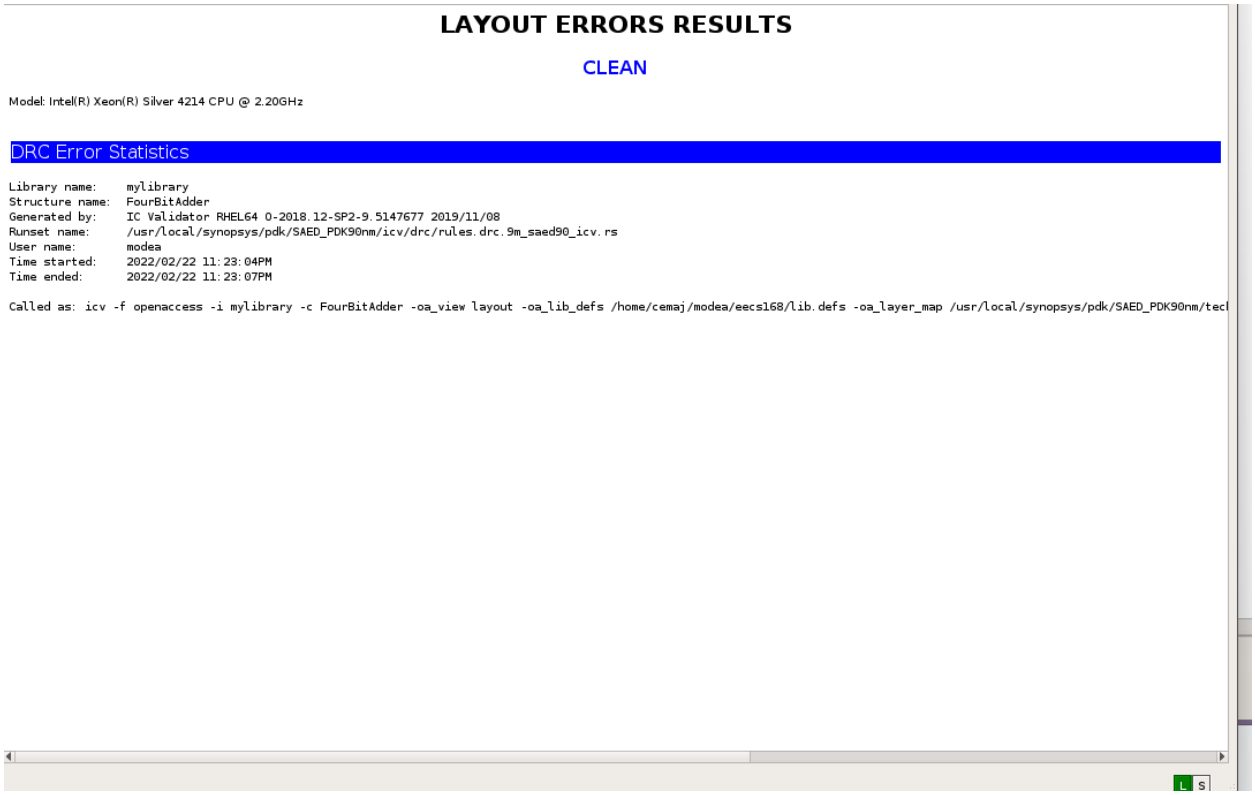
4-bit full adder schematic



4-bit full adder layout



DRC



LAYOUT ERRORS RESULTS

CLEAN

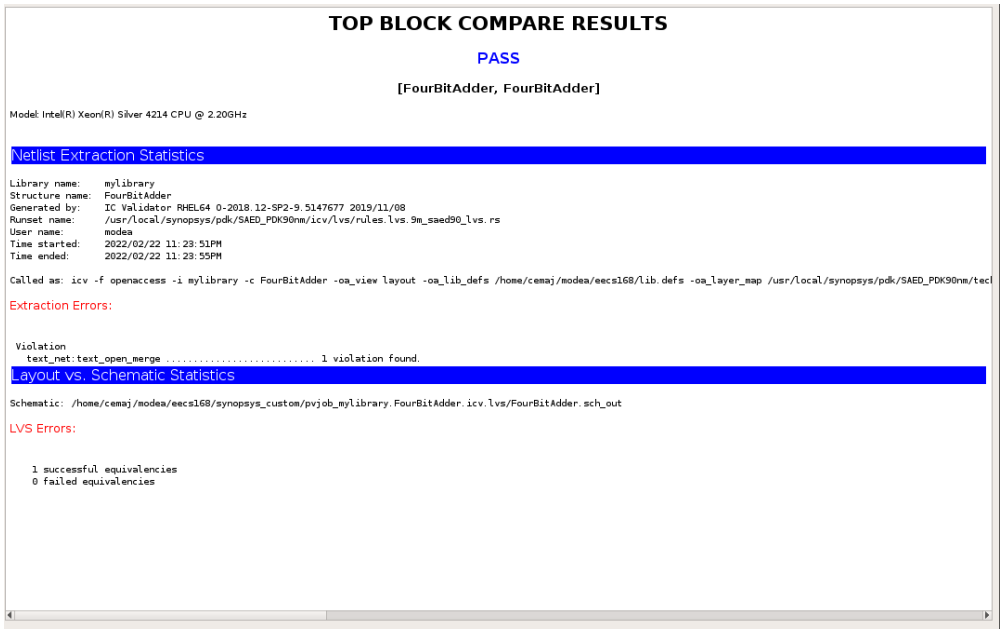
Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

DRC Error Statistics

```
Library name:     mylibrary
Structure name:   FourBitAdder
Generated by:     IC Validator RHEL64 O-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /usr/local/synopsys/pdk/SAED_PDK90nm/icv/drc/rules.drc.9m_saed90_icv.rs
User name:        modea
Time started:     2022/02/22 11:23:04PM
Time ended:       2022/02/22 11:23:07PM

Called as: icv -f openaccess -i mylibrary -c FourBitAdder -oa_view layout -oa_lib_defs /home/cemaj/modea/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDK90nm/tecl
```

LVS



TOP BLOCK COMPARE RESULTS

PASS

[FourBitAdder, FourBitAdder]

Model: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz

Netlist Extraction Statistics

```
Library name:     mylibrary
Structure name:   FourBitAdder
Generated by:     IC Validator RHEL64 O-2018.12-SP2-9.5147677 2019/11/08
Runset name:      /usr/local/synopsys/pdk/SAED_PDK90nm/icv/lvs/rules.lvs.9m_saed90_lvs.rs
User name:        modea
Time started:     2022/02/22 11:23:51PM
Time ended:       2022/02/22 11:23:55PM

Called as: icv -f openaccess -i mylibrary -c FourBitAdder -oa_view layout -oa_lib_defs /home/cemaj/modea/eecs168/lib.defs -oa_layer_map /usr/local/synopsys/pdk/SAED_PDK90nm/tecl
```

Extraction Errors:

```
 Violation
   text_net:text_open_merge ........................... 1 violation found.
```

Layout vs. Schematic Statistics

```
Schematic:  /home/cemaj/modea/eecs168/synopsys_custom/pvjob_mylibrary.FourBitAdder.icv.lvs/FourBitAdder.sch_out
```

LVS Errors:

```
    1 successful equivalencies
    0 failed equivalencies
```

4-bit full adder PRE (Schematic) SIMULATION

```
****** HSPICE -- K-2015.06-SP2 linux64 (Nov 18 2015) ******
 Input File:
 lic:
 lic: FLEXlm: v11.2.1
 lic: USER:   modea               HOSTNAME: bender.engr.ucr.edu
 lic: HOSTID: "f402709b4529"      PID:      38935
 lic: Using FLEXlm license file:
 lic: 27000@synopsys.engr.ucr.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 26-jan-2024/2021.09
 lic: 1(in_use)/50(total) FLOATING license(s) on SERVER 27000@synopsys.engr.ucr.edu
 lic:
 init: begin read circuit files,  cpu clock=  5.00E-02
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ad
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ad
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/behave
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/bjt
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/burr_brn
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/comlinear
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/dio
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/fet
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/lin_tech
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/pci
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/signet
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ti
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/tline
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/xilinx
       option runlvl
       option parhier = local
       option runlvl =     3.00
       option wdf =     1.00
       option opfile =     1.00
       option split_dp =     1.00
       option probe =     1.00
 init: end read circuit files,  cpu clock=  6.00E-02 peak memory=       191 mb
 init: begin check errors,  cpu clock=  6.00E-02
```

4-bit full adder POST (Layout) SIMULATION

```
****** HSPICE -- K-2015.06-SP2 linux64 (Nov 18 2015) ******
 Input File:
 lic:
 lic: FLEXlm: v11.2.1
 lic: USER:   modea                HOSTNAME: bender.engr.ucr.edu
 lic: HOSTID: "f402709b4529"       PID:      40075
 lic: Using FLEXlm license file:
 lic: 27000@synopsys.engr.ucr.edu
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 26-jan-2024/2021.09
 lic: 1(in_use)/50(total) FLOATING license(s) on SERVER 27000@synopsys.engr.ucr.edu
 lic:
 init: begin read circuit files,  cpu clock=  2.30E-01
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ad
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ad
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/behave
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/bjt
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/burr_brn
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/comlinear
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/dio
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/fet
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/lin_tech
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/pci
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/signet
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/ti
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/tline
       option search = /usr/local/synopsys/hspice/K-2015.06-SP2/hspice/
                       parts/xilinx
       option runlvl
       option parhier = local
       option runlvl =     3.00
       option wdf =     1.00
       option opfile =     1.00
       option split_dp =     1.00
       option probe =     1.00
 init: end read circuit files,  cpu clock=  2.60E-01 peak memory=       196 mb
 init: begin check errors,  cpu clock=  2.60E-01
```

Issues

The only main hard issue that I had was running Primewave simulation on my 4 bit adder pre and post parasitic testbenches. I made sure to set up everything according to the new setup and yet it still didn't function at all. I did however manage to get the output for the 1 bit adder pre and post parasitic extraction, and when I compared the two testbenches, they were almost identical in setup. I passed all DRC, LVS, and LPE tests with both 1 bit adder and 4 bit full adder.