EECS 168 Lab 3

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Session 21
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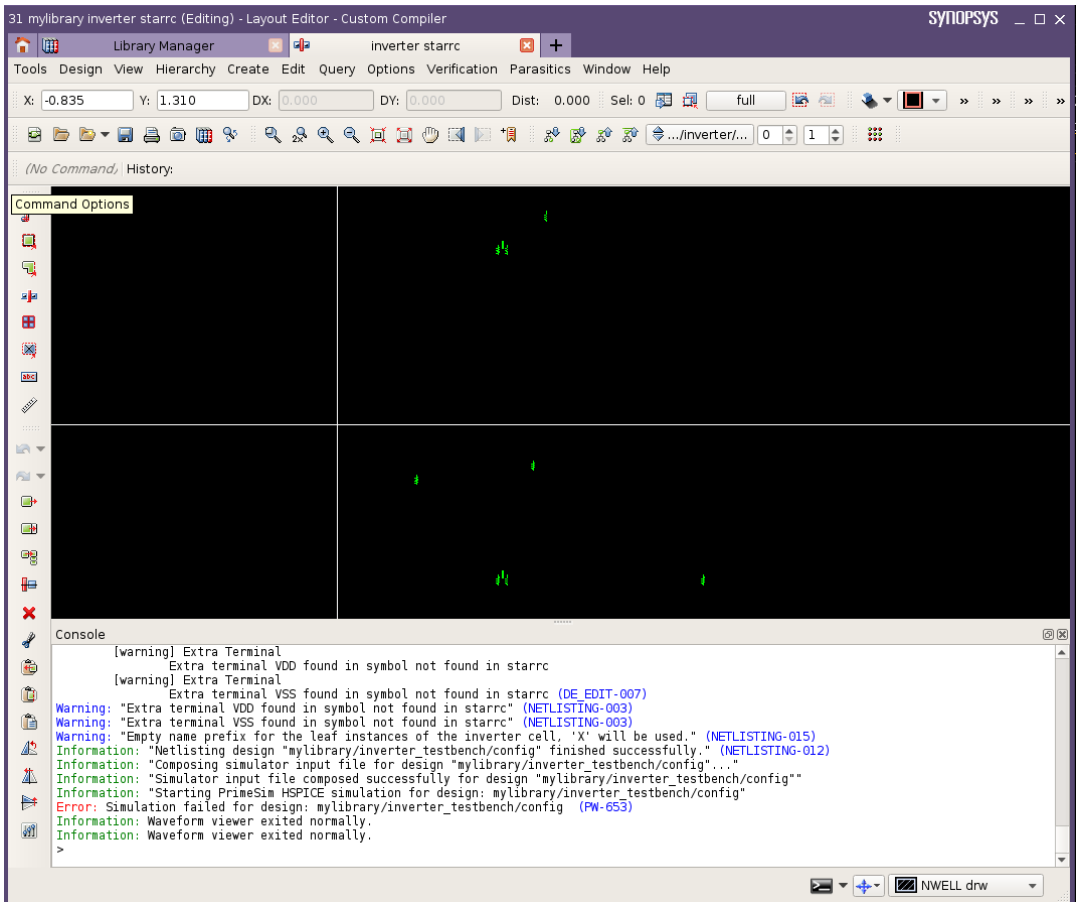
Lab 3, Week 1 CheckOff Video: Inverter parasitic, post simulation, ring oscillator:

https://drive.google.com/file/d/17uZKMZ2BthNiT_U3Akk1xZRf1WYD21TN/view?usp=sharing

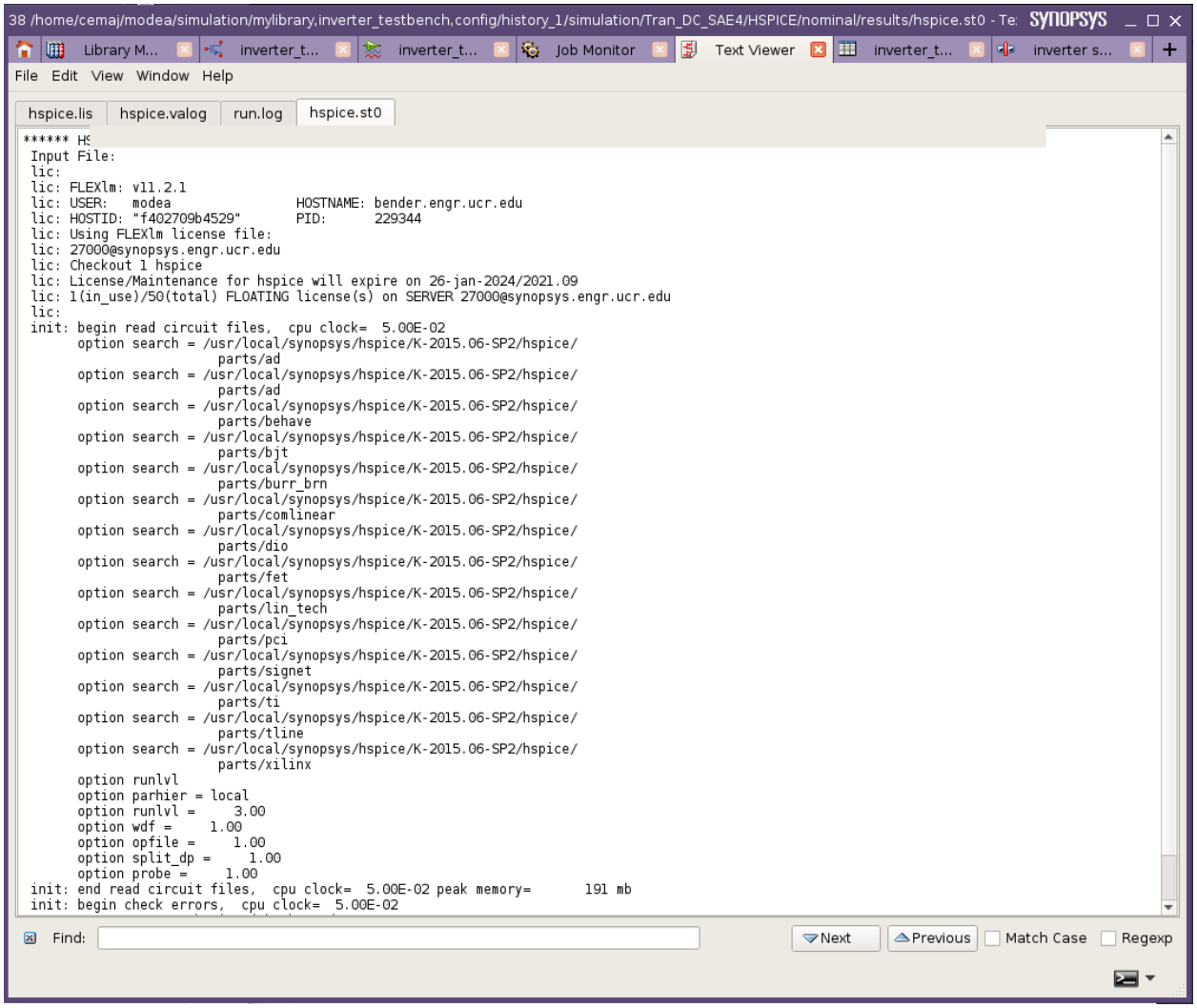
Summary

_____In this lab, I learned how to do parasitic extraction/ post layout simulation and hierarchical design. I used my inverter design for my first parasitic extraction and post layout simulation. For my hierarchical design, I designed a Ring Oscillator that was able to pass all three tests, LVS, LPE, and DVR. During this week, I also familiarized myself with the new interface since the system got updated last week and it is a massive improvement from the previous system. It was a lot easier and simpler for me to access the tools and functions, and it also allowed me to fix the LVS from lab 2 for my NAND gate.

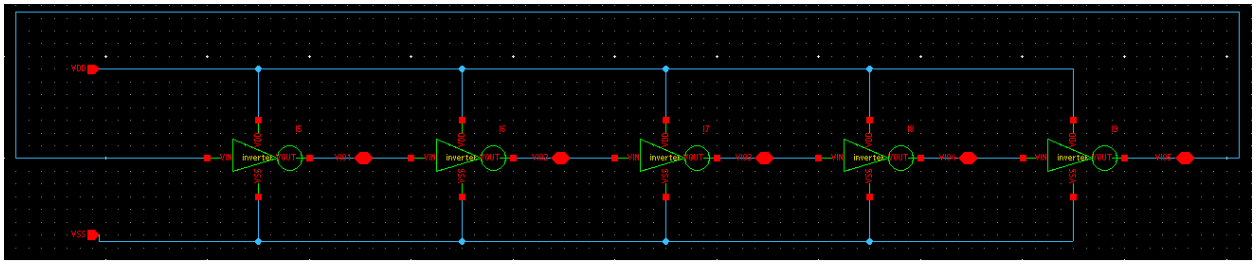
Inverter Parasitic



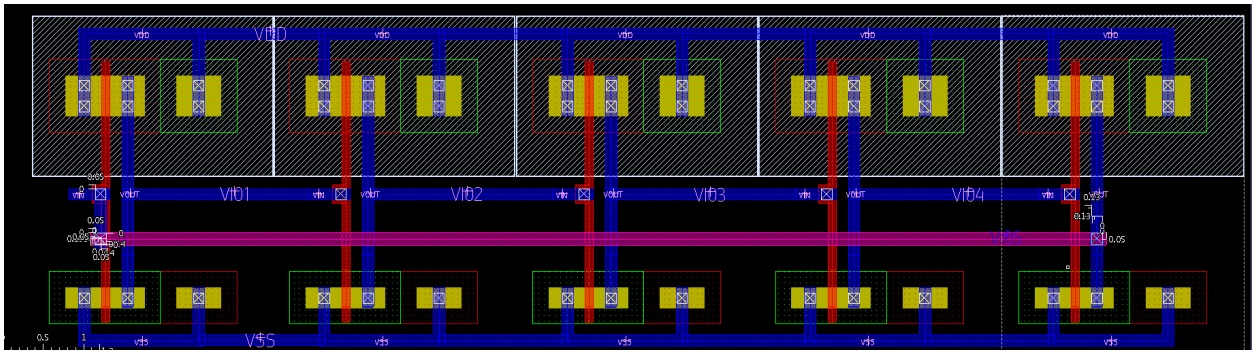
Post Simulation Result



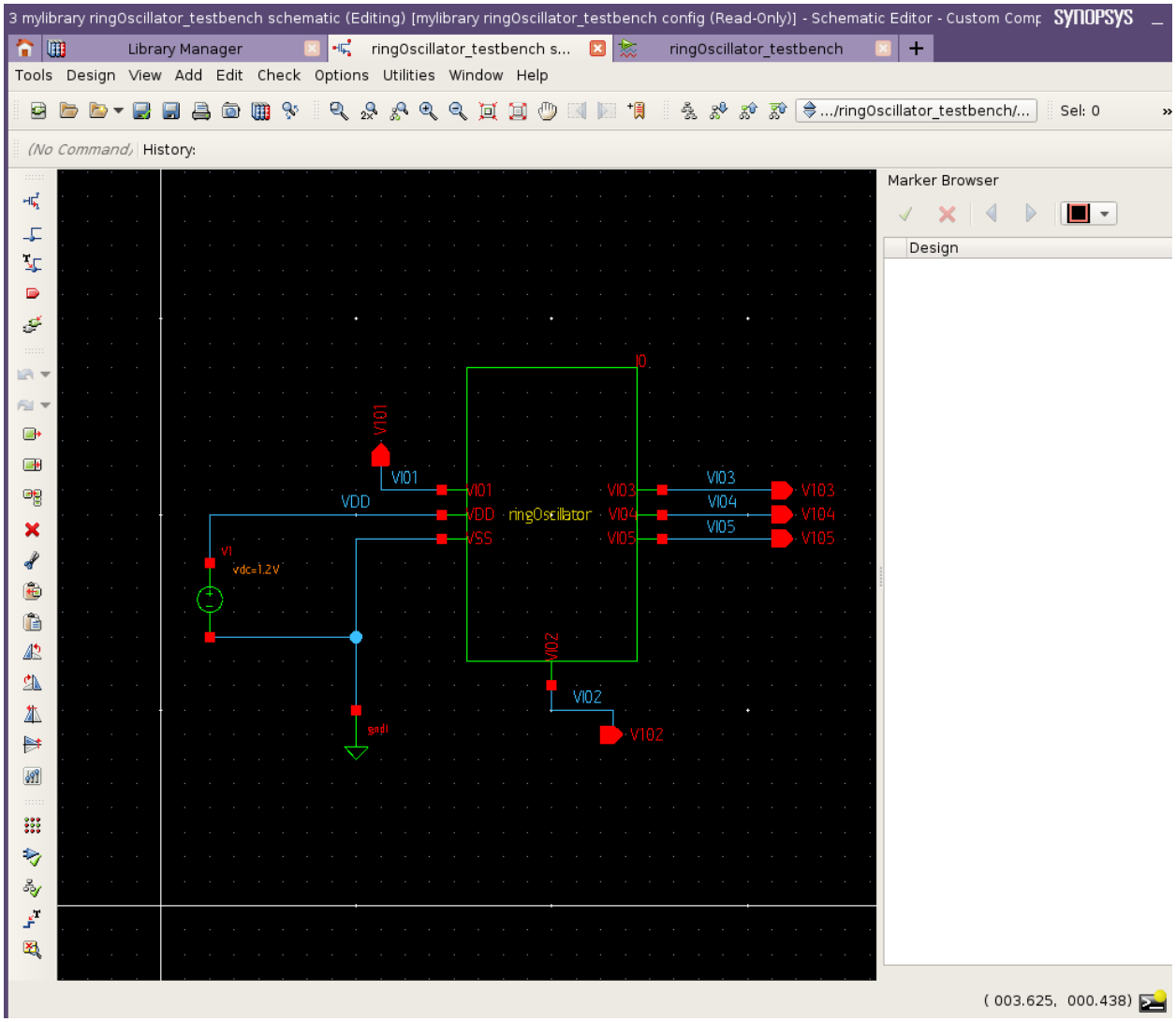
Ring Oscillator Schematic



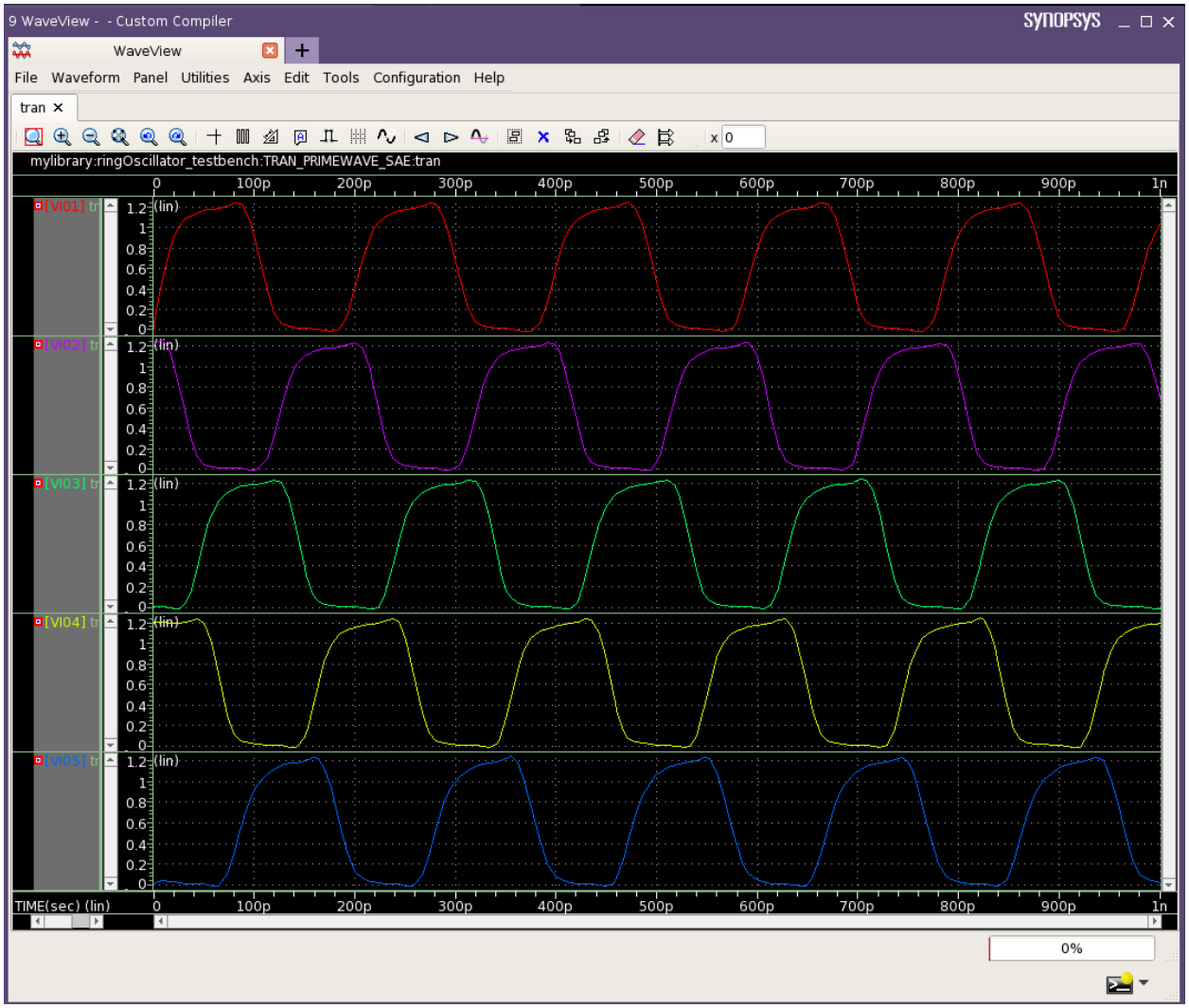
Ring Oscillator Layout



Ring Oscillator TestBench



Ring Oscillator POST SIMULATION with parasitic extrcaction



Issues

The only main hard issue that I had was running Primewave simulation on my inverter testbench. I made sure to set up everything according to the new setup and yet it still didn't function at all. I did however manage to get the output for the ring oscillator post parasitic extraction, and when I compared the two testbenches, they were almost identical in setup. I passed all DRC and LVS tests with both testbench and ring oscillator.