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| --- | --- | --- | --- | --- | --- | --- |
| 1 top\_reg | | | top\_reg | | Block | 0x0 |
| Offset | 0 | External | |  | size | 0x60 |
|  | | | | | | |
| oid=2e0449b9-399e-4d01-b743-6be1022fae41 | | | | | | |
| {reset\_type=async; intr.irq\_per\_channel=true; header.field\_mask = true; output\_file\_name=top\_reg\_ids; header.struct\_guard="NO\_REG\_STRUCT"} | | | | | | |

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| 1.1 CLOCK | | | | CLOCK | | | Block | | 0x0 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=467e1c36-0003-46bc-a533-febb7cdc91d5 | | | | | | | | | | |
|  | | | | | | | | | | |

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| 1.1.1 VERSION | | | | | | | | | | | | | | | | | | | VERSION | | | | | | | | | | | Reg | | | | | | 0x0 | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | |  | | | | | | default | | | | | | 0x000000a0 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=72d6ea10-c710-4d36-8a3b-66d77e329c59 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {registered=false} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | Name | | | | | | | s/w | | | | h/w | | | | Default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 31:0 | | VERSION | | | | | | | RO | | | | WO | | | | 0x000000A0 | | | | | Chip version read only register. | | | | | | | | | | | | | | | | | | | |

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| 1.1.2 CPU\_PLL\_CTRL | | | | | | | | | | | | | | | | | | | CPU\_PLL\_CTRL | | | | | | | | | | | Reg | | | | | | 0x4 | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | |  | | | | | | default | | | | | | 0x40006601 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=fba5cdb8-9d01-4f4c-b811-1adfd023221d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| This register controls the divider to output 1000MHz CPU\_CLK (target). Reference clock is 25MHz. CPU\_PLL 1000MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | Name | | | | | | | s/w | | | | h/w | | | | Default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 31 | | LOCK | | | | | | | RO | | | | WO | | | | 0 | | | | | CPU PLL Lock | | | | | | | | | | | | | | | | | | | |
| 30 | | RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | {rtl.hw\_set=1} {rtl.hw\_wp=1}  CPU PLL Reset, self-set bit.  Write 0 to trigger PLL reset. The bit will be self-set afterwards. | | | | | | | | | | | | | | | | | | | |
| 28 | | BYPASS | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit control signal to enable bypass  When 0: PLL operates normally  When 1: bypass mode is enabled | | | | | | | | | | | | | | | | | | | |
| 27 | | AFC\_ENB | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Low-active** 1-bit control signal for Auto Frequency Control  When 0: AFC is enabled and VCO is calibrated automatically  When 1: AFC is disabled and VCO is calibrated manually by EXTAFC field | | | | | | | | | | | | | | | | | | | |
| 26:22 | | EXTAFC | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 5-bit value used when AFC\_ENB=1, or AFC disabled. VCO is calibrated manually by EXTAFC for the test of VCO range | | | | | | | | | | | | | | | | | | | |
| 21 | | AFCINIT\_SEL | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value to select AFC initial delay  When 0: normal delay  When 1: twice of normal delay | | | | | | | | | | | | | | | | | | | |
| 20 | | PBIAS\_CTRL\_EN | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value. PBIAS voltage pull-down enable pin (active high) | | | | | | | | | | | | | | | | | | | |
| 19 | | PBIAS\_CTRL | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value. PBIAS pull-down initial voltage control pin.  When 0: 0.67 \* AVDD18  When 1: 0.50 \* AVDD18 | | | | | | | | | | | | | | | | | | | |
| 18:13 | | P | | | | | | | RW | | | | RO | | | | 0x3 | | | | | 6-bit wide pre-divider value, range should be from 1 to 63  NOTE: DO NOT SET TO 0 | | | | | | | | | | | | | | | | | | | |
| 12:3 | | M | | | | | | | RW | | | | RO | | | | 0xC0 | | | | | 10-bit wide main divider value, ranges should be from 64 to 1023  NOTE: DO NOT SET TO 0 | | | | | | | | | | | | | | | | | | | |
| 2:0 | | S | | | | | | | RW | | | | RO | | | | 0x1 | | | | | 3-bit wide scaler divider value, ranges could be from 0 to 6  2’b000: divided by 1  2’b001: divided by 2  2’b010: divided by 4  2’b011: divided by 8  2’b100: divided by 16  2’b101: divided by 32  2’b110: divided by 64  2’b111: PROHIBITED, DO NOT USE | | | | | | | | | | | | | | | | | | | |

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| 1.1.3 CPU\_PLL\_CTRL\_EXTRA | | | | | | | | | | | | | | | | | | | CPU\_PLL\_CTRL\_EXTRA | | | | | | | | | | | Reg | | | | | | 0x8 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000001 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=bb1eef90-d555-4b29-b20e-25e3c162a974 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Extra PLL control for CPU\_PLL. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 9:5 | | AFC\_CODE | | | | | | | RO | | | | WO | | | | 0 | | | | | Monitoring only. Output code of AFC (5bits) | | | | | | | | | | | | | | | | | | | |
| 4 | | FEED\_EN | | | | | | | RW | | | | RO | | | | 0 | | | | | Monitoring pin.  When 1: FEED\_OUT is enabled  When 0: FEED\_OUT is not enabled (default) | | | | | | | | | | | | | | | | | | | |
| 3 | | FOUT\_MASK | | | | | | | RW | | | | RO | | | | 0 | | | | | PLL Scaler’s re-initialization time control pin. Default is 0. | | | | | | | | | | | | | | | | | | | |
| 2 | | FSEL | | | | | | | RW | | | | RO | | | | 0 | | | | | Monitoring pin.  When 1: FEED\_OUT=FREF  When 0: FEED\_OUT=FEED | | | | | | | | | | | | | | | | | | | |
| 1:0 | | ICP | | | | | | | RW | | | | RO | | | | 1 | | | | | Charge pump current control signal.  Default is 2’b10, but model says 2’b01 | | | | | | | | | | | | | | | | | | | |

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| 1.1.4 DDR0\_PLL\_CTRL | | | | | | | | | | | | | | | | | | | DDR0\_PLL\_CTRL | | | | | | | | | | | Reg | | | | | | 0xc | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | |  | | | | | | default | | | | | | 0x40006801 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1b5a4ddb-3577-411d-8030-0369af03b81f | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| This register controls the divider to output 1066MHz DDR clock. Reference clock is 25MHz. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| Bits | | Name | | | | | | | s/w | | | | h/w | | | | Default | | | | | Description | | | | | | | | | | | | | | | | | | | |
| 31 | | LOCK | | | | | | | RO | | | | WO | | | | 0 | | | | | DDR PLL Lock | | | | | | | | | | | | | | | | | | | |
| 30 | | RSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | {rtl.hw\_set=1} {rtl.hw\_wp=1}  DDR PLL Reset | | | | | | | | | | | | | | | | | | | |
| 28 | | BYPASS | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit control signal to enable bypass  When 0: PLL operates normally  When 1: bypass mode is enabled | | | | | | | | | | | | | | | | | | | |
| 27 | | AFC\_ENB | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Low-active** 1-bit control signal for Auto Frequency Control  When 0: AFC is enabled and VCO is calibrated automatically  When 1: AFC is disabled and VCO is calibrated manually by EXTAFC field | | | | | | | | | | | | | | | | | | | |
| 26:22 | | EXTAFC | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 5-bit value used when AFC\_ENB=1, or AFC disabled. VCO is calibrated manually by EXTAFC for the test of VCO range | | | | | | | | | | | | | | | | | | | |
| 21 | | AFCINIT\_SEL | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value to select AFC initial delay  When 0: normal delay  When 1: twice of normal delay | | | | | | | | | | | | | | | | | | | |
| 20 | | PBIAS\_CTRL\_EN | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value. PBIAS voltage pull-down enable pin (active high) | | | | | | | | | | | | | | | | | | | |
| 19 | | PBIAS\_CTRL | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 1-bit value. PBIAS pull-down initial voltage control pin.  When 0: 0.67 \* AVDD18  When 1: 0.50 \* AVDD18 | | | | | | | | | | | | | | | | | | | |
| 18:13 | | P | | | | | | | RW | | | | RO | | | | 0x3 | | | | | 6-bit wide pre-divider value, range should be from 1 to 63  NOTE: DO NOT SET TO 0 | | | | | | | | | | | | | | | | | | | |
| 12:3 | | M | | | | | | | RW | | | | RO | | | | 0x100 | | | | | 10-bit wide main divider value, ranges should be from 64 to 1023  NOTE: DO NOT SET TO 0 | | | | | | | | | | | | | | | | | | | |
| 2:0 | | S | | | | | | | RW | | | | RO | | | | 0x1 | | | | | 3-bit wide scaler divider value, ranges could be from 0 to 6  2’b000: divided by 1  2’b001: divided by 2  2’b010: divided by 4  2’b011: divided by 8  2’b100: divided by 16  2’b101: divided by 32  2’b110: divided by 64  2’b111: PROHIBITED, DO NOT USE | | | | | | | | | | | | | | | | | | | |

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| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |
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| 1.2 RESET | | | | RESET | | | Block | | 0x50 | |
| offset | 0x50 | External |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=4f31c4c4-36f3-4aa8-af44-c675d7e4b1e3 | | | | | | | | | | |
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| 1.2.1 CPU\_RSTB\_CTRL | | | | | | | | | | | | | | | | | | | CPU\_RSTB\_CTRL | | | | | | | | | | | reg | | | | | | 0x50 | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | |  | | | | | | default | | | | | | 0x3b8e0ec3 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=6738fee6-3be6-4cc5-9162-16029d82855e | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| This register controls the reset of both NVMe and FTL core. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | Name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 29 | | CORE3\_VECTOR\_SEL | | | | | | | RW | | | | RO | | | | 1 | | | | | CORE3 reset vector select  0=reset vector 0 BOOTROM  1=reset vector 1 CORE3 IRAM | | | | | | | | | | | | | | | | | | | |
| 28 | | CORE3\_RUN\_STALL | | | | | | | RW | | | | RO | | | | 1 | | | | | Core3 CPU stall  0=run  1=stall | | | | | | | | | | | | | | | | | | | |
| 27 | | CORE3\_DRSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | Write 0 to keep debug logic in reset | | | | | | | | | | | | | | | | | | | |
| 26 | | CORE3\_BRSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | When 0: CORE3 held in reset  When 1: CORE3 not in reset | | | | | | | | | | | | | | | | | | | |
| 25 | | CORE2\_VECTOR\_SEL | | | | | | | RW | | | | RO | | | | 1 | | | | | Core2 reset vector select  0=reset vector 0 BOOTROM  1=reset vector 1 Core2 IRAM | | | | | | | | | | | | | | | | | | | |
| 24 | | CORE2\_RUN\_STALL | | | | | | | RW | | | | RO | | | | 1 | | | | | Core2 CPU stall  0=run  1=stall | | | | | | | | | | | | | | | | | | | |
| 23 | | CORE2\_DRSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | Write 0 to keep debug logic in reset | | | | | | | | | | | | | | | | | | | |
| 22 | | CORE2\_BRSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | When 0: Core2 held in reset  When 1: Core2 not in reset | | | | | | | | | | | | | | | | | | | |
| 21 | | NVM\_RUN\_STALL\_FINAL | | | | | | | RO | | | | WO | | | | 0 | | | | | Together (XOR) with BOOTMODE[0] and EFUSE external boot selection, this register bit shows the final NVM CPU stall control  The formula is NVM\_RUN\_STALL ^ (bootmode[0] & !EFUSE\_EXT\_BOOT)  0=run  1=stall | | | | | | | | | | | | | | | | | | | |
| 20 | | NVM\_VECTOR\_SEL\_FINAL | | | | | | | RO | | | | WO | | | | 0 | | | | | Together (XOR) with BOOTMODE[0] and EFUSE external boot selection, this register bit shows the final NCPU reset vector select  The formula is NVM\_VECTOR\_SEL ^ (bootmode[0] & !EFUSE\_EXT\_BOOT)  0=reset vector 0 is BOOTROM  1=reset vector 1 is NCPU IRAM | | | | | | | | | | | | | | | | | | | |
| 19 | | NVM\_SS\_RSTB\_EN | | | | | | | RW | | | | RO | | | | 1 | | | | | Enable for NVME register subsystem | | | | | | | | | | | | | | | | | | | |
| 18 | | NVM\_SS\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | NVM register Subsystem Reset  When 0: NVM register SS held in reset  When 1: NVM register SS not held in reset | | | | | | | | | | | | | | | | | | | |
| 17 | | CPU\_SS\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | {rtl.hw\_set=1} {rtl.hw\_wp=1}  CPU subsystem active low reset | | | | | | | | | | | | | | | | | | | |
| 15:14 | | MDMA\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | Main DMA engine 0 and 1 active low reset  MDMA\_RSTB[15] = MDMA1 reset  MDMA\_RSTB[14] = MDMA0 reset | | | | | | | | | | | | | | | | | | | |
| 12 | | FTL\_XOCD\_MODE | | | | | | | RO | | | | WO | | | | 0 | | | | | FTL CPU XOCD mode status | | | | | | | | | | | | | | | | | | | |
| 11 | | FTL\_RUN\_STALL | | | | | | | RW | | | | RO | | | | 1 | | | | | FTL CPU stall  0=run  1=stall | | | | | | | | | | | | | | | | | | | |
| 10 | | FTL\_VECTOR\_SEL | | | | | | | RW | | | | RO | | | | 1 | | | | | FTL reset vector select  0=reset vector 0 BOOTROM  1=reset vector 1 FCPU IRAM | | | | | | | | | | | | | | | | | | | |
| 9 | | FTL\_DRSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | Write 0 to keep debug logic in reset | | | | | | | | | | | | | | | | | | | |
| 8 | | FTL\_BRSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | When 0: FTL Core held in reset  When 1: FTL Core not in reset | | | | | | | | | | | | | | | | | | | |
| 7 | | ROM\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | ROM active low reset | | | | | | | | | | | | | | | | | | | |
| 6 | | SYSRAM\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | System RAM active low reset | | | | | | | | | | | | | | | | | | | |
| 4 | | NVM\_XOCD\_MODE | | | | | | | RO | | | | WO | | | | 0 | | | | | NVM CPU XOCD mode status | | | | | | | | | | | | | | | | | | | |
| 3 | | NVM\_RUN\_STALL | | | | | | | RW | | | | RW | | | | 0 | | | | | Together (XOR) with BOOTMODE[0] and EFUSE external boot selection, this register bit determines final NVM CPU stall control  The formula is NVM\_RUN\_STALL ^ (bootmode[0] & !EFUSE\_EXT\_BOOT)  0=run  1=stall | | | | | | | | | | | | | | | | | | | |
| 2 | | NVM\_VECTOR\_SEL | | | | | | | RW | | | | RW | | | | 0 | | | | | Together (XOR) with BOOTMODE[0] and EFUSE external boot selection, this register bit determines final NCPU reset vector select  The formula is NVM\_VECTOR\_SEL ^ (bootmode[0] & !EFUSE\_EXT\_BOOT)  0=reset vector 0 is BOOTROM  1=reset vector 1 is NCPU IRAM | | | | | | | | | | | | | | | | | | | |
| 1 | | NVM\_DRSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | {rtl.hw\_set=1} {rtl.hw\_wp=1}  Always read 1.  Write 0 to clear NVMe debug core, this bit is self-set.  Write 0 to keep debug logic in reset | | | | | | | | | | | | | | | | | | | |
| 0 | | NVM\_BRSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | {rtl.hw\_set=1} {rtl.hw\_wp=1}  Always read 1.  Write 0 to clear NVMe core, this bit is self-set. | | | | | | | | | | | | | | | | | | | |

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| 1.2.2 BLK\_RSTB\_CTRL | | | | | | | | | | | | | | | | | | | BLK\_RSTB\_CTRL | | | | | | | | | | | reg | | | | | | 0x54 | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | |  | | | | | | default | | | | | | 0x0000004e | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=e2b9db98-214c-4544-b991-6d16f98da6d0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| This register controls the reset bits to all subsystems | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | Name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 31 | | DDR3\_RSTB | | | | | | | rw | | | | ro | | | | 0 | | | | | DDR3 Subsystem  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 30 | | DDR2\_RSTB | | | | | | | rw | | | | ro | | | | 0 | | | | | DDR2 Subsystem  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 29 | | DDR1\_RSTB | | | | | | | rw | | | | ro | | | | 0 | | | | | DDR1 Subsystem  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 28 | | DDR0\_RSTB | | | | | | | rw | | | | ro | | | | 0 | | | | | DDR0 Subsystem  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 27 | | AI1\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AI1\_SS reset bit  When 0: AI1\_SS held in reset  When 1: AI1\_SS not in reset | | | | | | | | | | | | | | | | | | | |
| 26 | | AUDIO\_SS\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | AUDIO\_SS registers reset bit  When 0: AUDIO\_SS registers held in reset  When 1: AUDIO\_SS registers not in reset | | | | | | | | | | | | | | | | | | | |
| 25:24 | | WDT\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | Watchdog Timer (WDT) for WDT0 and WDT1  When 0: subsystem held in reset  When 1: subsystem not in reset  NOTES:   * WDT needs to be re-enabled and re-initialized after reset . * Putting WDT into reset should NOT cause system hang | | | | | | | | | | | | | | | | | | | |
| 23 | | GPIO\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 22 | | SPI\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 21:20 | | I2C\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | I2C\_RSTB[21] = I2C1 reset  I2C\_RSTB[20] = I2C0 reset  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 19 | | UART1\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | UART\_RSTB[19] = UART1 reset  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 18 | | UART0\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | UART\_RSTB[18] = UART0 reset  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 17 | | PERI\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | Peripheral Subsystem  When 0: subsystem held in reset  When 1: subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 16 | | AUDIO1\_ZSP\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AUDIO1\_ZSP reset bit  When 0: AUDIO1\_ZSP held in reset  When 1: AUDIO1\_ZSP not in reset | | | | | | | | | | | | | | | | | | | |
| 15 | | AUDIO1\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AUDIO1 reset bit  When 0: AUDIO1 held in reset  When 1: AUDIO1 not in reset | | | | | | | | | | | | | | | | | | | |
| 14 | | AUDIO0\_ZSP\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AUDIO0\_ZSP reset bit  When 0: AUDIO0\_ZSP held in reset  When 1: AUDIO0\_ZSP not in reset | | | | | | | | | | | | | | | | | | | |
| 13 | | AUDIO0\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AUDIO\_0 reset bit  When 0: AUDIO0 held in reset  When 1: AUDIO0 not in reset | | | | | | | | | | | | | | | | | | | |
| 12 | | PCI\_PIPE\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | PCI PIPE\_RESET\_N (PIPE\_CLK)  When 0: PCI Pipe subsystem held in reset  When 1: PCI Pipe subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 11 | | PCI\_MGMT\_STICKY\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | PCI MGMT\_STICKY\_RESET\_N(PCI\_CLK)  When 0: PCI management sticky subsystem held in reset  When 1: PCI management sticky subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 10 | | PCI\_MGMT\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | PCI MGMT\_RESET\_N(PCI\_CLK)  When 0: PCI management subsystem held in reset  When 1: PCI management subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 9 | | PCI\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | PCI RESET\_N (PCI\_CLK)  When 0: PCI subsystem held in reset  When 1: PCI subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 8 | | PCI\_PM\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | PCI PM\_RESET\_N  PM\_CLK = PCI management CLOCK  When 0: PCI PM subsystem held in reset  When 1: PCI PM subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 7 | | AI0\_RSTB | | | | | | | RW | | | | Ro | | | | 0 | | | | | AI0\_SS reset bit  When 0: AI0\_SS held in reset  When 1: AI0\_SS not in reset | | | | | | | | | | | | | | | | | | | |
| 6 | | EFUSE\_RSTB | | | | | | | rw | | | | ro | | | | 1 | | | | | When 0: EFUSE subsystem held in reset  When 1: EFUSE subsystem not in reset  OBSOLETE and RESERVED  For security reason, no one can reset EFUSE | | | | | | | | | | | | | | | | | | | |
| 5:4 | | TIMER\_RSTB | | | | | | | rw | | | | Ro | | | | 0 | | | | | TIMER\_RSTB[5] = TIMER1 reset  TIMER\_RSTB[4] = TIMER0 reset  When 0: top timer subsystem held in reset  When 1: top timer subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 3 | | TIMESTAMP\_RSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | When 0: top timestamp subsystem held in reset  When 1: top timestamp subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 2 | | SEQUENCER\_RSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | {rtl.hw\_set=1}{rtl.hw\_wp=1}  It resets chip bootup sequencer logic. Sometimes called DUT reset.  Please Use with caution.  When 0: top sequencer subsystem held in reset  When 1: top sequencer subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 1 | | TOP\_RSTB | | | | | | | rw | | | | Ro | | | | 1 | | | | | {rtl.hw\_set=1}{rtl.hw\_wp=1}  It resets bootstrap state machine.  When 0: top core subsystem held in reset  When 1: top core subsystem not in reset | | | | | | | | | | | | | | | | | | | |

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| 1.2.3 BLK\_RSTB\_CTRL\_1 | | | | | | | | | | | | | | | | | | | BLK\_RSTB\_CTRL\_1 | | | | | | | | | | | reg | | | | | | 0x58 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | false | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=41e63c59-f1ae-45a4-9fe2-dd130f0bd7c6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 11:8 | | SCLR\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | Reset bits for scaler 0-3  When 0: scaler held in reset  When 1: scaler not in reset | | | | | | | | | | | | | | | | | | | |
| 7:4 | | ENC\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | Reset bits for encoder 0-3  When 0: encoder held in reset  When 1: encoder not in reset | | | | | | | | | | | | | | | | | | | |
| 3:0 | | DEC\_RSTB | | | | | | | RW | | | | RO | | | | 0 | | | | | Reset bits for decoder 0-3  When 0: decoder held in reset  When 1: decoder not in reset | | | | | | | | | | | | | | | | | | | |

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| 1.2.4 NOC\_RSTB\_CTRL | | | | | | | | | | | | | | | | | | | NOC\_RSTB\_CTRL | | | | | | | | | | | reg | | | | | | 0x5c | | | | | |
| Offset | | | | | | |  | | | | | | | | External | | | | | | | | | false | | | | | | default | | | | | | 0xe00000d1 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=82b10356-f3d3-47f0-bd08-5107c797ba62 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| This register controls the reset bits to all subsystems | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | Name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 31 | | CENTRAL\_NOC\_RSTB | | | | | | | RO | | | | WO | | | | 1 | | | | | {registered=false}  **Read-only** bit for NOC reset input  When 0: CENTRAL NOC held in reset  When 1: CENTRAL NOC not in reset | | | | | | | | | | | | | | | | | | | |
| 30 | | CFG\_NOC\_RSTB | | | | | | | RO | | | | WO | | | | 1 | | | | | {registered=false}  **Read-only** bit for NOC reset input  When 0: CFG NOC held in reset  When 1: CFG NOC not in reset | | | | | | | | | | | | | | | | | | | |
| 29 | | CPU\_NOC\_RSTB | | | | | | | RO | | | | WO | | | | 1 | | | | | {registered=false}  **Read-only** bit for NOC reset input  When 0: CPU NOC subsystem held in reset  When 1: CPU NOC subsystem not in reset | | | | | | | | | | | | | | | | | | | |
| 7 | | PCIE\_NOC\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | Reset bit to reset PCIe NIU  When 0: PCIE NIU held in reset  When 1: PCIE NIU not in reset | | | | | | | | | | | | | | | | | | | |
| 6 | | AUDIO\_NOC\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | Reset bit to reset AUDIO\_NOC  When 0: AUDIO NOC held in reset  When 1: AUDIO NOC not in reset | | | | | | | | | | | | | | | | | | | |
| 5:4 | | AI\_NOC\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | Reset bit to reset AI\_NOC  When 0: AI NOC held in reset  When 1: AI NOC not in reset | | | | | | | | | | | | | | | | | | | |
| 3:0 | | VIDEO\_NOC\_RSTB | | | | | | | RW | | | | RO | | | | 1 | | | | | Reset bit to reset VIDEO\_NOC  When 0: VIDEO NOC held in reset  When 1: VIDEO NOC not in reset | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |