UNIVERSITY OF VIRGINIA
DIGITAL LOGIC DESIGN
STUDIO ASSIGNMENT 11

This assignment is to be completed without any aid from anyone other than the teaching staff for this class. You may use only the class text, other materials provided to you by the teaching staff for this class, and your own class notes to complete this assignment. You must not offer or provide aid to others taking this class. Submission of any part of this assignment represents your affirmation that you have complied with these requirements.

OBJECTIVE

This studio assignment will give you the opportunity to design an RTL system using LogisimFSM.

PROBLEM DESCRIPTION

Design an RTL system that computes the sum of all the positive integers stored in a register.

PRE-WORK

1. Start with the MysteryRTL circuit from class and change it so that it computes the sum of all the positive integers from the register file rather than finding the max or the min of the values. Assume that the numbers stored in the register file are all represented in 2's complement notation.
2. If overflow occurs anywhere in the computation, illuminate an LED and keep it illuminated until the end of the computation.
3. Submit your completed LogisimFSM file to collab before the beginning of your studio session.

IN STUDIO

Be prepared to demonstrate how your circuit works and to answer questions during your studio session.

GRADING SCALE

- 3 points for the datapath
- 3 points for the controller
- 2 points for explanation
- 2 points for professionalism & answering questions