UNIVERSITY OF VIRGINIA
DIGITAL LOGIC DESIGN
STUDIO ASSIGNMENT COUNTER DESIGN

This assignment is to be completed without any aid from anyone other than the teaching staff for this class. You may use only the class text, other materials provided to you by the teaching staff for this class, and your own class notes to complete this assignment. You must not offer or provide aid to others taking this class. Submission of any part of this assignment represents your affirmation that you have complied with these requirements.

OBJECTIVE

This studio assignment will give you the opportunity to design a simple finite state machine (FSM) to generate a specific output sequence.

PROBLEM DESCRIPTION

You are to design, simulate and build a 3-bit synchronous counter that produces the sequence

111, 101, 100, 000, 010, 011, 111, etc.

whenever the single input X is 1. The counter retains its current value whenever the input X is 0. The count output should only change on the rising edge of the clock.

PRE-WORK

1. Design your counter, deriving minimal functions for the D flip-flop excitation functions.
2. Use *Logisim* to represent, analyze, simulate and test your design before coming to the lab. Use D flip flops.
3. Use a hex display element to display the current state.
4. Use a button that sets the initial state. At this point you can pick whatever initial state you want but be prepared to change your circuit to start in a state that is given by the TA during your demonstration.

IN STUDIO

Bring your completed *Logisim* file and your documented design procedure to the studio to be reviewed by your studio instructor. Be prepared to answer questions about your design and make suggested changes to demonstrate understanding.

ANALYSIS

Your counter has a couple of don't care states. Set your initial state to be one of the don't care states and observe the next state behavior. Then do the same with the other don't care state. Be prepared to explain to the instructor why your circuit behaves as it does. Your circuit may behave differently from others' circuits.

GRADING SCALE

- 5 points for D FF design and implementation, including a well-documented and professional design process
- 1 point for using a hex display element with a splitter to display they current state to make it easy to see the state progression
- 1 point for using a button to establish the initial state
- 2 points for explanation and answering questions
- 1 point for professionalism