ECE/CS 2330 Digital Logic Design
University of Virginia
Studio Assignment Adder Design: Part 2

Standard honor statement.
This assignment is quite involved and will take a long time. Procrastinate at your own peril.

Objective

This studio assignment will give you the opportunity to design and compare several alternative design approaches for a combinational data processing element.

Problem Description

You are to design a binary adder which can add two signed 16-bit binary numbers in 2's complement representation. You will implement and evaluate several approaches using *Logisim* in a 2-part studio assignment. You will then extend this adder to allow it to perform subtraction as well. Use sections 4.3 and 6.4 in the text as a reference for this assignment. Read these sections very carefully so that you understand what you are building.

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Design Procedure

Be sure that you understand the full set of instructions before you begin. Your ability to answer the questions at the end may determine the design approach that you use for the different parts of this assignment.

1. Use an appropriate number of 1-bit full adders in *Logisim* to create a 16-bit ripple-carry adder. You can use *Logisim*'s built-in adder (set to add 2 bits) as a full adder. The basic design should resemble that shown in Figure 4.32 in the text (except that yours will produce a 16-bit adder instead of a 4-bit adder as shown in Figure 4.32). Connect these full adders together to produce a 16-bit adder.
2. Build a 4-bit carry-lookahead adder (CLA) explicitly (i.e. from discrete gates) using the approach demonstrated in Figure 6.56 in the text. Then use an appropriate number of these 4-bit carry-lookahead adders (use subcircuits) in a ripple-carry configuration to create a 16-bit adder as shown in Figure 6.59 of the text. Your circuits must match the figures exactly, same inputs and outputs.
3. Extend your 4-bit carry-lookahead adder (that you designed in step 2 above) to create two additional outputs (P and G) as shown in Figure 6.60 of the text. Then design the 4-bit carry-lookahead logic block as shown in Figure 6.60 in the text. Connect them as appropriate to create another 16-bit adder, with an overflow detector also. Look carefully at the figures in the text.
4. For each of your designs (from steps 1-3 plus your design from part 1) calculate the **delay**, that is, the length (in gates) of the longest path from any input to any output.

Pre-Work

Your designs should be complete before you come to the studio. Every input and output must be clearly labeled.

Grading

- 2 points for ripple-carry connection of full adders (step 1) including explanation
- 2 point for 4-bit CLA including explanation
- 1 point for 4-bit CLA connected with ripple-carry to form 16-bit adder including explanation
- 2 points for 16-bit CLA with carry-lookahead logic block including explanation
- 2 points for delay discussion with TA
- 1 point for professionalism