

SUPPLEMENTARY INFORMATION for:

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"Rapid technological progress in white light-emitting diodes and its sources in innovation and technology spillovers" *Environmental Science & Technology* (2023)

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## Contents

<b>1</b>	<b>Metrics</b>	<b>2</b>
1.1	Luminous Efficacy of Radiation . . . . .	2
1.2	Luminous Efficacy of Source . . . . .	2
1.3	Sub-Efficiencies . . . . .	2
1.3.1	Forward Voltage Efficiency $\eta_{V_f}$ . . . . .	3
1.3.2	Light Extraction Efficiency $\eta_{LE}$ . . . . .	3
1.3.3	Internal Quantum Efficiency $\eta_{IQ}$ . . . . .	3
1.3.4	Droop $\eta_{droop}$ . . . . .	3
1.3.5	Conversion Efficiency $\eta_C$ . . . . .	4
1.3.6	Spectral Efficiency $\eta_S$ . . . . .	4
<b>2</b>	<b>Methodology</b>	<b>5</b>
2.1	Systematic Literature Review . . . . .	5
2.2	Semi-Structured Interviews . . . . .	5
2.3	Performance Metrics Calculations . . . . .	6
2.4	Manufacturing Cost Model . . . . .	7
2.4.1	Our Approach to Cost Modeling . . . . .	7
2.4.2	Structure of the Model . . . . .	8
2.4.3	Manufacturing Process Steps by Chip Architecture . . . . .	8
2.4.4	Computation of Manufacturing Cost . . . . .	14
2.4.5	Computation of Yielded Cost . . . . .	16
2.4.6	Example of Input Data Considered: Sapphire Wafers . . . . .	17
2.4.7	Preliminary Sensitivity Analysis . . . . .	18
2.5	Computation of Contribution of Individual Variables . . . . .	20
<b>3</b>	<b>Additional Results</b>	<b>22</b>
3.1	Historical Progress in Sub-Efficiencies . . . . .	22
3.2	LED Innovations . . . . .	24
3.2.1	Non-Phosphor-Related . . . . .	24
3.2.2	Phosphor-Related . . . . .	24
3.3	Cost Comparison with Reported Industry Data and DOE Projections . . . . .	28
<b>4</b>	<b>Complete List of Sources for Figures</b>	<b>29</b>
4.1	Figure 1 (Historical Development of Luminous Efficacy) . . . . .	29
4.2	Figure 2 (Historical Development of Lamp Prices) . . . . .	29
4.3	Figure 3 (Historical Evolution of LED Chip Architectures) . . . . .	29
4.4	Fig. SI10 (Historical Developments in Device Sub-Efficiencies) . . . . .	29

# 1 Metrics

## 1.1 Luminous Efficacy of Radiation

Figure 1 in the main publication uses luminous efficacy of radiation as the primary metric to describe progress in lighting technologies. Care must be taken not to confuse this metric with luminous efficacy of source, which is used in Fig. SI11.

This metric describes the match of a light-emitting diode package spectrum to the human visual system. Efficacy in lighting is dependent on the luminosity function, which describes the wavelength-dependent sensitivity of the human eye. A light source emitting very *efficiently* in the infrared yet emitting no visible light has a very low *efficacy*. The luminous efficacy of radiation  $K$  is mathematically defined as the normalized, integrated product of the spectral radiant flux of a light source with the wavelength-dependent human sensitivity to light [1]

$$K[\text{lm/W}_{opt}] = \frac{\int_0^\infty K(\lambda)\phi d\lambda}{\int_0^\infty \phi d\lambda} \quad (\text{SI1})$$

where

$K$  ... spectral luminous efficacy

$\phi$  ... spectral radiant flux

$\lambda$  ... wavelength

This metric can be computed from spectral data alone and does not require additional spectral normalization. It enables straightforward comparison between the performance of different downconversion phosphors, as shown in the top panel of Fig. SI11. Light sources emitting in the far red or blue part of the spectrum have lower efficacy of radiation. Care must be taken not to confuse this efficacy metric with the *efficacy of source* described in the following subsection.

## 1.2 Luminous Efficacy of Source

The luminous efficacy *of a light source*  $\eta$  is defined as the ratio between the emitted luminous flux and the consumed electrical power [2]

$$\eta[\text{lm/W}_{el}] = \frac{\phi}{P_{el}} \quad (\text{SI2})$$

This metric is often cited in device datasheets, scientific literature and textbooks when describing the performance of light-emitting diodes. Care must be taken not to confuse this efficacy metric with the *luminous efficacy of radiation*, which depends only on the spectral characteristics of a light source. As the luminous efficacy of a light source  $\eta$  captures the overall device efficacy, it depends on a large number of other device properties and parameters. This makes attribution of changes in this metric to individual changes in device design or manufacturing difficult. For this reason, we do not use this metric in our study.

## 1.3 Sub-Efficiencies

This subsection provides definitions and equations for the LED device sub-efficiencies introduced in the Metrics section in the main text.

### 1.3.1 Forward Voltage Efficiency $\eta_{V_f}$

Device forward voltage efficiency<sup>1</sup> (VfE) describes all electrical losses at the interface between the electrodes and the semiconductor and in the bulk. These losses can be due to tunneling and Ohmic resistance at the interface, as well as Ohmic resistance and other electrical losses within the bulk of the semiconductor. It is defined as

$$\eta_{V_f} = \frac{E_{h\nu}}{V_f} \quad (1)$$

where  $E_{h\nu}$  denotes the photon energy and  $V_f$  is the diode forward voltage [4][3].

### 1.3.2 Light Extraction Efficiency $\eta_{LE}$

Device light-extraction efficiency (LEE) describes the losses due to absorption in the material after electron-hole recombination and the associated emission of a photon. It is defined as

$$\eta_{LE} = \frac{\# \text{ of photons out}}{\# \text{ of photons created}} = \frac{P_{opt}}{P_{int}} \quad (2)$$

where  $P_{opt}$  is the optical power of the device and  $P_{int}$  is the internal power of the device[4][3].

### 1.3.3 Internal Quantum Efficiency $\eta_{IQ}$

Internal quantum efficiency (IQE) describes non-radiative recombinatory processes in the semiconductor bulk. It is related to the external quantum efficiency through

$$\eta_{EQ} = \eta_{IQ} \times \eta_{LE} \quad (3)$$

and defined as

$$\eta_{IQ} = \frac{\# \text{ of photons created}}{\# \text{ of electron-hole pairs in}} \quad (4)$$

and depends on the current density of the device[4][3].

### 1.3.4 Droop $\eta_{droop}$

Efficiency droop describes the decrease of device internal quantum efficiency at high current densities, which is caused by a number of different physical effects[5]. This is often treated separately from internal quantum efficiency in the literature due to its importance in high-power devices. It is defined as

$$\eta_{droop} = 1 - \frac{\eta_{IQE}}{\eta_{IQE}(A \rightarrow 0)} \quad (5)$$

where  $\eta_{IQE}(A \rightarrow 0)$  denotes the internal quantum efficiency at low current densities. In practice, droop is often given as the percentage difference between the ideal luminous intensity curve  $\phi_{ideal}$  and the real luminous intensity curve  $\phi$  at a set diode test current  $A_{test}$  as

$$D = \frac{\phi_{ideal}(A_{test}) - \phi(A_{test})}{\phi_{ideal}(A_{test})/100} \quad (6)$$

---

<sup>1</sup>"Joule Efficiency"  $\epsilon_J$  in Tsao et al. [3]

Therefore, according to this definition, a lack of droop corresponds to a droop efficiency of  $\eta_{droop} = 100\%$ [4][3].

### 1.3.5 Conversion Efficiency $\eta_C$

Light conversion efficiency (LCE) describes losses in the conversion process of blue light that is the basis for all phosphor-converted white LEDs. These losses are the sum of the Stokes loss and well as scattering/absorption losses. It is defined as

$$\eta_C = \frac{E_B}{\sum_{i=\text{Red, Orange, Yellow, Green}} E_i} \quad (7)$$

where  $E_i$  denotes the total energy of light at the color corresponding to the down-converted photon wavelength [4][3]. Since every individual phosphor component in the device has its own associated conversion losses, the denominator sums over all components, i.e. Red, Orange, Yellow, Green.

### 1.3.6 Spectral Efficiency $\eta_S$

Spectral efficiency (SE) describes losses in the conversion process due to the wavelength-dependent efficiency of the human eyes. Photons converted into the infrared or ultraviolet are lost to illumination purposes. It is defined as

$$\eta_S = \frac{K}{K_{max}(CRI, CCT)} \quad (8)$$

where  $K$  is the luminous efficacy of radiation of the light source, which can be computed from the device spectrum and the luminosity function, which describes the sensitivity of the human eye.  $K_{max}$  is the maximum luminous efficacy of radiation of a perfect light source with the same color rendering performance and correlated color temperature as the light source in question[4][3].

## 2 Methodology

This subsection provides the details for the main methods and data sources used in our mixed-methods research approach, including the systematic literature review, semi-structured interviews with eminent experts, manufacturing cost modelling, and performance metrics calculations.

### 2.1 Systematic Literature Review

We collected data on LED performance and characteristics in a systematic literature review that included scientific publications, patents, conference proceedings from the largest semiconductor and optoelectronics conferences, industry periodicals and roadmaps, as well as company presentations and reports. This review was structured around the three main goals: 1) tracking the evolution of LED technology over time as indicated by three groups of progress metrics introduced in the main article; 2) identifying individual innovations that contributed to this evolution and whether or not they could be spillovers, and quantifying their impact on device performance and manufacturing cost; and 3) determining whether these innovations had originated within the LED technology domain, or in a field of research or technology outside of solid-state lighting, making them a technology spillovers.

Relevant sources for the review were found in an iterative search process that involved two components. The first was the search in specialized patent and publication databases as well as company websites. The second component was the analysis of backward citations in the identified sources, starting from the reviews mentioned in section Previous Literature in the main article and then iteratively repeating it for all newly identified sources, until no further relevant and significant new sources were found. We also relied on backward citations for the identification of technology spillovers, considering cited documents as indicators of knowledge origins of an innovation and analyzing whether those documents belonged to the LED technology domain or not.

### 2.2 Semi-Structured Interviews

To supplement our data collection efforts, verify our findings and identify additional spillovers, we conducted a series of elite semi-structured interviews with eleven eminent experts from academia, industry and the public research sector. Experts were selected based on their engagement in different sub-fields of LED research and manufacturing, as well as the recommendations from other interviewed experts, in essence expanding the list of experts that emerged from the initial literature review. All interviews were conducted between November 2019 and April 2022 by means of video conferencing and lasted for about one hour. A summary of the background of interviewed experts is provided in Table SI1.

The primary, structured part of the interviews explored which innovations were deemed most relevant to the evolution of device performance, consumer experience and manufacturing cost of LED packages. Thereafter, interviewees were asked to consider the extent to which these innovations may have originated outside of their respective field of expertise and the LED industry more broadly—i.e., which of the innovations may be considered spillovers. The remainder of the interview was focused on learning about particular aspects of the manufacturing processes relevant to cost and performance modelling, the current state of industry, and the circumstances surrounding the innovations and spillovers identified in the first part of the interview. Specific quantitative data was also provided by experts, helping fine-tune the parameters of the manufacturing cost model (described in Section 2) and verify device performance data.

Table SII: Anonymized list of LED experts interviewed for this study. Abbreviations: sr. - senior

#	Sector	Role	Country	Expertise
1	Academia	Sr. researcher	UK	Epitaxy
2	Industry	Consultant, former sr. researcher	USA	Device architecture
3	Industry	Consultant, former head of R&D	Germany	Epitaxy
4	Academia	Professor	Austria	Phosphors
5	Industry	Consultant, former head of R&D	USA	Device architecture
6	Consulting	Consultant, former sr. technical advisor	USA	Device architecture
7	Academia	Professor	Germany	Phosphors
8	Government	R&D manager	USA	Device architecture
9	Consulting	Consultant	USA	Device applications
10	Academia	Professor	France	Device physics
11	Industry	Sr scientist, former head of R&D	USA	Device architecture
12	Industry	Principal scientist	Germany	Phosphors
13	Industry	Former head of R&D	USA	Phosphors

## 2.3 Performance Metrics Calculations

The contribution of individual technology innovations and spillovers to the progress in overall device efficiency over time is estimated by index decomposition analysis. Mathematically, this involves breaking down a chosen performance indicator into its constituent components, each representing a specific factor that contributes to the change in the indicator [6]. Specifically, we use the additive logarithmic mean Divisia index method I (LMDI-I), also known as the Additive Sato-Vartia indicator [7]. It was developed by Boyd in 1987 [8] on the basis of Divisia Index, a method in statistical economics [9], and subsequently refined.

According to this method, for an overall device efficiency function  $F$  that is the product of variables  $a, b$  that represent sub-efficiencies, the contribution of the change in a single sub-efficiency variable  $a$  between times  $t = 0$  and  $t = T$  can be estimated as [10]

$$\Delta a = \frac{a_{t=T} - a_{t=0}}{\ln(a_{t=T}) - \ln(a_{t=0})} \times \ln\left(\frac{a_{t=T}}{a_{t=0}}\right) \quad (9)$$

$$\stackrel{a_{t=0} \neq a_{t=T}}{=} L(F_{t=T}, F_{t=0}) \times \ln\left(\frac{a_{t=T}}{a_{t=0}}\right) \quad (10)$$

where  $L(F_{t=T}, F_{t=0})$  is the logarithmic mean of  $F$  values at times  $t = 0$  and  $t = T$ . These terms contain no residuals, therefore it can be shown that the overall improvement in the device efficiency due to improvements in individual sub-efficiencies is equal to the sum of these improvements in individual sub-efficiencies:

$$\Delta a + \Delta b = \Delta F \quad (11)$$

To document historical improvements in LED device performance accurately, we need data on all sub-efficiencies for the selected device architectures and periods covered. However, the scope of data reporting in scientific literature and industry publications is typically limited to selected metrics of interest, rather than the full ensemble of sub-efficiencies that determine the overall device performance. For this reason, our data collection efforts were supplemented by performance calculations for individual sub-efficiencies where possible and necessary. Of the device sub-efficiencies, those related to the emission spectrum were computed from the spectral data often reported in LED device specifications. In particular, we used the `colour-science` package for Python[11] to calculate

the luminous efficacy of radiation, colour rendering performance and luminous efficacy of radiation of phosphor down-conversion of blue light on the basis of available LED emission spectra. This approach allowed us to quantify the improvements related to phosphor development in LEDs.

## 2.4 Manufacturing Cost Model

### 2.4.1 Our Approach to Cost Modeling

The model structure is generally based on the 2012 LEDCOM cost model, but we expand it significantly both in scope and in its ability to capture historical trends. The model captures three historical time periods corresponding to different “eras” in LED manufacturing: the early period of the first high-power white LEDs around 2003, the period of accelerating consumer adoption of LED lighting around 2012, and the most recent period around 2020, the year of our main data collection efforts. For each of these three years, the most prevalent manufacturing equipment was identified through industry periodicals, archived website data from the *Internet Archive*, and expert interviews. Because the architecture of LED chips has changed significantly since the introduction of the first commercial devices in 1996, three different chip architectures were initially considered in the model: classical chips, flip chips, and chip-scale package flip chips. The details of the manufacturing process for each architecture were collected from the scientific literature, textbooks and relevant patents. In addition, two LED life cycle analyses [12][13] were used to validate the model structure and extract some of the necessary quantitative model inputs. These studies captured a large number of LED manufacturing process steps and included the details on the use of metals, chemicals and electricity for each manufacturing step.

The aggregate result of the cost model is the manufacturing cost per LED package for each of the three years considered, which includes all costs associated with producing the chip, including running costs of the factory. Costs associated with research and development, administrative overhead of the manufacturer or other investment costs are not considered. We also note that the purpose of our cost model is not to give specific estimates of LED manufacturing cost for a factory of any size, specific geographic location or total annual manufacturing volume. It instead assumes an hypothetical factory with an assumed location in the United States and associated overhead costs related to the operation of the factory. It also assumes the use of the most up-to-date equipment for that year. Even with these simplifying assumptions, the model reasonably identifies the impact that changes in single process steps can have on the total LED manufacturing cost. An important limitation of our cost modelling efforts is that, even though the model captures three different chip architectures in its structure, in the present study we were able to collect, estimate and present the full set of quantitative inputs and outputs only for the classical chip architecture of low- to mid-power devices. Populating the model with data for the remaining two architectures requires access to proprietary industry information, which we have not been able to get thus far.

The cost model we developed relies on a cumulative approach to yielded cost[14]. In this approach, the yielded cost of process step 1 is defined as the ratio between the total cost of step 1  $C_1$  and the yield of step 1  $Y_1$ :

$$C_{Y_1} = \frac{C_1}{Y_1}, C_{Y_2} = C_{Y_{2 \rightarrow 3}} - C_{Y_1} = \frac{C_1(1 - Y_2) + C_2}{Y_1 Y_2}, C_{Y_3} = \dots \quad (12)$$

This cost metric is cumulative by definition, thus

$$\sum_i C_{Y_i} = \frac{\sum_i C_i}{\prod_i Y_i} \quad (13)$$

Yielded cost per step is dependent on the step order and blind to downstream information [14].

### 2.4.2 Structure of the Model

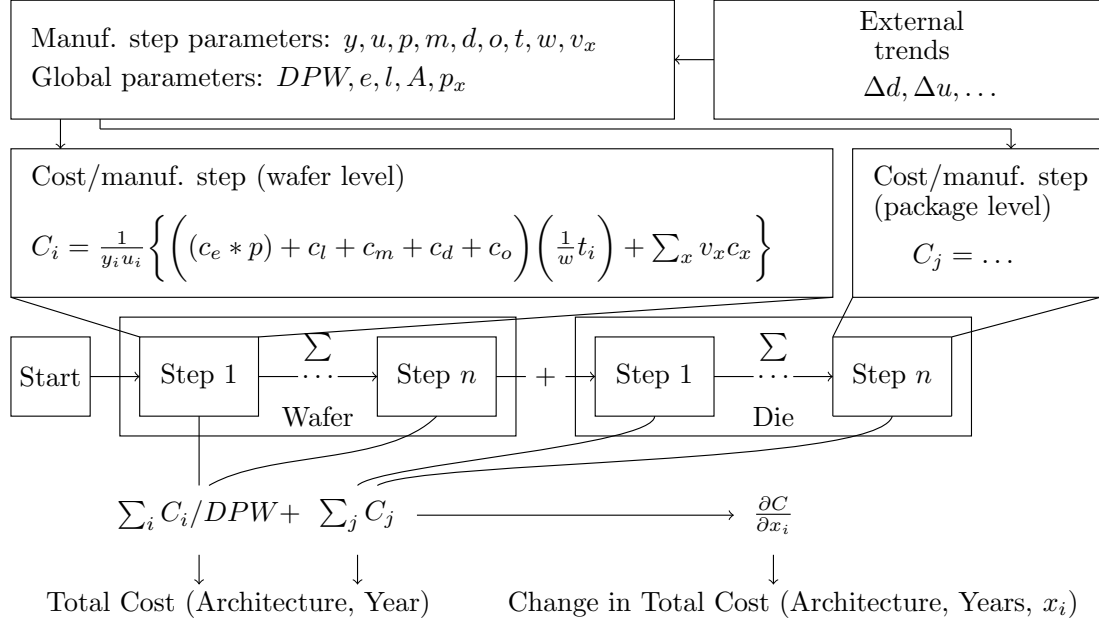


Figure SI1: Schematic diagram of the cost model showing inputs to each step and computational steps leading to the cost model outputs. For the description of cost variables, see definitions for Eq. (SI6). For the computation of total cost, see Section 2.4.4. For the computation of changes in total cost, see Section 2.5.

The cost model adapted for this publication is a microeconomic manufacturing cost model. Within the timeframe and scope laid out in the main publication, it returns the total manufacturing cost of phosphor converted warm white light-emitting diode packages. In this computation, it considers the main economic factors associated with operating and maintaining manufacturing equipment. It does not consider costs associated with research and development or those associated with the construction of manufacturing facilities. It considers market trends through their effect on manufacturing parameters.

A schematic diagram of the cost model is presented in Fig. SI1. The cost model is process step-based. It is split between the two stages of the manufacturing process: the first stage combining operations at the wafer level, followed by the LED packaging stage. The model takes as inputs parameters specific to individual manufacturing process steps ("*manufacturing step parameters*") and parameters affecting all manufacturing steps ("*global parameters*"). The cost for each process step is then computed. The cost model returns the costs of individual manufacturing steps as well as the total manufacturing cost. It further considers the yield per step and returns the cumulative yield, the yielded cost per step and the yielded total manufacturing cost.

### 2.4.3 Manufacturing Process Steps by Chip Architecture

Fig. SI2-Fig. SI6 show a simplified rendering of the manufacturing process of three different chip architectures considered in the cost model.



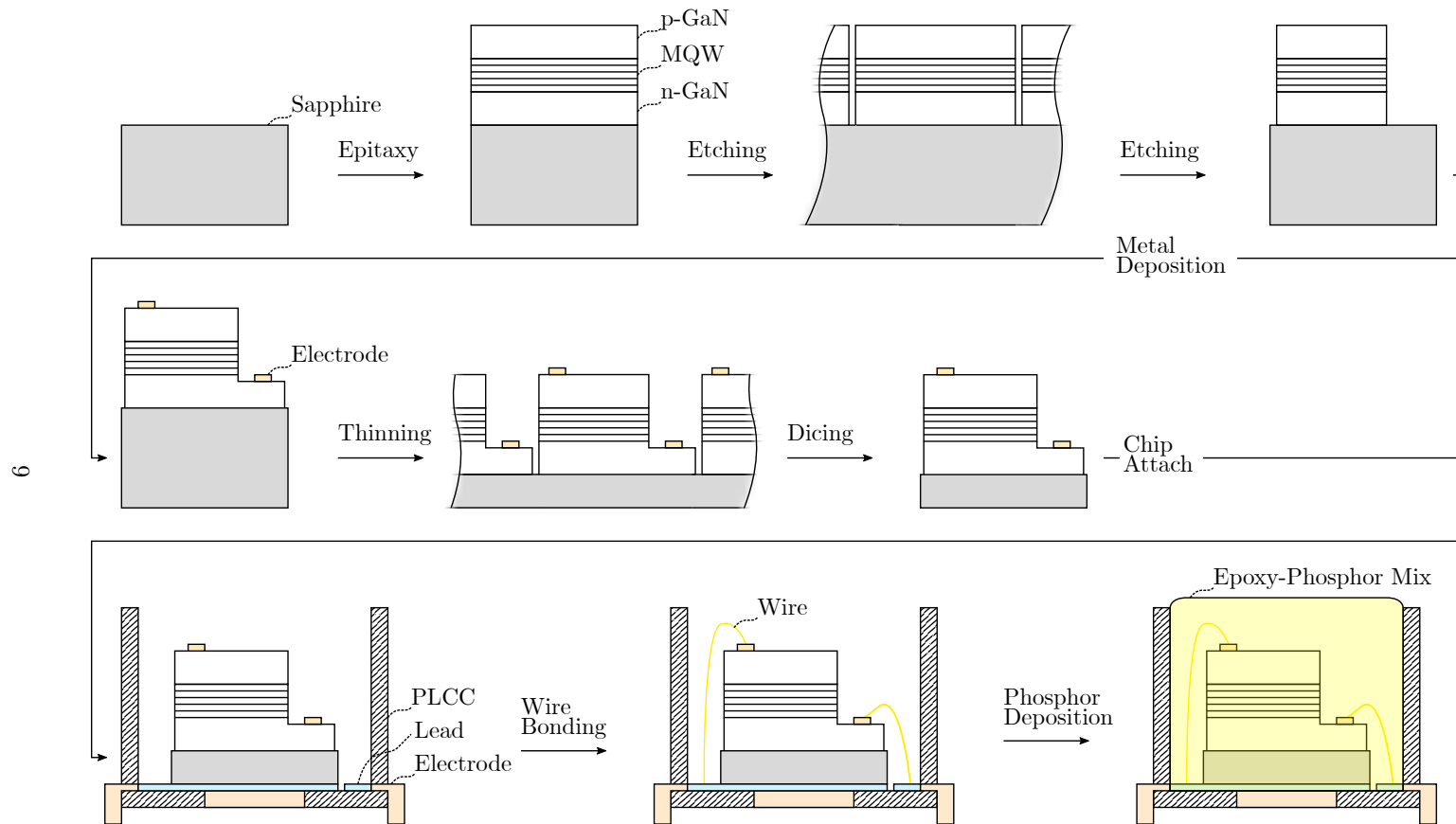


Figure SI2: Manufacturing process for a classical LED package with lateral current spreading, circa 2003. Abbreviations: MQW - multiple quantum well; PLLC - plastic led chip carrier.

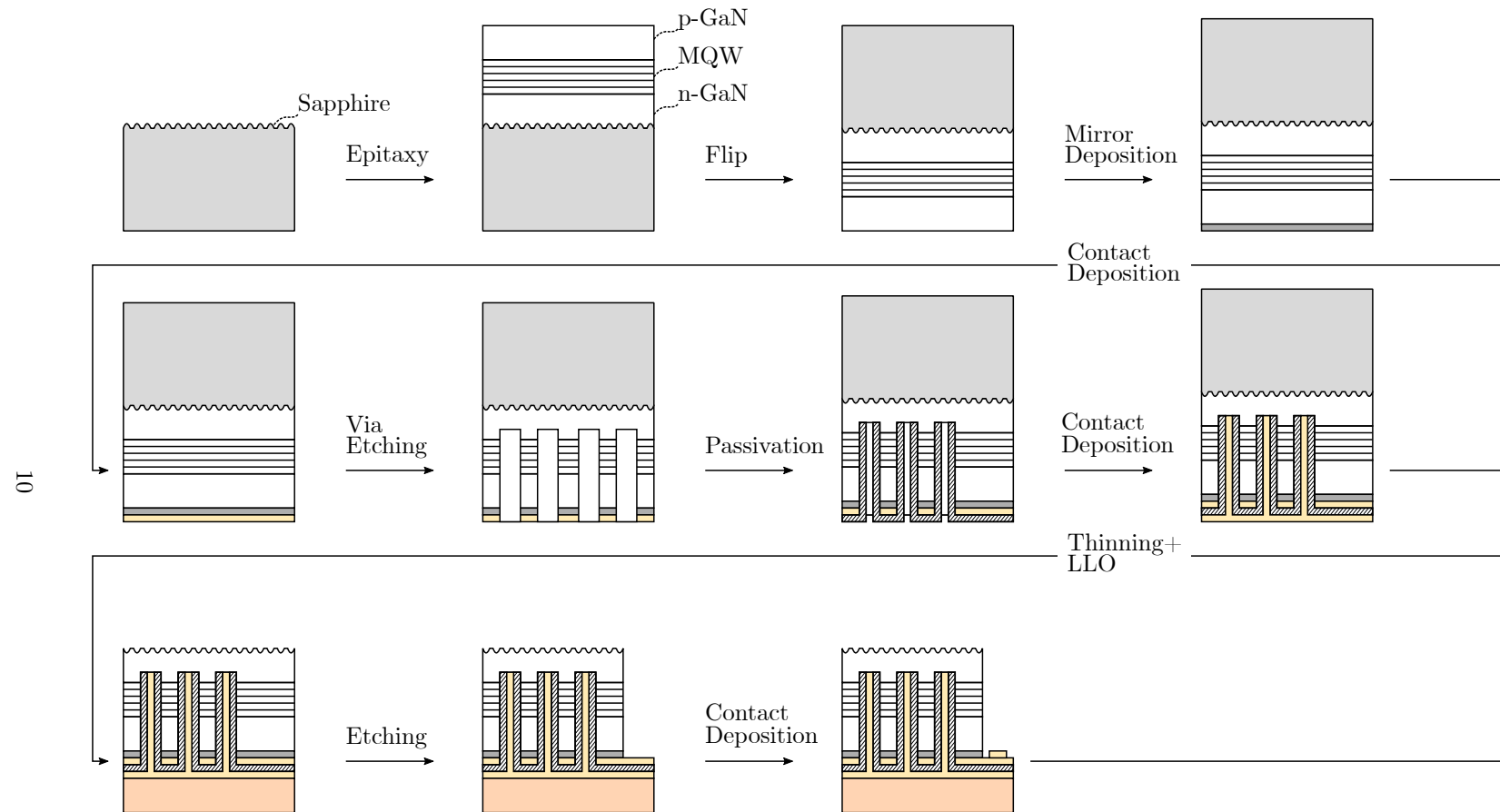


Figure SI3: (1/2) Manufacturing process for a vertical thin-film package flip-chip LED chip with vertical current spreading, circa 2012. Abbreviations: MQW - multiple quantum well; LLO - laser lift-off. Continued on next page.

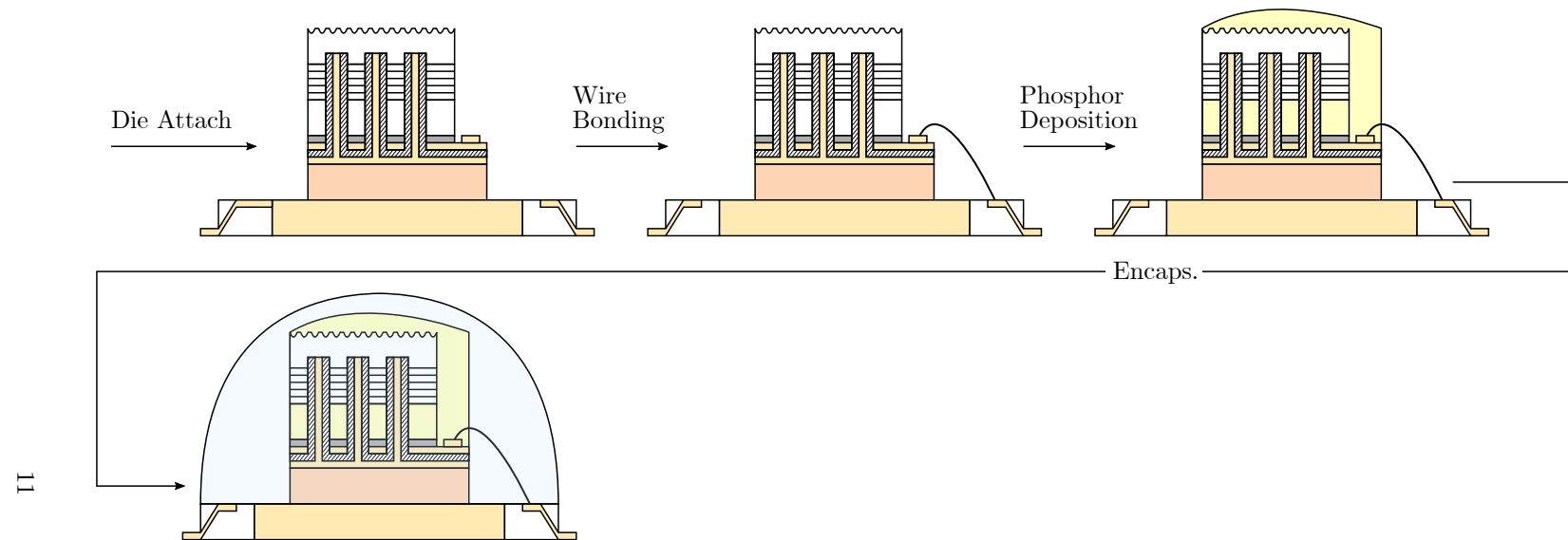


Figure SI4: (2/2) Continued from previous page. Abbreviations: Encaps. - encapsulation.

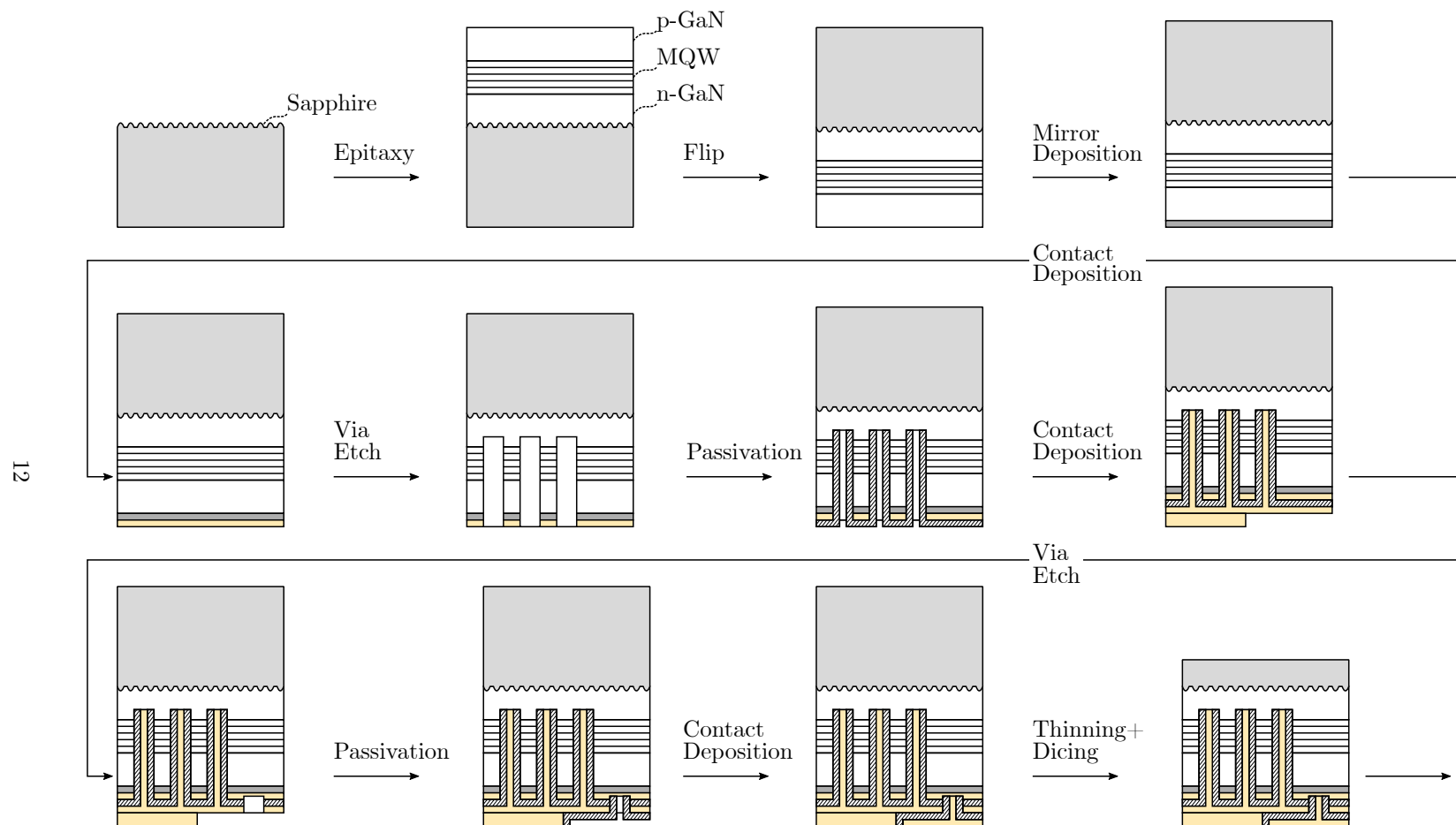


Figure SI5: (1/2) Manufacturing process for a chip scale package flip-chip LED chip with vertical current spreading, circa 2020. Abbreviations: MQW - multiple quantum well. Continued on next page.

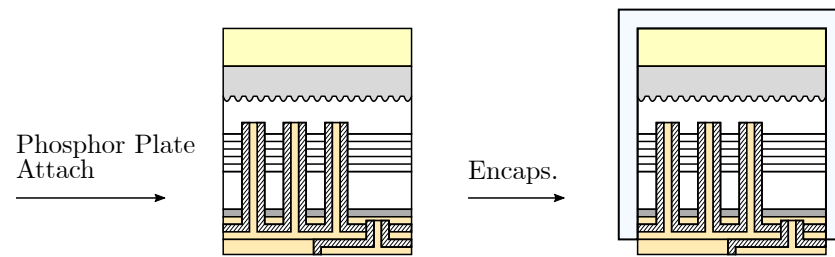


Figure SI6: (2/2) Manufacturing process for a chip scale package flip-chip LED chip with vertical current spreading, circa 2020. Continued from previous page. Abbreviations: Encaps. - encapsulation.

#### 2.4.4 Computation of Manufacturing Cost

The manufacturing process of semiconductor devices can be categorized by the level at which manufacturing process steps are implemented, i.e., either at the wafer level or at the individual chip/package level. The total manufacturing cost per die is thus the sum of the total costs of all wafer processing steps and all die packaging steps.

$$C \left[ \frac{\text{USD}(2020)}{\text{die}} \right] = P_S + C_w + C_p \quad (\text{SI3})$$

where

$P_S$  ... sapphire substrate price per die

$C_w$  ... wafer processing cost per die

$C_p$  ... die processing cost

The total wafer processing cost and total die packaging costs are in turn the sum of all associated process steps.

$$C_w = \sum_i C_i \quad (\text{SI4})$$

$$C_p = \sum_j C_j \quad (\text{SI5})$$

The cost of a single process step  $C_i$  can now be written as

$$C_i \left[ \frac{\text{USD}(2020)}{\text{die}} \right] = \frac{1}{DPW} \frac{1}{y_i} \left\{ \left( (c_e * p) + c_l + c_m + c_d + c_o \right)_i \left( \frac{t_i}{w_i u_i} \right) + \sum_x v_x c_x \right\} \quad (\text{SI6})$$

where the index  $i$  runs over all wafer processing steps, the index  $j$  runs over all die processing steps and the index  $x$  run over all materials.

$DPW$  ... number of functional (i.e., successfully tested) die per wafer

$y$  ... process step yield

$u$  ... equipment utilization (relative to theoretical equipment capacity)

$p$  ... power consumption

$c_e$  ... hourly electricity cost

$c_m$  ... hourly maintenance cost

$c_d$  ... hourly depreciation cost

$c_l$  ... hourly labour cost

$c_o$  ... hourly overhead cost

$t_i$  ... time per run

$w$  ... wafers per run

$A$  ... wafer area

$v_x$  ... volume of material  $x$  per wafer

$c_x$  ... cost of material  $x$  per volume

The number of die per wafer  $D$  depends on the total usable wafer area. The usable area depends on the wafer diameter, the cutting street width between the chips and the exclusion zone at the rim of the wafer.

$$A_{\text{usable}} = A_{\text{wafer}} - A_{\text{cut}} - A_{\text{exclusion}} \quad (\text{SI7})$$

Determining the usable wafer area as a function of these three parameters requires a numerical solution. However, following discussions in the literature [15], we approximate the number of functional die per wafer<sup>2</sup> as

$$DPW = \frac{\pi}{4} \left( \frac{d - 2e}{\sqrt{a} + s/2} \right)^2 - \frac{\pi}{\sqrt{2}} \frac{d - 2e}{(\sqrt{a} + s/2)^2} \quad (\text{SI8})$$

where

$d$  ... wafer diameter  
 $e$  ... wafer edge exclusion zone width  
 $a$  ... die area  
 $s$  ... cutting street width

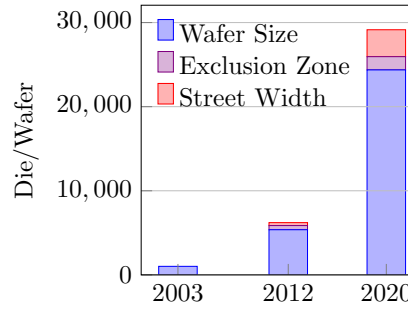


Figure SI7: Number of die per wafer for the different wafer sizes used in different years: (DPW)  $d(2002) = 50\text{mm} \rightarrow 851\text{DPW}$ ,  $d(2002) = 50\text{mm} \rightarrow 5370\text{DPW}$ ,  $d(2020) = 100\text{mm} \rightarrow 26,838\text{DPW}$ . Source: own estimates, based on Eq. (SI8) and the dominant wafer size of the considered year, informed by expert interviews. For detailed statistics on changes in wafer size, compare also Fig. SI8.

Results are plotted in Fig. SI7, showing the increase in die per wafer (DPW) over time. Eq. (SI8) then gives us for the cost of a manufacturing step  $C_i$  in the wafer processing category

$$C_i \left[ \frac{\text{USD}(2020)}{\text{die}} \right] = \left( \frac{\pi}{4} \left( \frac{d - 2e}{\sqrt{a} + s/2} \right)^2 - \frac{\pi}{\sqrt{2}} \frac{d - 2e}{(\sqrt{a} + s/2)^2} \right)^{-1} \times \frac{1}{y_i} \left\{ \left( (c_e * p) + c_l + c_m + c_d + c_o \right)_i \left( \frac{t_i}{w_i u_i} \right) + \sum_x v_x c_x \right\} \quad (\text{SI9})$$

and the cost of a manufacturing step  $C_j$  in the packaging category

$$C_j \left[ \frac{\text{USD}(2020)}{\text{die}} \right] = \frac{1}{y_j} \left\{ \left( (c_e * p) + c_l + c_m + c_d + c_o \right)_i \frac{c_j}{u_j} + \sum_x a v_x c_x \right\} \quad (\text{SI10})$$

where  $c_j$  is throughput<sup>-1</sup>. The total cost is thus

$$C = P_s + \sum_i \left\{ \frac{1}{DPW} \frac{1}{y_i} \left[ \frac{t_i}{w_i u_i} \left( (e * p) + l + m + d + o \right)_i + \sum_x v_x p_x \right] \right\} + \sum_j \left\{ \frac{1}{y_j} \left[ \frac{c_j}{u_j} \left( (e * p) + l + m + d + o \right)_i + \sum_x a v_x p_x \right] \right\} \quad (\text{SI11})$$

<sup>2</sup>often "good die per wafer" in the literature

Note that in keeping with the categorization introduced by the United States Department of Energy (cf. eg. [16]), certain steps from these two categories are reported separately. In the wafer processing category, the epitaxy step is reported separately due to its complexity and the large share of cost carried. In the wafer processing category, the phosphor step is reported separately.

#### 2.4.5 Computation of Yielded Cost

Devices may be damaged or otherwise rendered unusable during the manufacturing process. The ratio between the number of good devices per step and the number of handled devices per step is known as the yield. Optimizing this yield is critical for reducing manufacturing cost [17]. This is because cumulative yield quickly drops as the yield from manufacturing steps with below 100% yield is multiplied. We must thus consider not only the manufacturing cost per process step, but also the cost including the yield [14][18]. While there are different mathematical approaches to including yield, we follow the definition in [14]. We write for the yielded cost  $C_{Y_i}$  of a step  $i$  with associated cost (before considering yield)  $C_1$  and yield  $Y_1$ :

$$C_{Y_1} = \frac{C_1}{Y_1} \quad (\text{SI12})$$

$$C_{Y_2} = \frac{C_1 + C_2}{Y_1 Y_2} - C_{Y_1} = \frac{C_1 + C_2}{Y_1 Y_2} - \frac{C_1}{Y_1} = \frac{1}{Y_1 Y_2} \left( C_1(1 - Y_2) + C_2 \right) \quad (\text{SI13})$$

$$C_{Y_i} = \frac{\sum_{x \leq i} C_x}{\prod_{x \leq i} Y_x} - \frac{\sum_{x < i} C_x}{\prod_{x < i} Y_x} \quad (\text{SI14})$$

If a step is applied more than once, we can conveniently rewrite this in a form suited to computation within the *Excel* worksheet. Assuming step 2 is used twice, we get for the yielded cost of this step an equation of the form

$$C_{Y_2}^{(2\times)} = \left( \frac{C_1 + C_2}{Y_1 Y_2} - \frac{C_1}{Y_1} \right) + \left( \frac{C_1 + 2C_2}{Y_1 Y_2^2} - \frac{C_1 + C_2}{Y_1 Y_2} \right) \quad (\text{SI15})$$

$$= \frac{1}{Y_1 Y_2^2} \left( C_1(1 - Y_2^2) + 2C_2 \right) \quad (\text{SI16})$$

which can be compared to Eq. (SI12) to find a more general form:

$$C_{Y_2}^{(n\times)} = \frac{1}{Y_1 Y_2^n} \left( C_1(1 - Y_2^n) + nC_2 \right) \quad (\text{SI17})$$

It can be shown by induction that the general form of a term for a step  $i > 1$  repeated  $n$  times can be expressed as:

$$C_{Y_{i>1}}^{(n\times)} = \frac{1}{Y_i^{n-1} \prod_{x \leq i} Y_x} \left( nC_i + \sum_{x < i} C_x(1 - Y_i^n) \right) \quad (\text{SI18})$$

This cumulative approach to yielded cost is different from the approach taken in the original *LED COM* model. It uses what in the literature is described as an "*itemized approach*" to yielded cost [14]. In this approach, the yielded cost of a single process step  $f$  is described as

$$f_{\text{single}} = \frac{i + s}{y} \quad (\text{SI19})$$



where

$i \dots$  material cost of previous step  
 $s \dots$  step cost

For process steps that are performed more than once, a series expression is used

$$f_{\times 2} = \frac{\frac{i+s}{y} + s}{y} \quad (\text{SI20})$$

$$f_{\times n} = \frac{i + s(1 + y + y^2 + \dots + y^{n-1})}{y^n} \quad (\text{SI21})$$

This itemized approach serves as a convenient approximation, but its cumulative contributions do not equal the total yielded cost of the entire manufacturing process

$$f_{\text{total}} = \frac{\sum_i^n s_i}{\prod_i^n y_i} \neq \sum_i^n f_i \quad (\text{SI22})$$

where  $n$  is the total number of steps. This is due to the approximation introduced through the series approximation in Eq. (SI21).

#### 2.4.6 Example of Input Data Considered: Sapphire Wafers

Sapphire wafers form the substrate on which all other layers of the light-emitting diode are grown. Being transparent to radiation in the visible spectrum, it is not removed after growth in the Classical architecture or the Thin-Film Flip-Chip architecture. In the Vertical Thin-Film architecture, it is removed by means of a laser-lift-off process. Wafers can be either unpatterned or patterned, where the latter has become commonplace by 2020 due to the beneficial properties that microstructures on the surface have on layer growth [19] and light-extraction efficiency [20]. The price of sapphire substrates has decreased significantly since the year 2000, as shown in the bottom panel of Fig. SI8. This can be attributed not only to the lighting industry, but more importantly to increased supply as a result of increased demand from electronics manufacturing [21], where sapphire glass is used to protect screens and sensor interfaces from scratches [22]. Wafer sizes used in manufacturing have also increased, due to the favourable economics of large wafer processing. The market has been dominated by U.S.-based *Rubicon Technology* and Russian-based *Monocrystal*. The evolution of sapphire wafer prices and diameters used in LED manufacturing over the years is shown in top panel of Fig. SI8.

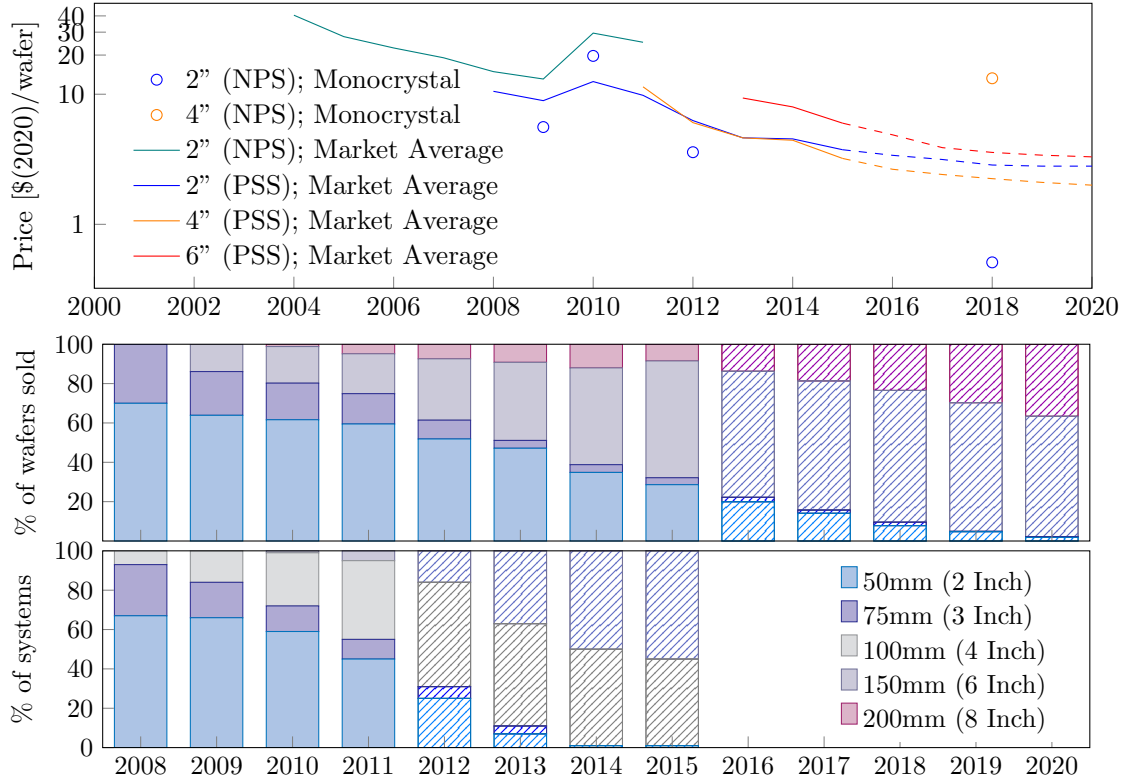


Figure SI8: Top: Historical data for sapphire substrate prices of different surface properties and diameters. Shown is data for polished surface (NPS) and patterned substrates (PSS). *Monocrystal* denotes the Russian manufacturer of the same name. Dashed lines are projections from the previous year. Sources: [23][24][21]. Bottom: Prevalence of sapphire wafer size used in the manufacturing of light-emitting diodes. Hatched bars are projections given by the sources. Sources: [25][26][21]

#### 2.4.7 Preliminary Sensitivity Analysis

A sensitivity analysis of the cost model has been performed using parameter variations listed in table Table SI2. The amount of parameter variation was chosen to encompass the identified range of parameter values in different manufacturing setups for each considered year. As an example, the lower range in the variation for the price of metals used in the model (+50%,-0%) was chosen because the prices quotes from the United State Geological Survey price database. Industry metals are not sold below the price of the raw material and often the markup is small compared to the price of the material. The upper range was chosen because a survey of industrial metal suppliers for semiconductor manufacturing showed that the largest markup was below 50%. The results of the analysis are shown in Fig. SI9. The cost model is generally more sensitive to the variation in parameters at smaller wafer diameters. The most sensitive parameters are global parameters, such as yield or average equipment throughput.

Table SI2: Cost model sensitivity analysis parameter list. The results of the sensitivity analysis for the parameters in this table are presented in Fig. SI9.

<i>Parameter</i>	<i>Unit</i>	<i>2003</i>	$\pm[\%]$	<i>2012</i>	$\pm[\%]$	<i>2020</i>	$\pm[\%]$	Source
Cleanroom Cost	USD/m <sup>2</sup>	3000	+16,-16	3000	+16,-16	3000	+16,-16	[27][28] [29][30]
Person-hour	FTE	100%	+50,-50	100%	+50,-50	100%	+50,-50	I
Equip. Discount	% of USD	0%	+25,-25	0%	+25,-25	0%	+25,-25	I [31]
Overall Yield	%	100%	+25,-25	100%	+25,-15	100%	+25,-25	I, [32][33] [34][28]
Inspec. Yield Savings	%/inspec.	0.5%	+80,-80	0.5%	+80,-80	0.5%	+80,-80	[35]
Overall Throughput	UPH or h <sup>-1</sup>	100%	+50,-50	100%	+50,-50	100%	+50,-50	Datasheets
Wafer Diameter	mm	100	+0,-50	150	+33.3,-33.3	200	+0,-25	I and Fig. SI8
Edge Exclusion	mm	7	+0,-50	5	+40,-0	5	+40,-20	[36][37] [38][39]
Cutting Width	$\mu\text{m}$	100	+50,-25	75	+33.3,-20	20	+300,-50	[40][41] [42][43]
Metal Prices	USD/kg	100%	+50,-0	100%	+50,-0	100%	+50,-0	Datasheets
Electricity Price	USD/kWh	100%	+50,-50	100%	+50,-50	100%	+50,-50	[44][45]
Saph. Subst. Price	USD	40	+12.5,-12.5	10	+100,-20	3	+66.6,-33.3	Fig. SI8
Phosphor Prices	USD/g	100%	+50,-50	150	+0,-0	200	+0,-0	I, [46][47]

Note: The units for the values in columns *2003-2020* are indicated in the column *Units*. If values in columns *2003-2020* are instead given in %, this indicates that the parameters were varied by a set percentage from their respective model baselines. Abbreviations: FTE - full-time equivalent; UPH - units per hour; Equip. Discount - equipment discount (sales rebate for large purchases); Inspec. Yield Savings - yield savings from inspection (early detection and alleviation of issues in the manufacturing workflow).

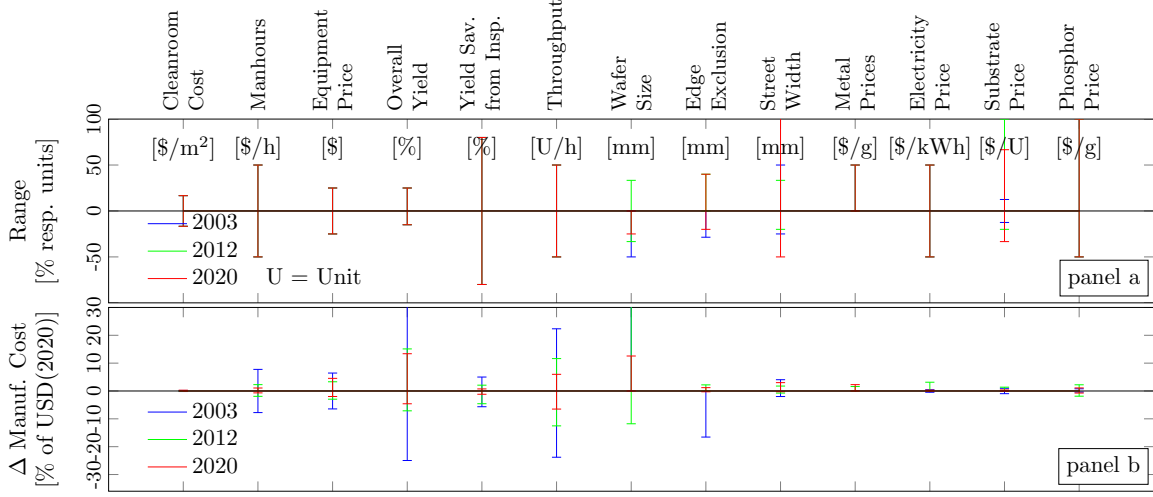


Figure SI9: Sensitivity analysis for selected cost model parameters. Panel a represents the tested range of variation of parameters indicated on horizontal axis along with their respective measurement units, as represented in Table SI2. Panel b shows the resulting range of variation in the manufacturing cost. Ranges are represented for three years considered in the cost model, where corresponding data is available, by whiskers of the following colour: 2003 – blue, 2012 – green, 2020 – red. Note the overall trend of decreasing sensitivity to cost model parameters as the number of die per wafer increases over time. Abbreviations: resp. - respective; yield sav. from insp. - yield savings from inspection.

## 2.5 Computation of Contribution of Individual Variables

To quantify the drivers of changes in manufacturing cost or device performance among many contributing factors, one would need to identify the magnitude of contribution to these changes made by single variables in equations Eq. (SI6) and Eq. (SI10). Mathematically, given a function  $C$  which describes the manufacturing cost or performance function of a device at time  $t$ ,

$$F = ab + cd \quad (\text{SI23})$$

and input variables  $a, b, c, d$ , we are looking for the contribution  $\Delta F_a$  made by a single variable  $a$  to the total change in the function value  $\Delta F$  between points  $t_0, t_1$  such, that

$$\Delta F = F(t_1) - C(t_0) = \sum_{i=a, \dots, d} \Delta F_i \quad (\text{SI24})$$

The infinitesimal contribution to the total function value by the infinitesimal change in an input variable is defined through the total differential of the function as

$$dF(x_1(t), x_2(t), \dots) = \sum_i \frac{\partial F}{\partial x_i} \frac{dx_i}{dt} = \sum_i \frac{\partial F}{\partial x_i} \Delta x_i \quad (\text{SI25})$$

where  $x_i$  is an input cost variable. The contribution of the change  $\Delta x_1$  in variable  $x_1$  to the total function value  $F$  over the period  $t_0 < t < t_1$  is then

$$\Delta F_{x_1} = \int_{t=t_1}^{t_2} \frac{\partial F}{\partial x_1} \frac{dx_1}{dt} dt \quad (\text{SI26})$$

However, data on the input variables is not available in continuous time. Disaggregating the contribution of single variables to the change in the cost or performance is thus not straightforward in our model. This problem does not arise in cost models which compute cost changes directly, such as [48] [49]. In our work, we propose to address this problem by following an approach developed by Kavlak et al. [50]. For the detailed derivation, we refer to this publication.

The function  $F$  as a function of a vector of input model variables  $\vec{r} = (r_1, r_2, \dots)$  is defined as

$$F(\vec{r}) = F(r_1, r_2, \dots) = \sum_i F_i \quad (\text{SI27})$$

where

$$F_i(\vec{r}) = F_i^0 \prod_w g_{iw}(r_w) \quad (\text{SI28})$$

Using logarithmic differentiation, the integral from Eq. (SI26) can be rewritten as

$$\Delta F_x = \int_{t=t_0}^{t_1} F(t) \frac{\partial \ln F}{\partial x} \frac{dx}{dt} dt \quad (\text{SI29})$$

where for  $F(t)$  a constant  $F(t) \approx \tilde{F}$  can be chosen such that  $\Delta F_{x_i} = \Delta F$ . In practice, this constant value can be approximated through the geometric and arithmetic means  $\tilde{F} \approx \frac{2}{3} F_i^{\text{geo}} + \frac{1}{3} \overline{F}_i$ . The contribution of a single cost model variable  $r_z$  can then be written as

$$\Delta F_z(t_1, t_2) \approx \sum_i \tilde{F}_i \ln \frac{g_{iz}(t_2)}{g_{iz}(t_1)} \quad (\text{SI30})$$

We use this approach to estimate the effect of individual innovations and spillovers on LED device performance, as discussed in section 4.3 and shown in Figure 5 in the main article. Due to time constraints, we leave the quantification of the impact of different drivers of cost reductions with this methodological approach for our future work.

### 3 Additional Results

This section provides additional background and details for the results of our study presented in the Results section in the main text.

#### 3.1 Historical Progress in Sub-Efficiencies

The historical progress in the different sub-efficiencies contributing to overall efficiency (lamp efficiency) is shown in Fig. SI10. Context for figure panels is provided below:

**Panel A1:** Device forward voltage at a test current of  $I=350\text{mA}$ . The physical limit for a blue light wavelength of 450nm without electric pumping is shown for reference. Data points for devices released in 2020 by various manufacturers are shown in an inset plot.

**Panel A2:** Efficiency droop at the test current of  $I=350\text{mA}$ .

**Panel B1:** Internal quantum efficiency, for different chip architectures, by type of measurement used. Note that the artifact in the DOE Average around 2013 is due to a change in definition for internal quantum efficiency laid out in [51]. Measurement methods: PL - Photoluminescence[52], EL - Electroluminescence[53]; ABC Model[54], Ideality Factor[55]. “Not reported” denotes data points where the IQE measurement technique was not reported. Whiskers indicate reported ranges, where applicable.

**Panel B2:** Light extraction efficiency for different chip architectures, by type of specific technology used to improve light-extraction efficiency. The source of data points is shown for reference: simulation - ray-tracing computer simulation; experimental (absolute) - light-extraction efficiency given directly; experimental (relative) - relative improvement over baseline chip architecture given. Abbreviations: TFFC - Thin-Film Flip-Chip; FC - Flip-Chip; CSP - Chip-Scale Package; ITO - Indium Tin Oxide; ZnO - Zinc Oxide; PSS - Patterned Sapphire Substrate; electr. - electrode; text. - textured.

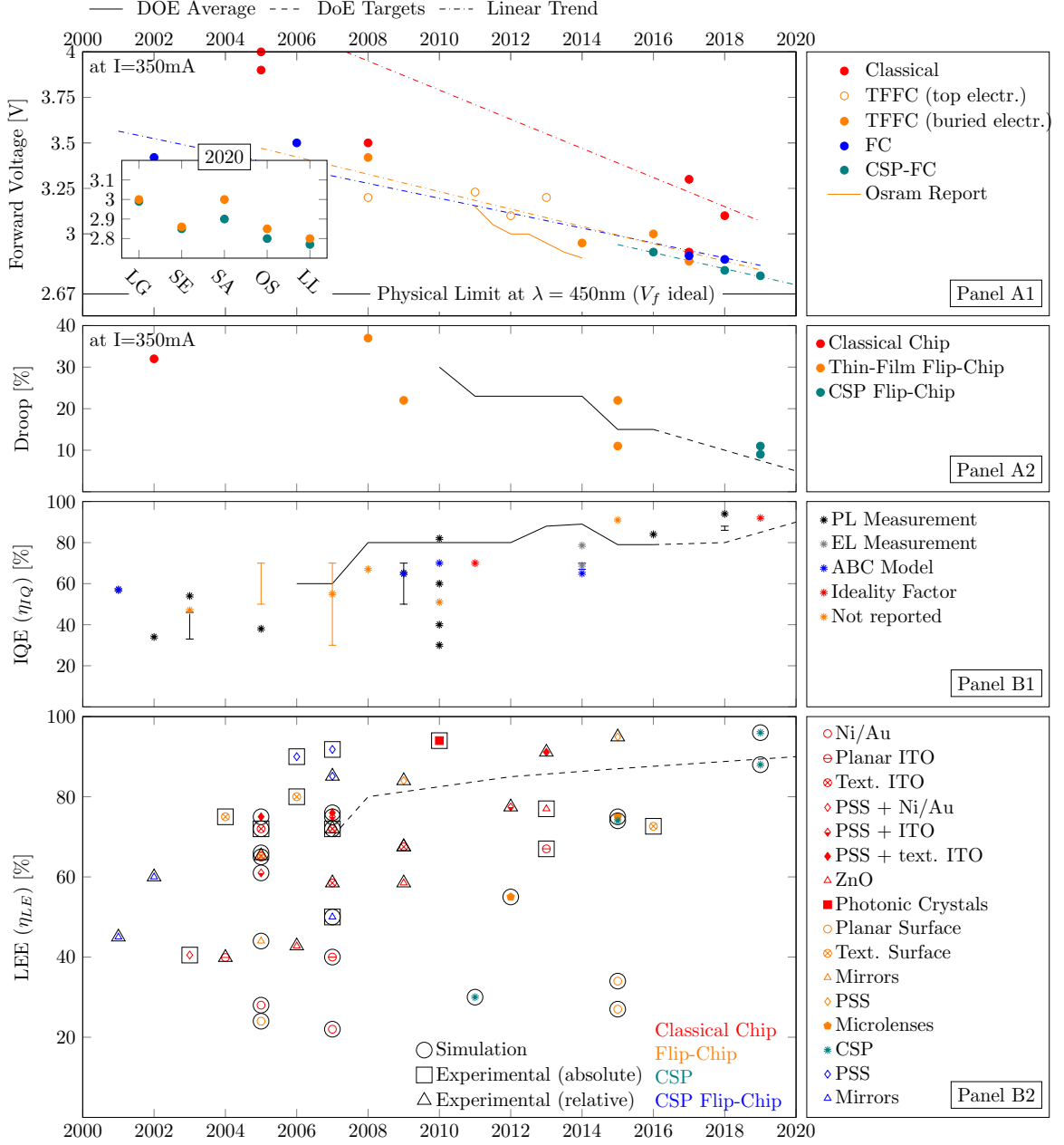


Figure SI10: Historical improvements in light-emitting diode technology. Panels A1-A2 show they key metrics used to compute forward voltage efficiency  $\eta_{Vf}$  and droop efficiency  $\eta_{droop}$ . Panels B1-B2 show the sub-efficiencies internal quantum efficiency  $\eta_{IQ}$  and light extraction efficiency  $\eta_{LE}$ . Source: own synthesis of data from the full list of sources provided in Section 4. Data on average device performance adapted from U.S. Department of Energy (DOE) Reports [56][57][51][58][59] and an Osram company report [60].

## 3.2 LED Innovations

### 3.2.1 Non-Phosphor-Related

Table SI3 summarizes LED innovations and technology and manufacturing process improvements identified in this study as affecting key white LED sub-efficiencies. Note that phosphor-related LED innovations affecting consumer experience metrics, along with spectral efficiency, are presented separately in Table 1 in the main publication and discussed in detail in Section 3.2.2.

### 3.2.2 Phosphor-Related

This section provides additional details for phosphor-related LED innovations identified in this study as affecting both spectral sub-efficiencies and consumer experience metrics.

**3.2.2.1 YAG and YGAG Phosphors** Prior to Nakamura’s invention of highly efficient blue LEDs in the 1990s, Japan’s Nichia Corporation had not sold commercially successful semiconductor products, instead specializing in phosphors for cathode ray tubes (CRT) and fluorescent lamps [74]. Nevertheless, extensive firm expertise in this area helped Nichia’s Yoshinori Shimizu formulate the principles of using CRT phosphors to convert blue light from Nakamura’s LEDs into white light in 1994 [75][76]. By 1996, Shimizu and his colleagues developed [77][78] the first practical LED application of a well-known Yttrium Aluminium Garnet (YAG) CRT phosphor activated with cerium [79], enabling the first commercial white LED products manufactured and sold by Nichia since late 1996 [80][76].

Importantly, the YAG phosphor does not exhibit the spectral properties desirable in general illumination applications (see Figure 6 in the main article). An early solution to this problem, which was first discovered in the late 1967 [81] and suggested for LEDs by the same team at Nichia in 1996 [80][78], was to use the gadolinium-doped red-shifted YAG phosphor (YGAG). Used in combination with red-emitting sulfide phosphors, by 2002 it helped bring to the market the first generation of warm white light LED products, e.g., those produced by Lumileds [82]. However, sulfide phosphors led to accelerated deterioration of sensitive parts of LED devices and became less efficient as operating temperatures increased. New chemically stable and non-toxic red phosphors were needed.

**3.2.2.2 258, SLA and SALON phosphors** In 1997, Hubert Huppertz and Wolfgang Schnick, working at the University of Bayreuth in Germany, synthesized the first compound in a new class of rare earth nitridosilicate materials [83] later dubbed “258” due to a proportion of elements in its chemical formula. The luminescent properties of these materials were identified by the Schnick’s group, by then at Ludwig-Maximilians University of Munich, in 2000 [84] after a suggestion made to Schnick at a conference following earlier reports of good luminosity properties of europium-doped compounds [85]. U.S.-based LED manufacturer Lumileds applied for a patent for the first class of red LED phosphors based on the 258 nitridosilicate chemistry in 2002 [86]. The first use of the 258 phosphor in a commercial “Luxeon” LED package was then reported in a joint publication co-authored by inventors from Lumileds and researchers from the Schnick’s group in 2005 [87].

Further efforts in LED phosphor development were directed towards synthesizing a red narrow-band phosphor. Narrow LED emission peak widths yield the highest luminous efficacy of radiation, as in this case less light is emitted in the far-red range of the spectrum in which the human eye is not very sensitive. After synthesizing several narrow-band phosphors emitting in yellow [88] and cyan [89], the Schnick’s group identified the local cubic cation coordination structure of the cyan phosphor compound as the reason for its narrow band width [90]. A search for a structurally analogous nitride compound with the narrow red instead of the cyan emission was undertaken. After several unsuccessful attempts, the sought-after cuboidal nitride compound was found in a 2008 publication led by Francis DiSalvo [91]. Based on information provided in this work, Schnick and colleagues



synthesized and studied the spectral properties of a new narrow band red SLA phosphor in 2013 [92][93][94]. The material was introduced in commercial LED devices by Lumileds in 2015 [95].

The most recent red narrow-band phosphor innovation included in Table 1 and Figure 6 in the main article, indicated as SALON, has been under development during the late 2010s by a group of Austrian and German researchers that included Huppertz, the discoverer of the “258” material, working in collaboration with Osram, another major LED manufacturer [96][97][98]. The first U.S. patent application for this phosphor was filed in 2017 [96]. The SALON phosphor is a derivate of the SLA phosphor. Therefore, it is the only innovation related to consumer experience metrics identified in our study that seemingly not involved technology spillovers.

**3.2.2.3 PFS Phosphor** Down conversion with ultra-narrow-band phosphor can achieve the highest spectral efficiency. However, few such phosphors have been identified, with even less exhibiting desirable material properties such as thermal stability [99]. The first commercially successful ultra-narrow-band red phosphor was developed by General Electric (GE). It is based on a potassium fluorosilicate (PFS) compound activated with manganese ions. Its luminescence was first recorded by Adrian Paulusz at GE in 1972 [100]. In the early 2000s, while searching for potential new LED phosphor materials for GE’s lighting business at GE Lumination, Emil Radkov rediscovered Paulusz’s findings in the literature. Following extensive research on PFS chemical synthesis and material properties conducted in collaboration with the University of Sofia in Bulgaria, Radkov’s Alma Mater, the PFS phosphor had been under development at GE since 2005 [101][102]. This work, supported by public funding from the U.S. Department of Energy (DOE) Solid-State Lighting program [103], resulted in a series of critical improvements in the PFS phosphor properties [104][105], eventually enabling its commercialization under the “TriGain” brand in 2015 [106][107][108].

**3.2.2.4 Quantum Dots for Light Down-Conversion** Quantum dots (QD) are semiconductor nanocrystals whose quantum size effects make QDs behave as “artificial atoms”. Semiconductor quantum dots were first synthesized in the Soviet Union in 1981 [109] and at Bell Labs in the U.S. in 1983 [110]. Luminescent properties of quantum dots were first empirically observed in 1984 [111] and extensively studied in the early 1990s. The key feature of QD luminescence discovered in those studies is that its colour is determined by the QD particle size, making it possible to create pure monochromatic blue, green and red light sources just by tuning the QD size. The first application of QDs in LEDs was reported in 1994 in an electroluminescent hybrid QD-polymer LED. However, this LED type could not be used in general illumination due to its very low luminous efficacy. An alternative application of QDs as a kind of a “phosphor” for light down conversion from an LED light source was proposed in the early 2000s as part of the U.S. Department of Energy (DOE)-funded “A Revolution in Lighting” project at Sandia National Laboratory [112]. This concept was successfully demonstrated by Sandia researchers on a commercial LED in 2003 [113][114] and was swiftly taken up and advanced further by a group in Taiwan [115][116]. The first commercial application of QDs in an LED lamp was brought about by a collaboration between an MIT-born startup QD Vision and the U.S.-based luminaire manufacturer Nexxus Lighting in 2009 [117], [118]. However, rapid advances in the spectral and conversion performance of down-conversion phosphors and high manufacturing cost of quantum dots resulted in the discontinuation of this product. After finding market success in display backlighting first demonstrated by Samsung in 2010 [119] and commercialized by QD Vision in Sony television sets in 2013 [118], QDs returned to the general lighting market in products offered by Lumileds [120][121] around 2017 and Osram in 2019 [122] in the form of mid-power LED packages that combined QDs with traditional phosphors for light down conversion.

Table SI3: LED innovations and technology improvements affecting key white LED device sub-efficiencies. The table includes innovations and technology improvements affecting forward voltage efficiency, light extraction efficiency, internal quantum efficiency, and light conversion efficiency. For a list of innovations affecting spectral efficiency, see Table 1 in the main article.

Forward Voltage Efficiency (VFE) $\eta_{Vf}$				
<i>Year</i>	<i>Innovation</i>	<i>Area of Improvement</i>	<i>Spillover</i>	<i>Source</i>
1999	Indium Tin Oxide Current spreading layer	Contact resistance	Yes	[61]
1998	Digitated electrodes	Contact resistance	No	[62]
Ongoing	Epitaxy improvements and better doping	Polarization and bulk resistance	No	I
1998	Silver p-Contacts	Contact resistance	No	[63]
Light extraction efficiency (LEE) $\eta_{LE}$				
<i>Year</i>	<i>Innovation</i>	<i>Area of improvement</i>	<i>Spillover</i>	<i>Source</i>
< 2003	Optimization for cavity effects	Reduces self-interference of quantum well	No	I, [64]
1993	Chip surface randomization	Total reflection and absorp- tion	No	I, [65][66]
1993	Thin-film chip architecture	Absorption	No	I, [66]
1996	Patterned sapphire substrate	Total reflection and absorp- tion	Yes	I, [67]
Ongoing	Chip design for high LEE	Total reflection and absorp- tion	No	I, [68]
~2000	Silver p-contacts	Absorption	No	I, [63]
Internal quantum efficiency (IQE) $\eta_{IQ}$				
<i>Year</i>	<i>Innovation</i>	<i>Area of improvement</i>	<i>Spillover</i>	<i>Source</i>
1994	Double heterostructure	Higher Radiative recombina- tion probability	No	[69]
1996	Multiple quantum well	Higher Radiative recombina- tion probability	No	[70]
Ongoing	Active region Doping	Radiative recombination prob- ability	No	I, [4]
Ongoing	Epitaxy Improvements	Radiative recombination prob- ability	No	I
Ongoing	Chip architecture Improvements	Radiative recombination prob- ability	No	I
Light Conversion efficiency (CE) $\eta_C$				
<i>Year</i>	<i>Innovation</i>	<i>Area of improvement</i>	<i>Spillover</i>	<i>Source</i>
Ongoing	Lower current density	Current density	No	I
Ongoing	Epitaxy Improvements	Charge distribution Defect density	No	I, [71]
Ongoing	Chip architecture improvements	Charge distribution Defect density	No	I, [72]
< 2017	Defect getting underlayer	Defect Density	No	I, [73]

Note: *Year* column indicates the first instance of application of corresponding invention in white LEDs. 'Ongoing' indicates improvements that are incremental in nature and have been ongoing since the earliest days of LED manufacturing, with no individual breakthroughs identified. *Spillover* column indicates if the innovation involved technology spillovers. *Source* column indicates the source of information about the innovation or improvement, with 'I' indicating expert interviews as such a source.

### 3.2.2.5 Spectral Data for Identified LED Phosphor Innovations

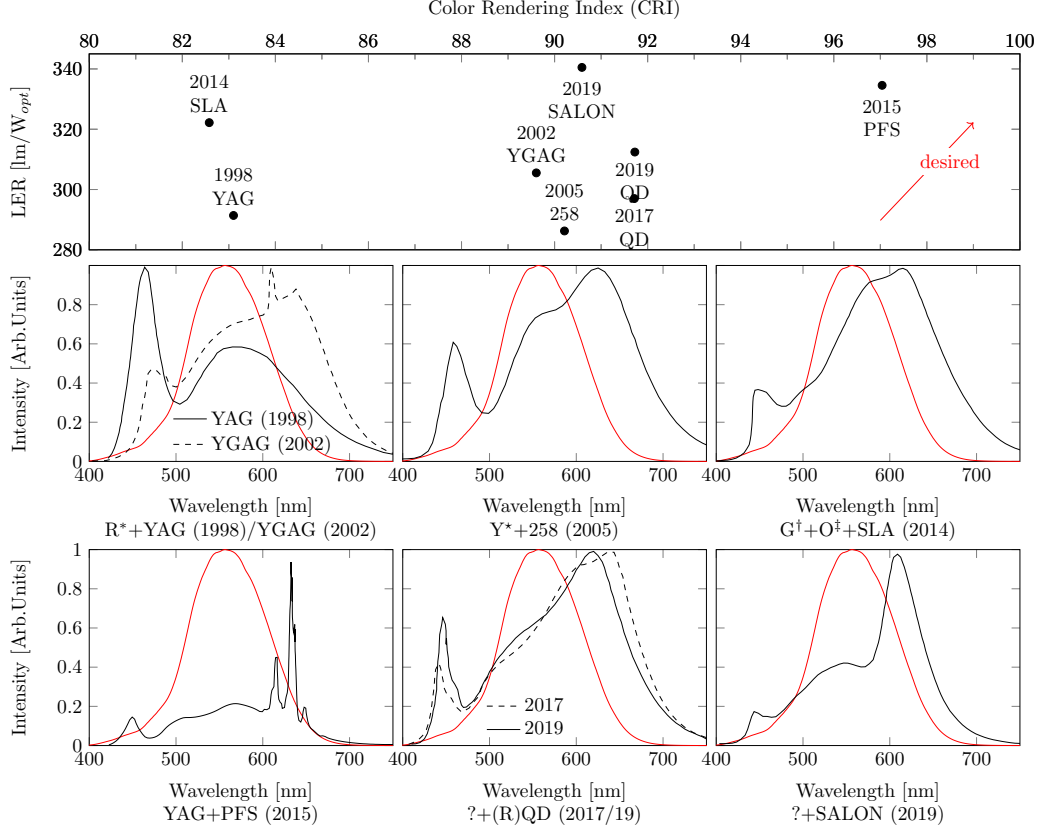


Figure SI11: Spectral data and additional consumer experience metrics for the earliest identified representative white LED products with published spectral data, shown in Figure 6 in the main article, that used phosphor innovations listed in Table 1 in the main article, each indicated by the phosphor label and spectral data publication year. Top panel: Luminous efficacy of radiation (LER) and colour rendering index (CRI) of white LED devices represented in Figure 6 in the main article. The desirable direction of improvements towards higher luminous efficacy at higher CRI is indicated by a red arrow. Metrics were calculated from spectral data shown in the two bottom panels using the `colour-science` package for Python [123]. Bottom two rows of panels: Corresponding spectral data. The luminosity function [124], describing the wavelength-dependent sensitivity of the human eye, is shown for reference in red in each panel. Note that peaks or large tails of the device emission spectrum at the far ends of the luminosity function are not desirable, as the photons of the corresponding energy are lost to the human eye and count towards the spectral loss channel. Plot legends indicate the years of publication of the spectral data and phosphor mixtures used in corresponding LED devices, with the following designations for additional phosphor mix components: ? - other parts of phosphor mixture not disclosed, G\* -  $\text{CaSrS:Eu}^{2+}$ , Y\* -  $\beta\text{-SiAlON:Eu}^{2+}$ , G<sup>†</sup> -  $\text{Lu}_3\text{Al}_5\text{O}_{12}\text{:Ce}^{3+}$ , O<sup>‡</sup> -  $(\text{Ba,Sr})_2\text{Si}_5\text{N}_8\text{:Eu}^{2+}$ . Source (top panel): own elaboration based on spectral data. Arb. Units - Arbitrary Units, defined as the ratio of radiation intensity at a wavelength compared to the highest point in the spectrum. Sources: top panel - own elaboration based on spectral data; bottom two panels: adapted from published spectral data for LEDs with the following phosphors: YAG [80], YGAG [82], 258 [87], SLA [93], PFS [106], QD [125][126], SALON [97].

### 3.3 Cost Comparison with Reported Industry Data and DOE Projections

We conducted a comparison of the LED manufacturing cost structure produced by our cost model with previously reported US DOE calculations and projections based on the LEDCOM model and industry data provided as part of industry round table discussions (see Fig. SI12). We note some differences between the results of our model and the cost structure reported or projected by the DOE. For instance, the share of the epitaxy step is consistently larger in the DOE data. This can in part be explained by our model relying on state-of-the-art equipment at a virtual US-based manufacturing location, while industry might not run low-power and mid-power chip production on these, more expensive, reactors. In addition, the manufacturing lines of the majority of manufacturers is located in Asia. We also note that the share of the substrate price in the DOE data is much larger than in our model, which can in part be explained by the overestimation of the actual price of sapphire wafers in earlier projections for 2015-2020. Finally, the relative importance of the packaging part of the manufacturing process is very similar in our model and in the DOE results in 2012. However, in the DOE projections it significantly decreases by 2020, while in our model it retains and even increases its share of the total cost. This trend has been independently confirmed by researchers and industry reports on wafer-level packaging [127][128][129], showing better performance of our cost model compared to earlier DOE model projections

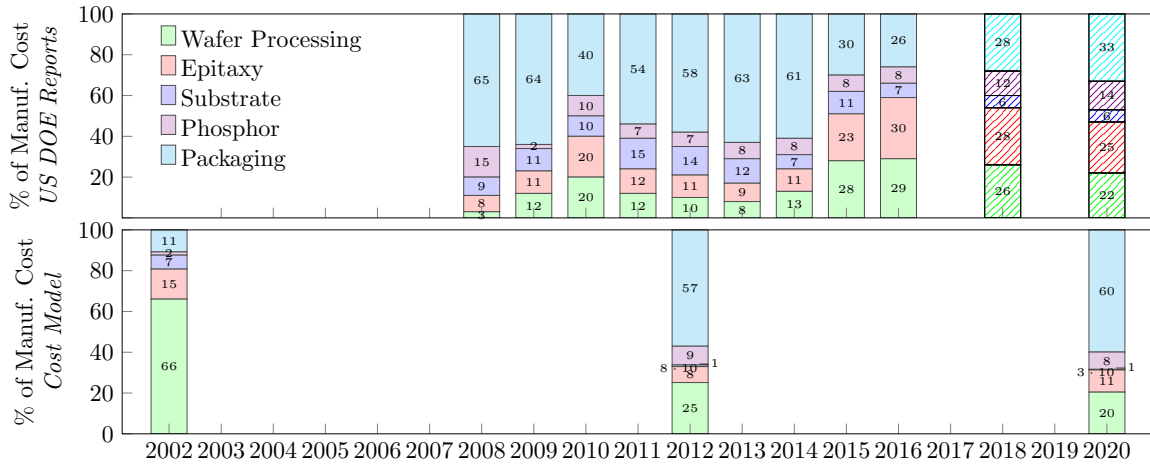


Figure SI12: Comparison of LED manufacturing cost structure between our manufacturing cost model (bottom panel) and previously published US DOE manufacturing cost calculations and projections based on industry data and LEDCOM model (top panel). Hatched bars are projections given by US DOE for 2018 and 2020. Sources for top panel: [130][131][132][133][134][135][136]. Sources for bottom panel: own elaboration based on the cost model described in Section 2.

## 4 Complete List of Sources for Figures

### 4.1 Figure 1 (Historical Development of Luminous Efficacy)

The list of sources for Figure 1 in the main article is organized by different technologies:

<i>Technology</i>	<i>References</i>
LED	own research, compare [137]
CFL (<1984)	[138][139]
CFL (1984-2011)	[140]
CFL (>2011)	[141]
Fire, Incandescent, HID	[142] augmented by own calculations based on [143]
Max. efficacy	[144]

### 4.2 Figure 2 (Historical Development of Lamp Prices)

The sources for Figure 2 in the main article are grouped by the provider of data:

<i>Provider of References</i>	<i>References</i>
Stiftung Warentest (Germany)	[145][146][147][148][149][150][151][152][153][154][155][156][157][158]
Konsument (Austria)	[159]
Which (UK)	[160]
Industry Periodical	[161]
Government Report	[162]

### 4.3 Figure 3 (Historical Evolution of LED Chip Architectures)

The sources for Figure 3 in the main article are grouped by their type:

<i>Type of Source</i>	<i>References</i>
Scientific Publications	[163][164][165][166]
Patents	[167][168][169][169][170][171][172]
Other Publications	[173][174][175]

### 4.4 Fig. SI10 (Historical Developments in Device Sub-Efficiencies)

The sources for Fig. SI10 are grouped by sub-efficiencies represented on different panels of the figure:

<i>Panel (Sub-Eff.)</i>	<i>References</i>
Panel A1 ( $V_f$ )	[176][177][178][179][180][181][182][183][184][185][186][187][188] [189][190][191][192][193][194][195][196][197][198]
Panel A2 (Droop)	Data calculated from luminous intensity curves of respective device datasheets: [199][184][200][201][202][183][189][190][195]
Panel B1 (IQE)	own research, compare [137] [203][56][57][204][205][206][207][51][208][209][58]
Panel B2 (LEE)	[210][211][212][213][214][215][216][217][218][219][220][221][222][223] [224][225][226] [210][227][228][229][230][231][232][233][234][235][227] [228][236][237][238][239][240][241][242][243]

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