Computer Science 118, Homework 1

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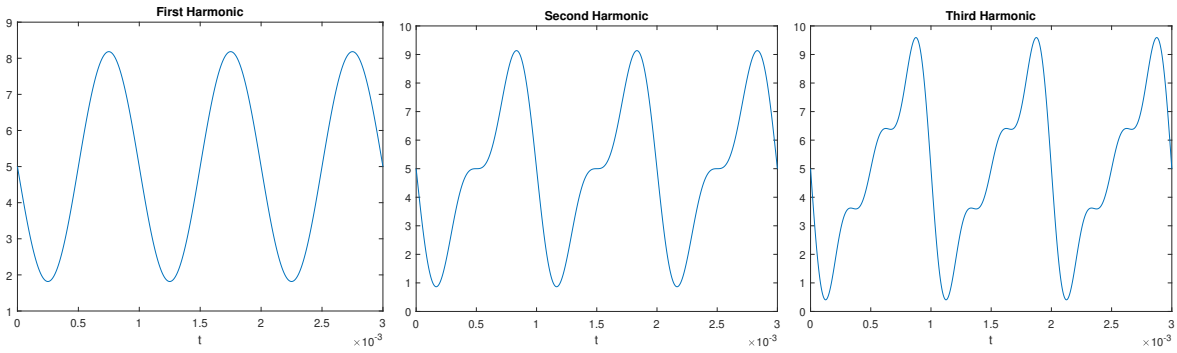
Problem 1

a) There are 3 periods of the signal. This makes sense because the first harmonic frequency is 1000 Hz.

b) The plots of the first three harmonics are shown below.

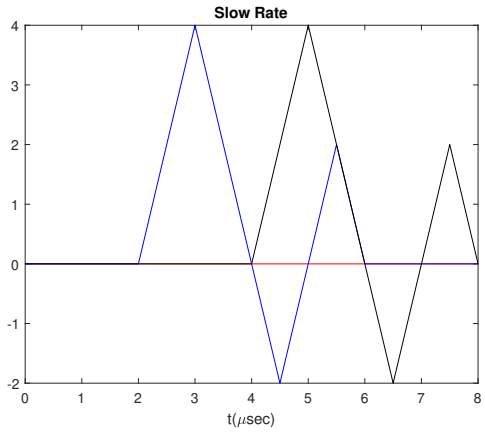


c) It appears to be a sawtooth wave with a frequency of 1000 Hz, a minimum of 0, and a maximum of 10.

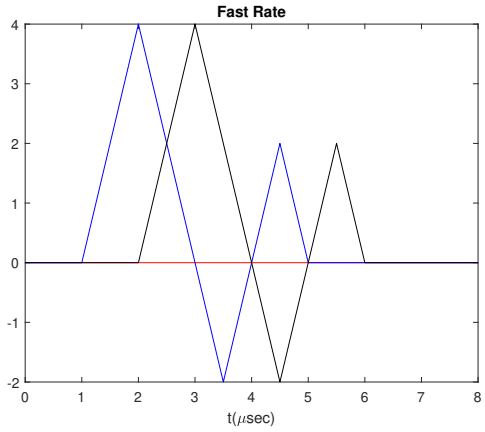
d) Assuming that this is baseband bandwidth, only the first harmonic would be allowed to go through, so the output signal would look like the first harmonic.

Problem 2

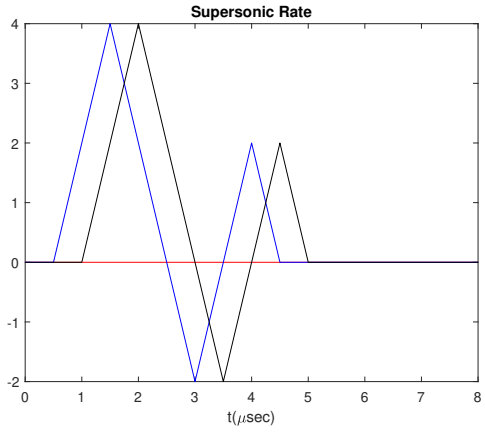
a) The receiver will measure 0V, 4V, then 4V. Thus it will correctly receive the bits 011.



b) The receiver will measure 0V, 4V, then 4V. Thus it will correctly receive the bits 011.

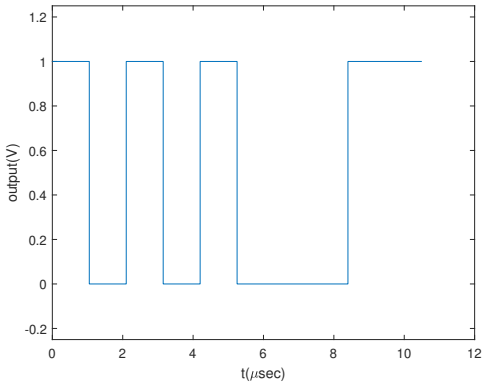


c) The receiver will measure 2V, 6V, then 6V. Thus it will receive the bits 111. Therefore bit interference has caused the 0 to become a 1. Note that all the bits experience bit interference, as the measured voltages are increased due to the effects of other bits.



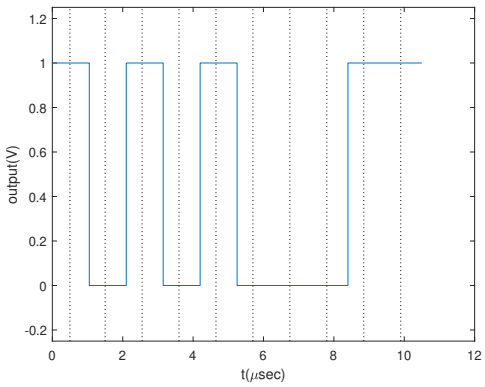
Problem 3

a) The waveform is shown in the following figure.



b) The sampling will happen 0.475μs earlier than it should have if there is no clock recovery.

c) With clock recovery, the sampling will happen at times 0.5μs, 1.5μs, 2.55μs, 3.60μs, 4.65μs, 5.70μs, 6.75μs, 7.80μs, 8.85μs, and 9.90μs. This is shown in the following figure.



d) Lets assume this noise causes the receiver to register a transition. Then at 0.4μs the lag will be set to 0.4μs. The first sample will remain at 0.5μs. At this time the predicted next transition will be at 1.4μs. Then at the transition at 1.05μs, the lag will be set to -0.35μs. The next sampling will be at 1.9μs. The predicted next transition will be at 2.05μs. At 2.10μs, the lag will be set to 0.05μs. The next sampling will be at 2.55μs. From here on out the sequence of samples remains the same as in the previous part, leading to the sampling happening at times 0.5μs, 1.9μs, 2.55μs, 3.60μs, 4.65μs, 5.70μs, 6.75μs, 7.80μs, 8.85μs, and 9.90μs.

e) Lets assume this noise causes the receiver to register a transition. The sampling will proceed normally until 2.4μs. At 2.4μs the receiver has a predicted transition value of 2.05μs, so it will calculate a lag of 0.35μs. It will sample at 2.55μs, updating the predicted transition value to 3.4μs. At 3.15μs, the lag will be set to -0.25μs. A sample occurs at 3.9μs, and the receiver updates the predicted transition value to 4.15μs. At 4.20μs, the lag is updated to 0.05μs. The next sample occurs at 4.65μs. From here on out the sequence of samples remains the same as the previous part, leading to the sampling happening at times 0.5μs, 1.5μs, 2.55μs, 3.90μs, 4.65μs, 5.70μs, 6.75μs, 7.80μs, 8.85μs, and 9.90μs.

Problem 4

a) You can send three bits every microsecond by having 8V correspond to 111, 6V correspond to 110, 4V correspond to 101, 2V correspond to 100,

-2V correspond to 011, -4V correspond to 010, -6V correspond to 001, and -8V correspond to 000.

b) No this coding scheme does not guarantee transitions, for example if all 1's were sent then the signal would stay at 8V and if all 0's were sent then the signal would stay at -8V.

c) No this coding scheme is not DC balanced, as the signal could be a constant 8V if all 1's are being sent.

d) The best DC balanced code I can think of is encoding 11 as either -8V or 8V, 10 as either -6V or 6V, 01 as either -4V or 4V, and 00 as either -2V or 2V. The encoded signal would choose the appropriate inverse value for each bit sequence in order to make the signal DC balanced.

e) In this DC balanced code, two bits are transmitted each microsecond.

f) Yes, transitions can be guaranteed. This is because if a sequence of the same bit pattern is sent, we can simply send a voltage that is opposite in sign but the same magnitude. This way between any two pairs of bit patterns there can be a transition.

g) The maximum amount of noise that this scheme can tolerate is noise with a magnitude of 0.5V, due to the Shannon limit.

Problem 5

We can send one bit every 40ns without interference due to dispersion. This means that the maximum bit rate that we can use without causing inter-symbol interference is 2.5×10^7 bits per second. If we double the length of the fiber link, we can expect the difference between the longest route and shortest route to increase to 80ns. This will halve our bit rate to 1.25×10^7 bits per second.