CS M51A and EE M16 Summer 2016 Section 1

Logic Design of Digital Systems

Dr. Yutao He

Project #1 - Orientation of Verilog and Vivado

Due: Sunday, July 17^{th} 2016

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Discussion: 1A

Date: 7/15/16

Result	
Correctness	
Creativity	
Report	
Total Score	

Project #1 Orientation of Verilog and Vivado Project Requirement

Dr. Yutao He

1 Objectives

This first project is intended to get you acquainted with Verilog and Vivado software by implementing a simple combinational circuit, and familiar with the typical work-flow of using the Computer-Aided Design(CAD) tool in the design of digital systems.

2 Project Description

In this project, you will use the Xilinx Vivado software and Verilog to implement the circuit that is specified in Figure 2.12 on page 32 of the textbook. It consists of two basic steps:

(1) **Verilog Coding**

You should use the *Text Editor* in Vivado to write the Verilog code that describes the function of the circuit and then to synthesize it.

(2) **Function (Behavior) Simulation**

After the Verilog code passes compilation, simulation is followed to test if your implementation performs the specified function (that is, to verify its correctness). In order to do so, you must apply each combination of input values to the circuit and obtain the corresponding output values. This can be entered as a separate test bench file. *ISim* is a simulator in the Vivado serves this purpose. The *Waveform Window* can be used to display the results in the waveform (i.e., a Timing Diagram). If the implementation is incorrect, you have to debug it until it works properly.

Extra Credits

To pique interests of some highly motivated and curious minds, we will give extra credits to those of you who will take your design and implement it successfully on the Mojo FPGA (Field Programmable Gate Array) development board.

3 Report Outline

You are required to submit a report that provides complete documentation of your project. As in all technical writing, its purpose is to communicate your work with your colleagues in an efficient and professional way. As a result, it must be clear, concise and complete and must contain the following parts:

(1) *Title Page*

It is provided and you just need to fill in your information in the blanks.

(2) *Project Requirement*

It is this handout.

(3) *The Function of The Circuit*

The function of the circuit has already been specified in the textbook so you do not need to design from the scratch. But you must include in your report its canonical switching expression and the corresponding schematic diagram.

(4) *The Verilog file*

The Verilog file (with extension .v) you write is the implementation of the circuit. You should include it in your report with your name and student ID on it.

(5) *The Simulation Result*

You have to demonstrate that your implementation works as specified by showing the simulation result from Vivado. **Screendump** the Timing Diagram that consists of waveforms of the inputs and the output. Please provide enough information on the timing diagram so that one of your colleagues who doesn't know anything about your project could understand which function you are trying to implement

and evaluate it. **A timing diagram without any explanation is subject to penalty**.

(6) *The Summary*

This writeup should be short and state at least one problem you encounter during the implementation and the workaround you come up with, or any other comments you would like to make.

4 Vivado Software

The Xilnx Vivado Software provides a free version, called *WebPack* for Windows and Linux operating systems. It requires registration for downloading. The download website is: http://www.xilinx.com/support/download/index.htm.

5 Mojo FPGA Development Board

Mojo is one of cheapest FPGA development boards that allows implementation of digital systems on the FPGA device. Its details can be found at https://embeddedmicro.com/products/mojo-v3.html.

6 Project Submission

By July 15th, a sumbmission link will be set up on the course website. You should submit one zipped file named 1234567.zip, where 1234567 is your student ID. The zipped file must include the following three files:

1. The pdf file of your report. It must be named with your student ID. As a result, your report should be called *1234567.pdf*;
2. The Verilog file of your circuit implementation. It must be named as: *csm51a_proj1.v*;
3. The testbench file. It must be named as *csm51a_proj1_tb.v*.

7 Project Deadline

The report is due at midnight (11:59:59pm) July 17th (Sunday), 2016. Late submission is subject to penalty.

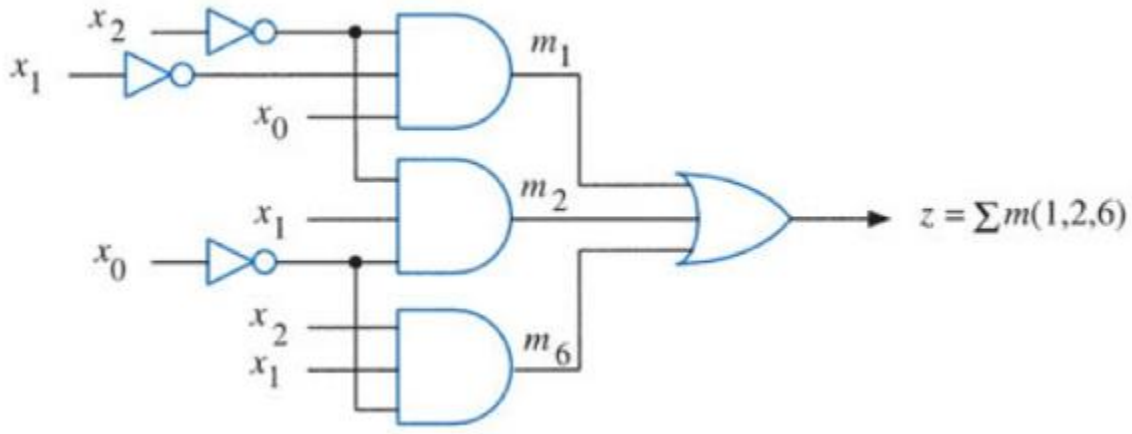
The Function of the Circuit

The function implemented is $E(x_2, x_1, x_0) = \sum m(1,2,6)$.

The canonical sum of products expression for the circuit is

$$z = x_2' x_1' x_0 + x_2' x_1 x_0' + x_2 x_1 x_0'$$

which has the corresponding diagram

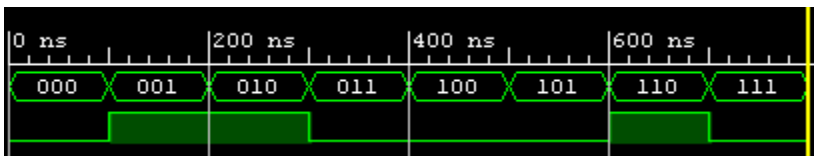


The Verilog File

```
//csm51a_proj1.v
//Michael Wu
//ID: 40451542
`timescale 1ns / 1ps
module myCircut(
    input [2:0] x,
    output z
    );
wire m1,m2,m6;
assign m1=~x[2]&~x[1]&x[0];
assign m2=~x[2]&x[1]&~x[0];
assign m6=x[2]&x[1]&~x[0];
assign z=m1|m2|m6;
endmodule
```

The Simulation Result

This test bench plugged every possible binary value into the module. This input is represented by the row of binary numbers. The waveform below corresponds to the output, which has a value of 1 when it is high and 0 when it is low. The function correctly output 1 for the binary representations of the numbers 1, 2, and 6.



The Summary

In this project I implemented a combinational circuit in Verilog. One problem I had was with the simulation, as I did not know the syntax to change the value of the input after a given period of time. I ended up writing a for loop in order to increment the binary input each 100ns. The actual code did not take very long, once I read about the syntax.