IT5002 Tutorial 5

AY 2025/26 Semester 1

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Slides adapted from Theodore Leebrant, Prof. Colin and Prof. Aaron

1. A byte-addressed machine with a word size of 16 bits and address width of 32 bits has a direct-mapped cache with 16 blocks and a block size of 2 words. Given the sequence of memory accesses, indicate whether the reference is a hit or miss. For a miss, identify the type (compulsory/conflict/capacity).

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	
7	7	
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

92 = 0x5C = 0b00000000000000000000000001011100

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4			
5			
6			
7	0x0000001	M[0x5c]	M[0x60]
8			
9			
10			
11			
12			
13			
14			
15			

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

7 = 0x007 = 0b00000000000000000000000000000111

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4			
5			
6			
7	0x0000001	M[0x5c]	M[0x60]
8			
9			
10			
11			
12			
13			
14			
15			

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

146 = 0x092 = 0b00000000000000000000000010010010

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90]	M[0x92] Miss
5			
6			
7	0x0000001	M[0x5c]	M[0x60]
8			
9			
10			
11			
12			
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

30 = 0x01E = 0b00000000000000000000000011110

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000000	M[0x1C]	M[0x1E] Miss
8			
9			
10			
11			
12			
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

95 = 0x05F = 0b00000000000000000000001011111

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000001	M[0x5C]	M[0x5E] Miss
8			
9			
10			
11			
12			
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	
93	5D	
145	91	
264	108	
6	6	

176 = 0x0B0 = 0b00000000000000000000000010110000

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000001	M[0x5C]	M[0x5E]
8			
9			
10			
11			
12	0x0000002	M[0x0B0] Miss	M[0x0B2]
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	M (cold)
93	5D	
145	91	
264	108	
6	6	

93 = 0x05D = 0b00000000000000000000000001011101

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000001	M[0x5C] Hit	M[0x5E]
8			
9			
10			
11			
12	0x0000002	M[0x0B0]	M[0x0B2]
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	M (cold)
93	5D	H
145	91	
264	108	
6	6	

145 = 0x091 = 0b00000000000000000000000010010001

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2			
3			
4	0x0000002	M[0x90] Hit	M[0x92]
5			
6			
7	0x0000001	M[0x5C]	M[0x5E]
8			
9			
10			
11			
12	0x0000002	M[0x0B0]	M[0x0B2]
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	M (cold)
93	5D	H
145	91	H
264	108	
6	6	

264 = 0x108 = 0b00000000000000000000000100001000

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2	0x0000004	M[0x108] Miss	M[0x10A]
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000001	M[0x5C]	M[0x5E]
8			
9			
10			
11			
12	0x0000002	M[0x0B0]	M[0x0B2]
13			
14			
15			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	

6 = 0x006 = 0b00000000000000000000000000000110

(direct mapped)

Index	Tag Value	Word 0	Word 1
0			
1	0x0000000	M[0x4]	M[0x6]
2	0x0000004	M[0x108]	M[0x10A]
3			
4	0x0000002	M[0x90]	M[0x92]
5			
6			
7	0x0000001	M[0x5C]	M[0x5E]
8			
9			
10			
11			
12	0x0000002	M[0x0B0]	M[0x0B2]
13			
14			
15			

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (conflict)
95	5F	M (conflict)
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	H

92 = 0x5C = 0b00000000000000000000000010111100

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4						
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	Miss		

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

7 = 0x007 = 0b00000000000000000000000000000111

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6] Hit			
2						
3						
4						
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

146 = 0x092 = 0b00000000000000000000000010010010

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92] Miss			
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]			

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

30 = 0x01E = 0b00000000000000000000000011110

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92]			
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	0x0000000	M[0x01C]	M[0x01E]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

95 = 0x05F = 0b00000000000000000000000001011111

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92]			
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	Hit 000000	M[0x01C]	M[0x01E]

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	
93	5D	
145	91	
264	108	
6	6	

176 = 0x0B0 = 0b00000000000000000000000101**10**000

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92]	0x0000005	M[0x0B0]	M[0x0B2]
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	0x0000000	M[0x01C]	M[0x01E]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	
145	91	
264	108	
6	6	

93 = 0x05D = 0b00000000000000000000000001011101

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92]	0x0000005	M[0x0B0]	M[0x0B2]
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	Hit 000000	M[0x01C]	M[0x01E]

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	
264	108	
6	6	

145 = 0x091 = 0b00000000000000000000000010010001

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2						
3						
4	0x0000004	M[0x90]	M[0x92]	Hit 000005	M[0x0B0]	M[0x0B2]
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	0x0000000	M[0x01C]	M[0x01E]

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	
6	6	

264 = 0x108 = 0b00000000000000000000000100001000

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6]			
2	0x0000008	M[0x108]	M[0x10A]	Miss		
3						
4	0x0000004	M[0x90]	M[0x92]	0x0000005	M[0x0B0]	M[0x0B2]
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	0x0000000	M[0x01C]	M[0x01E]

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	

6 = 0x006 = 0b00000000000000000000000000000110

(two-way set associative)

Index	Set 0			Set 1		
	Tag Value	Word 0	Word 1	Tag Value	Word 0	Word 1
0						
1	0x0000000	M[0x4]	M[0x6] Hit			
2	0x0000008	M[0x108]	M[0x10A]			
3						
4	0x0000004	M[0x90]	M[0x92]	0x0000005	M[0x0B0]	M[0x0B2]
5						
6						
7	0x0000002	M[0x5C]	M[0x5E]	0x0000000	M[0x01C]	M[0x01E]

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	H

92 = 0x5C = 0b00000000000000000000000001011100

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

7 = 0x007 = 0b00000000000000000000000000000111

(fully associative)

Tag Value	Word 0	Word 1	
0x0000001	M[0x4]	M[0x6]	Hit
0x0000017	M[0x5C]	M[0x5E]	

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

146 = 0x092 = 0b00000000000000000000000010010010

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

30 = 0x01E = 0b00000000000000000000000000011110

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

95 = 0x05F = 0b00000000000000000000000010111**11**

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	
93	5D	
145	91	
264	108	
6	6	

176 = 0x0B0 = 0b00000000000000000000000010110000

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]
0x000002C	M[0xB0]	M[0xB2]

Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	
145	91	
264	108	
6	6	

93 = 0x05D = 0b00000000000000000000000001011101

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]
0x000002C	M[0xB0]	M[0xB2]

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	
264	108	
6	6	

145 = 0x091 = 0b00000000000000000000000010010001

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]
0x000002C	M[0xB0]	M[0xB2]

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	
6	6	

264 = 0x108 = 0b00000000000000000000000100001000

(fully associative)

Tag Value	Word 0	Word 1	
0x0000001	M[0x4]	M[0x6]	
0x0000017	M[0x5C]	M[0x5E]	
0x0000024	M[0x90]	M[0x92]	
0x0000007	M[0x1C]	M[0x1E]	
0x000002C	M[0xB0]	M[0xB2]	
0x0000042	M[0x108]	M[0x10A]	Miss

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	

6 = 0x006 = 0b00000000000000000000000000000110

(fully associative)

Tag Value	Word 0	Word 1
0x0000001	M[0x4]	M[0x6]
0x0000017	M[0x5C]	M[0x5E]
0x0000024	M[0x90]	M[0x92]
0x0000007	M[0x1C]	M[0x1E]
0x000002C	M[0xB0]	M[0xB2]
0x0000042	M[0x108]	M[0x10A]

Hit

Memory Address		Hit (H) or Miss (M)
(in decimal)	(in hexadecimal)	
4	4	M (cold)
92	5C	M (cold)
7	7	H
146	92	M (cold)
30	1E	M (cold)
95	5F	H
176	B0	M (cold)
93	5D	H
145	91	H
264	108	M (cold)
6	6	H

2. A machine with byte addresses and a word size of 32 bits and address width of 32 bits has a direct-mapped data cache with 4 blocks each consisting of 2 words. Given the MIPS program below, and assuming that array A starts at memory hexadecimal location 0x1000 while array B starts at memory hexadecimal location 0x4010. Fill in the first 10 address requests seen at the data cache and indicate whether the reference is a hit (H) or a miss (M). Assume that the cache is initially empty

```
start:
      la   $s0, A                 #PC=0x100
      la   $s1, B                 #PC=0x104
      li   $t0, 1                 #PC=0x108
loop:
      slt  $t1, $t0, 1000         #PC=0x10c
      beq  $t1, $zero, end_loop   #PC=0x110
      sll  $t2, $t0, 2            #PC=0x114
      add  $t3, $s0, $t2          #PC=0x118
      lw   $a0, 0($t3)            #PC=0x11c
      add  $t4, $s1, $t2          #PC=0x120
      lw   $a1, 0($t4)            #PC=0x124
      add  $v0, $a0, $a1          #PC=0x128
      sw   $v0, -4($t3)           #PC=0x12c
      addi $t0, $t0, 1            #PC=0x130
      j    loop                   #PC=0x134
end_loop:
      .   .   .
```

```
start:
      la   $s0, A                  #PC=0x100
      la   $s1, B                  #PC=0x104
      li   $t0, 1                  #PC=0x108
loop:
      slt  $t1, $t0, 1000          #PC=0x10c
      beq  $t1, $zero, end_loop    #PC=0x110
      sll  $t2, $t0, 2             #PC=0x114
      add  $t3, $s0, $t2           #PC=0x118
      lw   $a0, 0($t3)             #PC=0x11c
      add  $t4, $s1, $t2           #PC=0x120
      lw   $a1, 0($t4)             #PC=0x124
      add  $v0, $a0, $a1           #PC=0x128
      sw   $v0, -4($t3)            #PC=0x12c
      addi $t0, $t0, 1             #PC=0x130
      j    loop                    #PC=0x134
end_loop:
      .   .   .
```

$s0 = 0x1000
$s1 = 0x4010
$t0 = 1

Set $t1 to result of whether $t0 is less than 1000 i.e.
$t1 = ($t0 < 1000) ? 1 : 0

Branch to end_loop if $t1 is equal to 0, i.e. $t0 < 1000 is false, i.e. $t0 >= 1000

$t2 = $t0 * 4 = 1 * 4 = 4

$t3 = $s0 + $t2 = 0x1000 + 4 = 0x1004
Load word from 0($t3) into $a0 i.e. $a0 = M[$t3]

$t4 = $s1 + $t2 = 0x4010 + 4 = 0x4014
Load word from 0($t3) into $a1 i.e. $a1 = M[$t4]

$v0 = $a0 + $a1
Store $v0 into –4($t3) i.e. M[$t3 – 4] = $v0

$t0 = $t0 + 1
Jump to loop

$t0 starts from 1. In each iteration, it is increased by 1. The loop only stops when $t0 >= 1000.

```
start:
      la   $s0, A                    #PC=0x100
      la   $s1, B                    #PC=0x104
      li   $t0, 1                    #PC=0x108
loop:
      slt  $t1, $t0, 1000            #PC=0x10c
      beq  $t1, $zero, end_loop      #PC=0x110
      sll  $t2, $t0, 2               #PC=0x114
      add  $t3, $s0, $t2             #PC=0x118
      lw   $a0, 0($t3)               #PC=0x11c
      add  $t4, $s1, $t2             #PC=0x120
      lw   $a1, 0($t4)               #PC=0x124
      add  $v0, $a0, $a1             #PC=0x128
      sw   $v0, -4($t3)              #PC=0x12c
      addi $t0, $t0, 1               #PC=0x130
      j    loop                      #PC=0x134
end_loop:
      .   .   .
```

1. lw from 0x1004 – … 0001 0000 0000 0100 (Cold Miss)
2. lw from 0x4014 – … 0100 0000 0001 0100 (Cold miss)
3. sw to 0x1000 – … 0001 0000 0000 0000 (Hit)
4. lw from 0x1008 – … 0001 0000 0000 1000 (Cold Miss)
5. lw from 0x4018 – … 0100 0000 0001 1000 (Cold Miss)
6. sw to 0x1004 – 0001 0000 0000 0100 (Hit)
7. lw from 0x100c – … 0001 0000 0000 1100 (Hit)
8. lw from 0x401c – … 0100 0000 0001 1100 (Hit)
9. sw to 0x1008 - 0001 0000 0000 1000 (Hit)
10. lw from 0x1010 - … 0001 0000 0001 0000 (Conflict Miss)

Index	Tag Value	Word 0	Word 1
0	0x80	M[0x1000]	M[0x1004]
1	0x80	M[0x1008]	M[0x100C]
2	0x200	M[0x4010]	M[0x4014]
3	0x200	M[0x4018]	M[0x401C]

Fill the final contents of the cache.

Note that at iteration *i*, the 3 memory accesses are
- lw from 0x1000 + 4i
- lw from 0x4010 + 4i
- sw to 0x1000 + 4(i-1)

For iteration 999, they are
lw to 0x1000 + 4*999 = 0x1F9C (index = 3, tag = 0xFC)
lw to 0x4010 + 4*999 = 0x4FAC (index = 1, tag = 0x27D)
sw to 0x1000 + 4*998 = 0x1F98 (index = 3, tag = 0xFC)

Since this is the last iteration, we can be sure that these values will end up in the cache.

For iteration 998, they are
lw from 0x1000 + 4 * 998 = 0x1F98 (index = 3, tag = 0xFC)
lw from 0x4010 + 4 * 998 = 0x4FA8 (index = 1, tag = 0x27D)
sw to 0x1000 + 4 * 997 = 0x1F94 (index = 2, tag = 0xFC)

For iteration 997, they are
lw from 0x1000 + 4 * 997 = 0x1F94 (index = 2, tag = 0xFC)
lw from 0x4010 + 4 * 997 = 0x4FA4 (index = 0, tag = 0x27D)
sw to 0x1000 + 4 * 996 = 0x1F98 (index = 3, tag = 0xFC)

Index	Tag Value	Word 0	Word 1
0	0x27D	M[0x4FA0]	M[0x4FA4]
1	0x27D	M[0x4FA8]	M[0x4FAC]
2	0xFC	M[0x1F90]	M[0x1F94]
3	0xFC	M[0x1F98]	M[0x1F9C]

What is the total number of data cache memory references, hits and misses?

In each iteration, there is two lw and one sw instruction.

The sw always hits the block brought in by the first lw. So in all 999 iterations, sw always hits.

The first lw starts with index 0. It cycles through the indices 0, 1, 2, 3.

The second lw starts with index 2 and cycles through the indices 3, 0, 1, 2.

Importantly, the two lw instructions do not 'interfere' with each other. That is, the two lw's do not overwrite each other's block that they just brought in.

Other than the first iteration, all the other 999 – 1 = 998 iterations will have one cold miss (to load the block into cache) followed by 1 cache hit.

Total no. of data cache references = 999 * 3 = 2997

Number of hits = (998 / 2) * 2 + 999 = 1498

Number of misses = 2 (first iteration) + (998 / 2) * 2 = 1000

3. Suppose a (32 bit) MIPS processor has an instruction cache that is also direct mapped with 4 blocks each consisting of 2 words. Using the same program found in Question 2, fill in the final contents of the cache, assuming *start* is at location 0x100, and each instruction occupies 32 bits.

```
start:
      la    $s0, A                  #PC=0x100
      la    $s1, B                  #PC=0x104
      li    $t0, 1                  #PC=0x108
loop:
      slt   $t1, $t0, 1000          #PC=0x10c
      beq   $t1, $zero, end_loop    #PC=0x110
      sll   $t2, $t0, 2             #PC=0x114
      add   $t3, $s0, $t2           #PC=0x118
      lw    $a0, 0($t3)             #PC=0x11c
      add   $t4, $s1, $t2           #PC=0x120
      lw    $a1, 0($t4)             #PC=0x124
      add   $v0, $a0, $a1           #PC=0x128
      sw    $v0, -4($t3)            #PC=0x12c
      addi  $t0, $t0, 1             #PC=0x130
      j     loop                    #PC=0x134
end_loop:
      .   .   .
```

PC = 0x10c (index = 1, tag = 0x8)
PC = 0x110 (index = 2, tag = 0x8)
PC = 0x114 (index = 2, tag = 0x8)
PC = 0x118 (index = 3, tag = 0x8)
PC = 0x11c (index = 3, tag = 0x8)
PC = 0x120 (index = 0, tag = 0x9)
PC = 0x124 (index = 0, tag = 0x9)
PC = 0x128 (index = 1, tag = 0x9)
PC = 0x12c (index = 1, tag = 0x9)
PC = 0x130 (index = 2, tag = 0x9)
PC = 0x134 (index = 2, tag = 0x9)
PC = 0x10c (index = 1, tag = 0x8)
PC = 0x110 (index = 2, tag = 0x8)

Index	Tag Value	Word 0	Word 1
0	0x9	PC=0x120	PC=0x124
1	0x8	PC=0x108	PC=0x10C
2	0x8	PC=0x110	PC=0x114
3	0x8	PC=0x118	PC=0x11C

Find the Miss Rate.

Initialization
PC = 0x100 (index = 0, tag = 0x8) cold miss
PC = 0x104 (index = 0, tag = 0x8) hit
PC = 0x108 (index = 1, tag = 0x8) cold miss

Iteration 0 ($t0 = 1)
PC = 0x10c (index = 1, tag = 0x8) hit
PC = 0x110 (index = 2, tag = 0x8) cold miss
PC = 0x114 (index = 2, tag = 0x8) hit
PC = 0x118 (index = 3, tag = 0x8) cold miss
PC = 0x11c (index = 3, tag = 0x8) hit
PC = 0x120 (index = 0, tag = 0x9) cold miss
PC = 0x124 (index = 0, tag = 0x9) hit
PC = 0x128 (index = 1, tag = 0x9) cold miss
PC = 0x12c (index = 1, tag = 0x9) hit
PC = 0x130 (index = 2, tag = 0x9) cold miss
PC = 0x134 (index = 2, tag = 0x9) hit

5 cold misses, 6 hits

Index	Tag Value	Word 0	Word 1
0	0x8	PC=0x100	PC=0x104
1	0x8	PC=0x108	PC=0x10C
2			
3			

Index	Tag Value	Word 0	Word 1
0	~~0x8~~ 0x9	PC=~~0x100~~ 0x120	~~C=0x104~~ 0x124
1	~~0x8~~ 0x9	PC=~~0x108~~ 0x128	~~PC=0x10C~~ 0x12C
2	~~0x8~~ 0x9	PC=~~0x110~~ 0x130	~~PC=0x114~~ 0x134
3	0x8	PC=0x118	C=0x11C

Iteration 1 ($t0 = 2)
PC = 0x10c (index = 1, tag = 0x8) conflict miss
(and all subsequent misses are conflict misses)

PC = 0x110 (index = 2, tag = 0x8) miss
PC = 0x114 (index = 2, tag = 0x8) hit
PC = 0x118 (index = 3, tag = 0x8) hit
PC = 0x11c (index = 3, tag = 0x8) hit
PC = 0x120 (index = 0, tag = 0x9) hit
PC = 0x124 (index = 0, tag = 0x9) hit

Index	Tag Value	Word 0	Word 1
0	0x9	PC=0x120	PC=0x124
1	~~0x9~~ 0x8	PC=0x110	PC=0x114
2	~~0x9~~ 0x8	PC=0x118	PC=0x11C
3	0x8	PC=0x118	PC=0x11C

PC = 0x128 (index = 1, tag = 0x9) miss
PC = 0x12c (index = 1, tag = 0x9) hit
PC = 0x130 (index = 2, tag = 0x9) miss
PC = 0x134(index = 2, tag = 0x9) hit

4 (conflict) misses, 7 hits

Index	Tag Value	Word 0	Word 1
0	0x9	PC=0x120	PC=0x124
1	~~0x8~~ 0x9	PC=0x128	PC=0x12C
2	~~0x8~~ 0x9	PC=0x130	PC=0x134
3	0x8	PC=0x118	PC=0x11C

Last iteration ($t0 = 1000): Only the first two instructions are executed (both conflict misses)

Total Misses = 2 (initialization) + 5 (iteration 0) + 998 * 4 (iteration 1-998) + 2 (last iteration) = 4001

Total Hits = 1 (initialization) + 6 (iteration 0) + 998 * 7 (iteration 1-998) = 6993

Miss Rate = 4001 / (4001 + 6993) = 36.39%

Slides uploaded to https://github.com/michaelyql/IT5002

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Anonymous feedback: https://bit.ly/feedback-michael

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