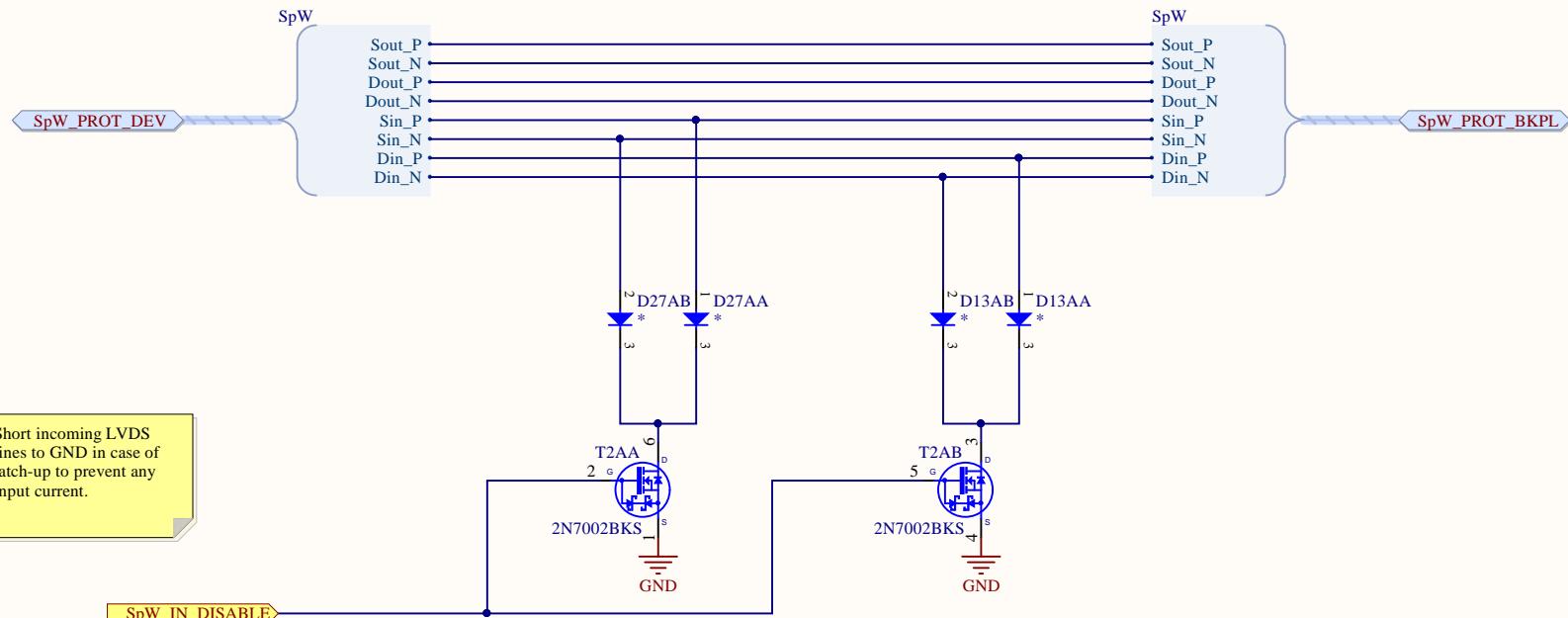


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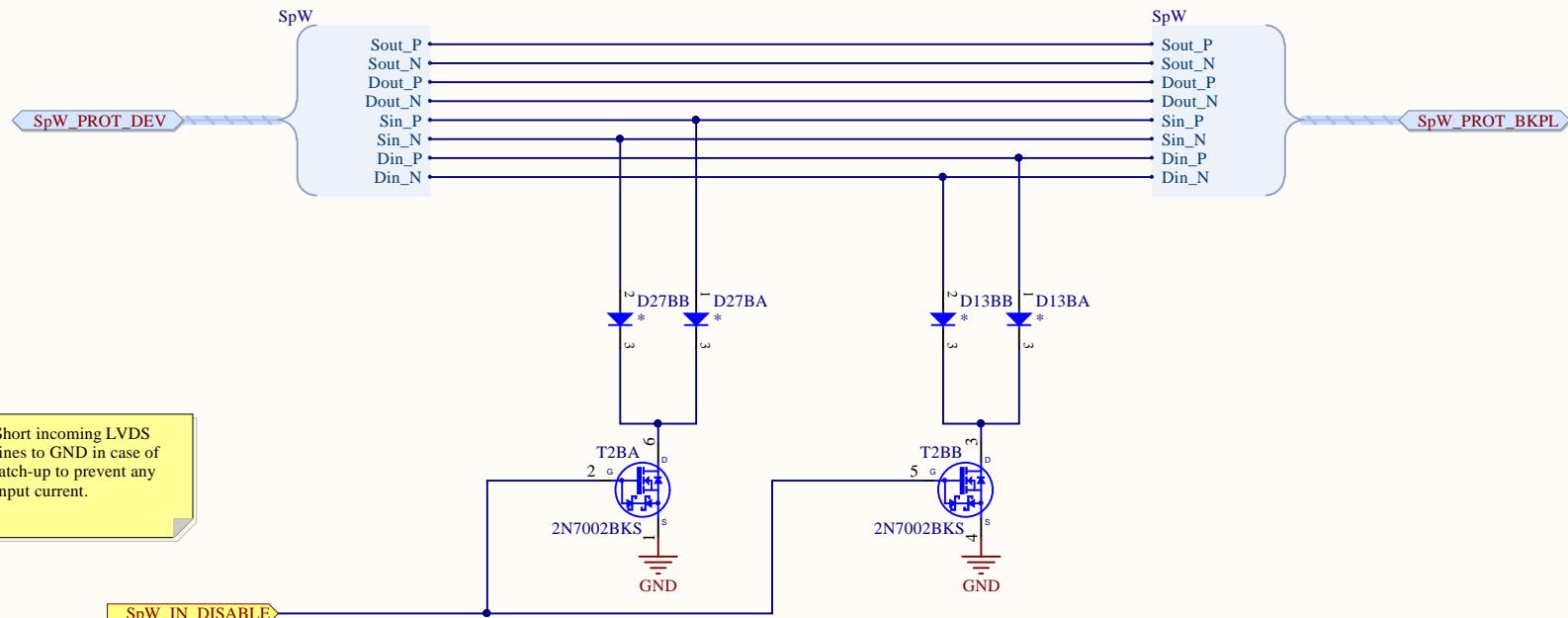
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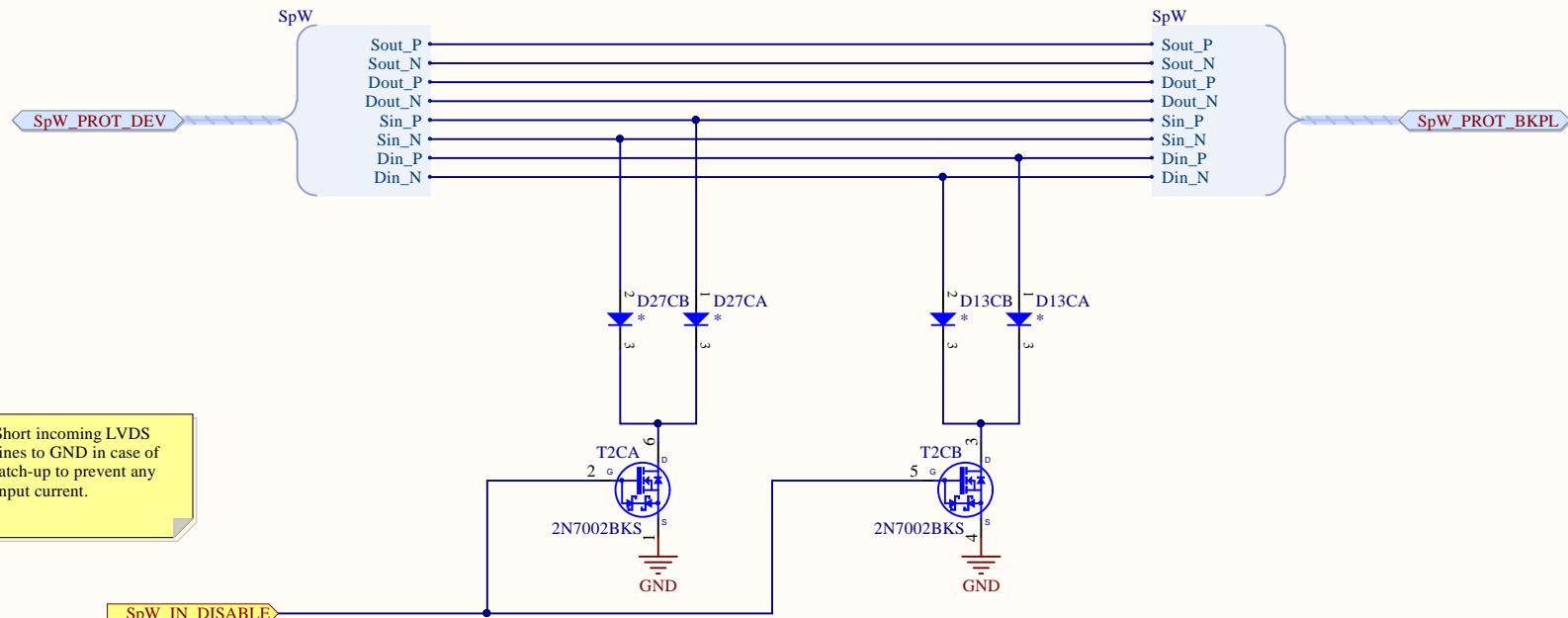
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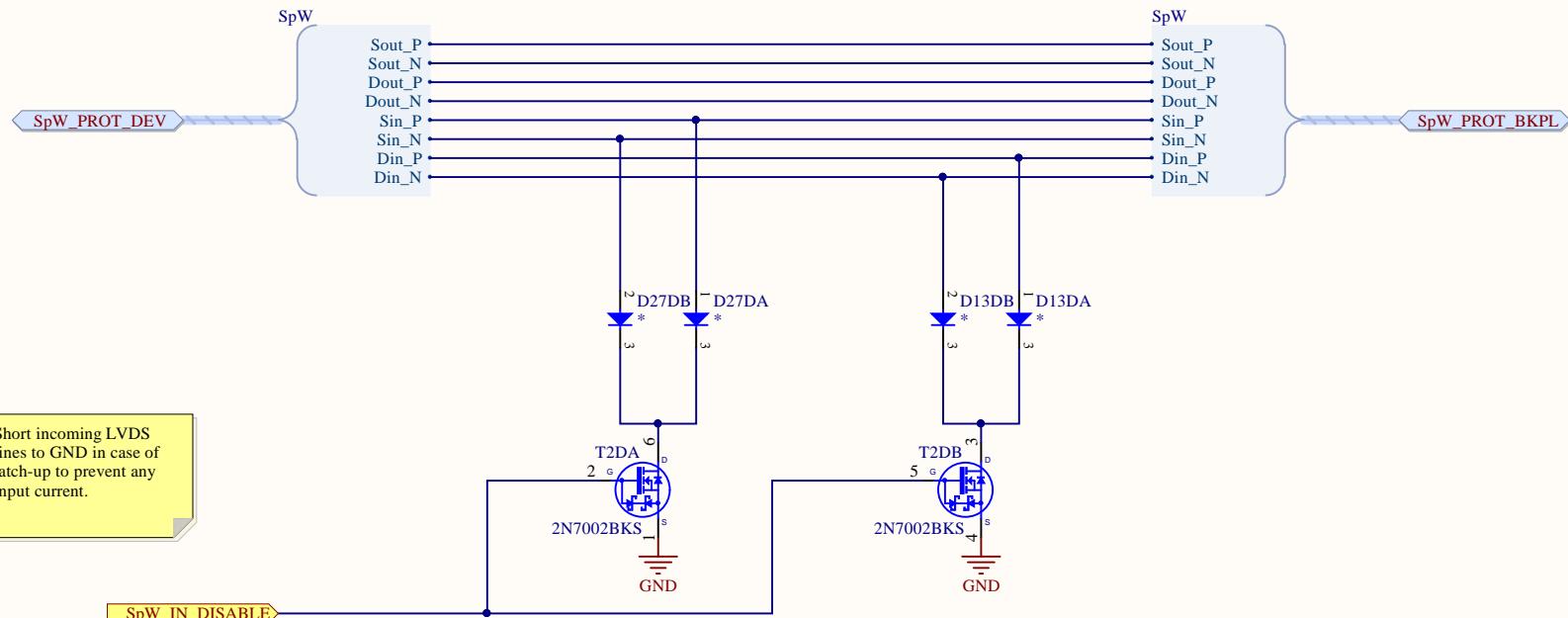
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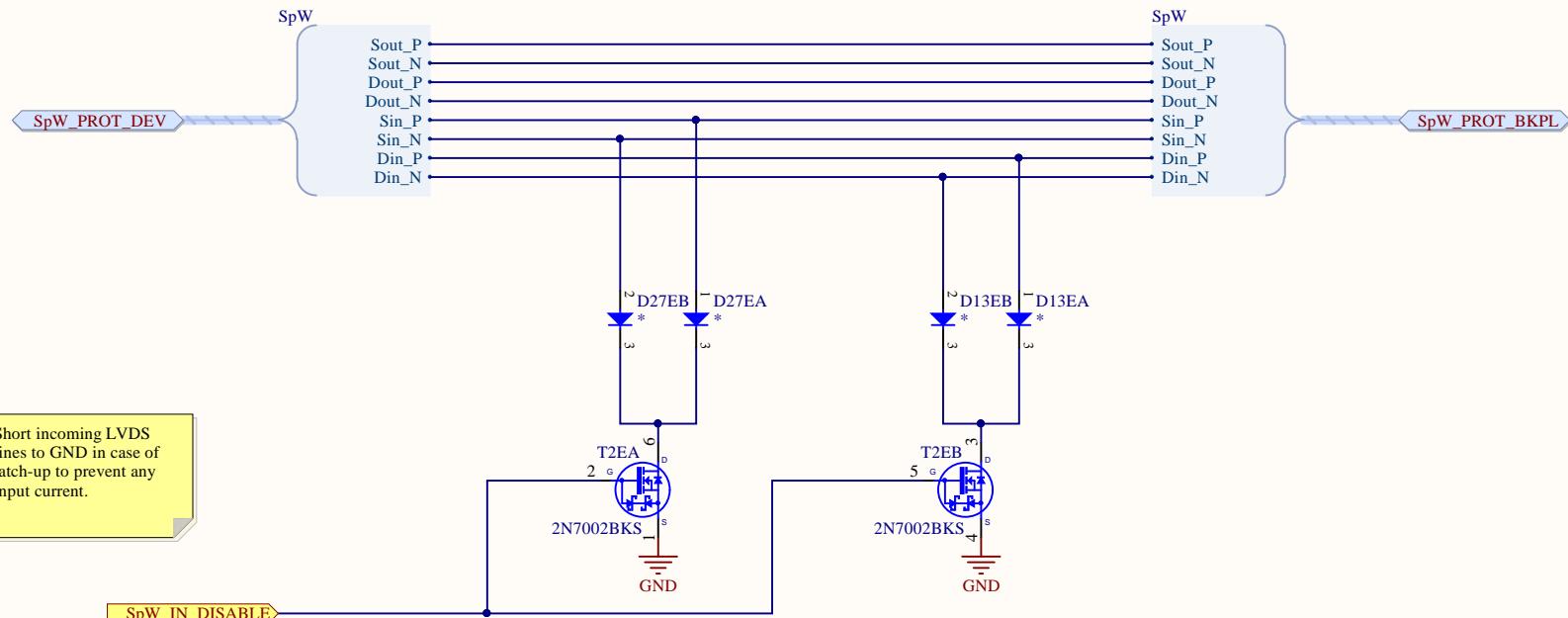
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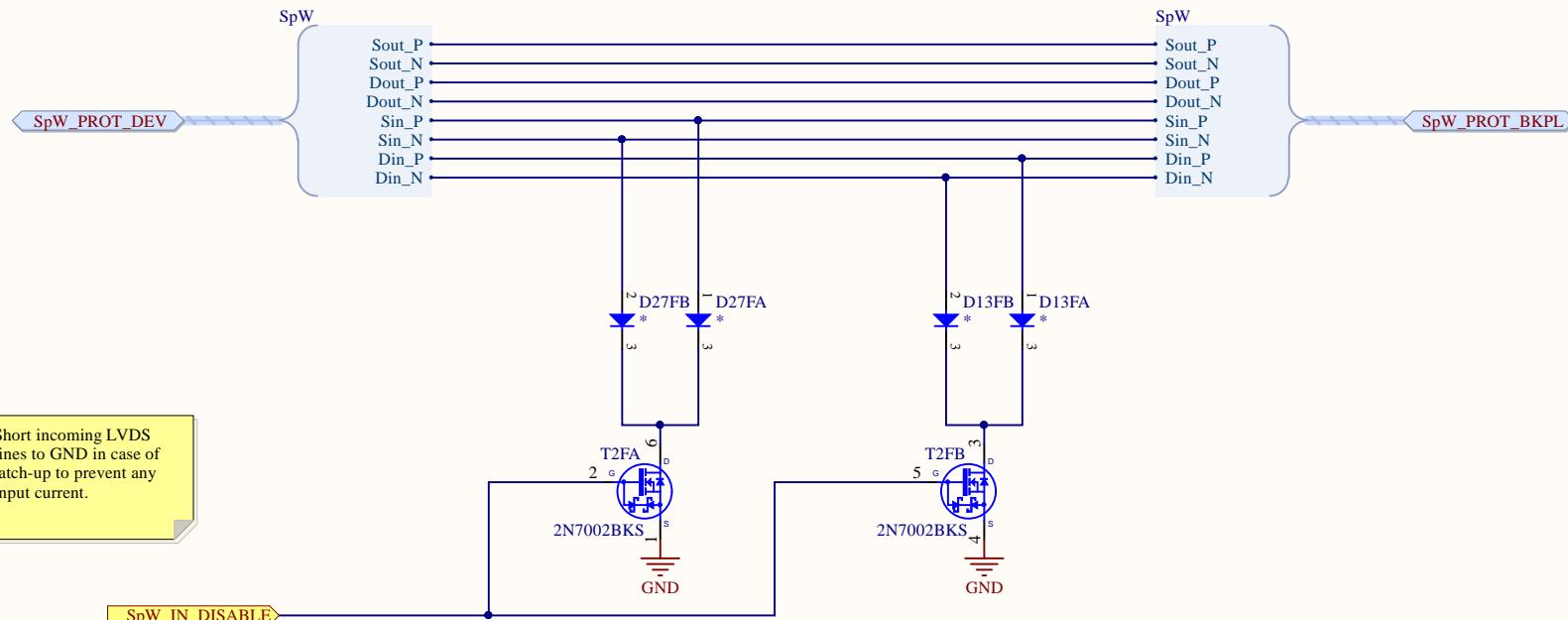
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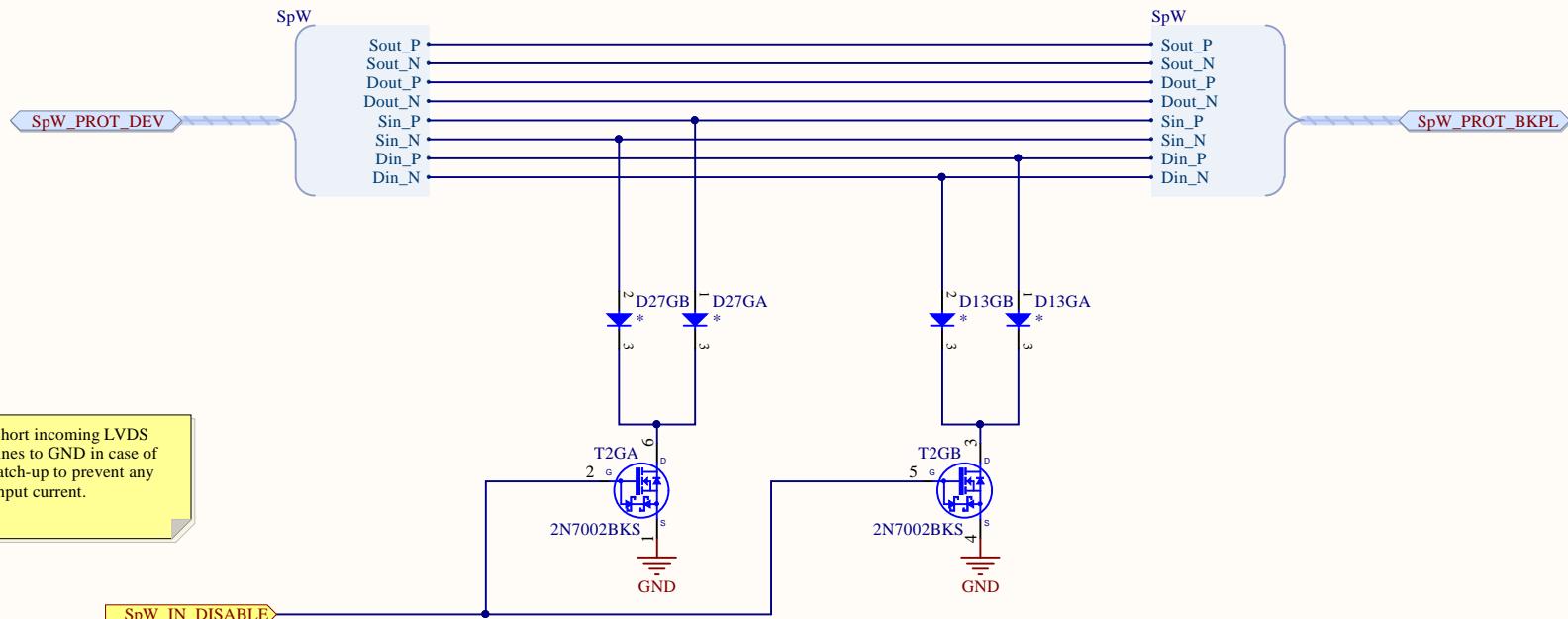
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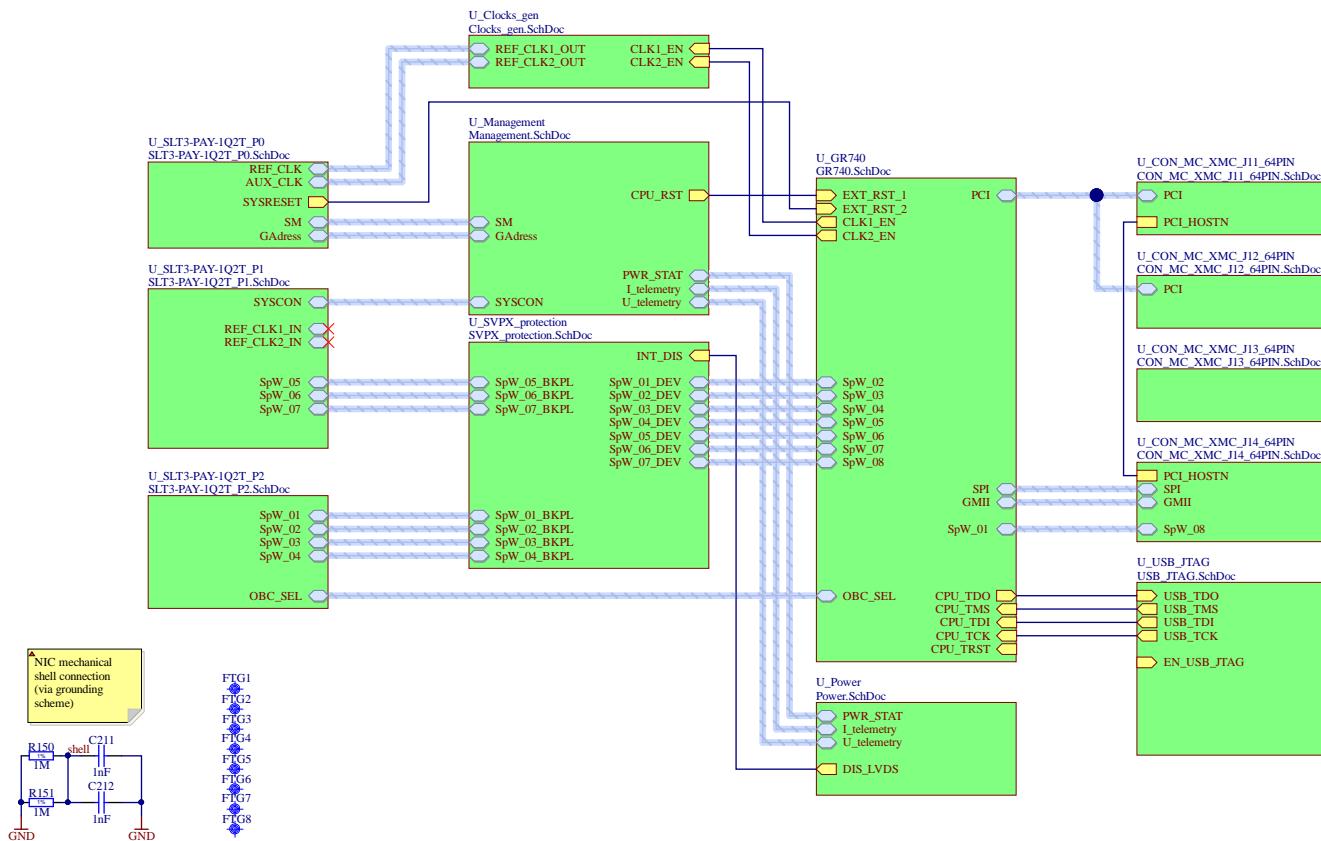
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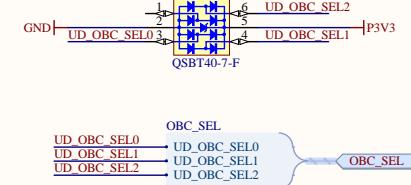
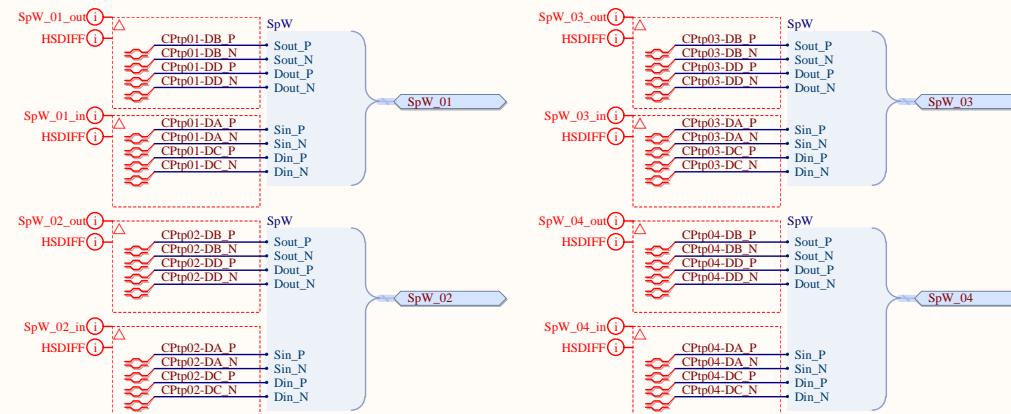
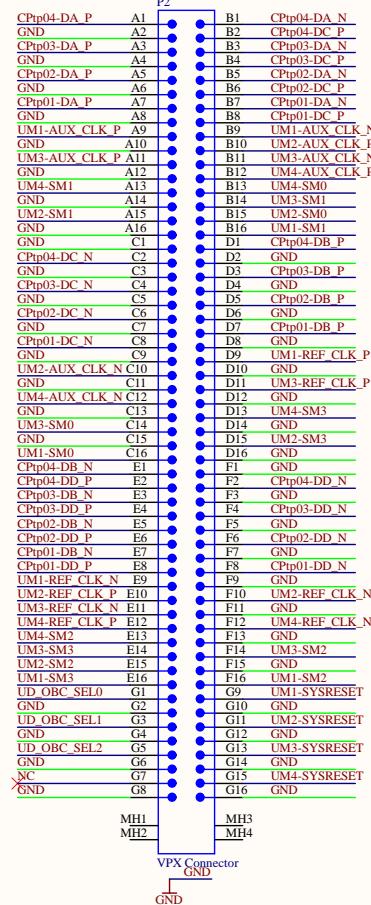
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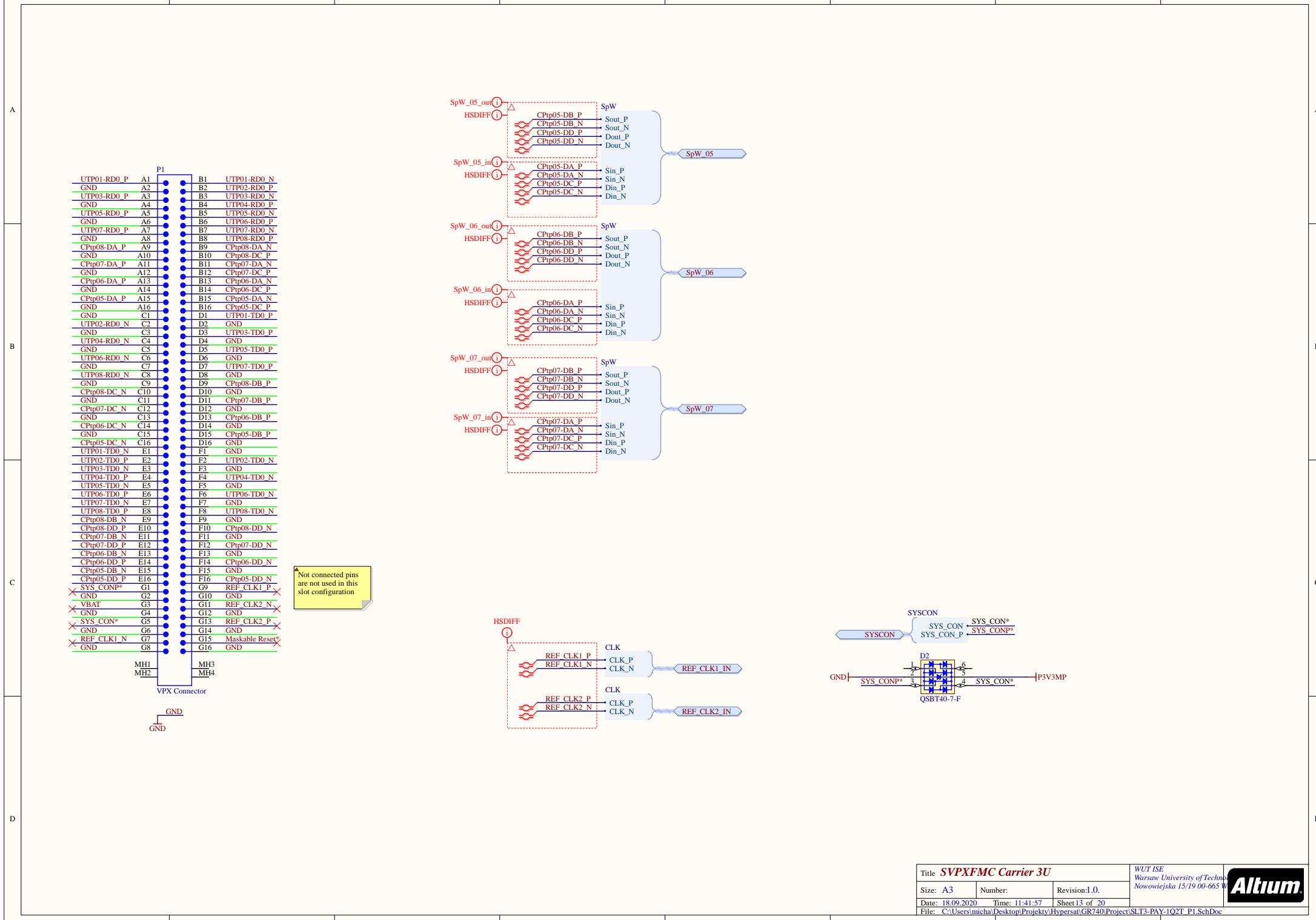


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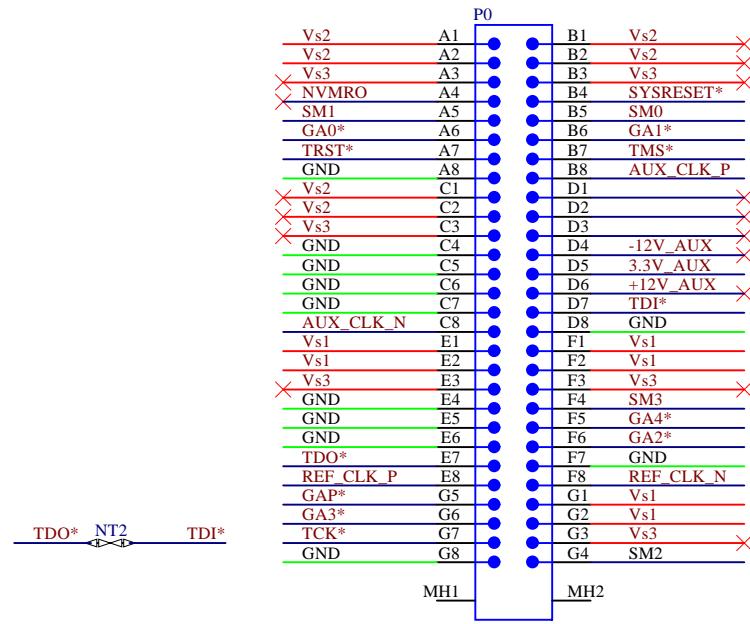
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Designer	G.Kasprowicz	Drawn by	T.Przywozki
Document		Check by	\
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Print Date	18.09.2020 11:41:57	Sheet	1 of 20
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Not connected pins  
are not used in  
this slot configuration

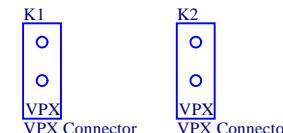




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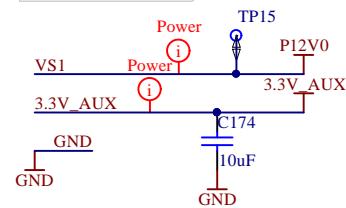


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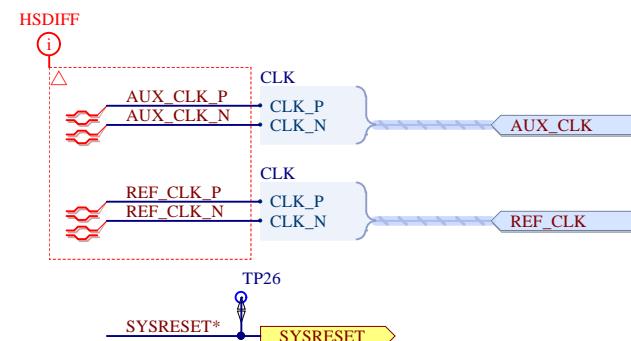
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VS1 → 12V  
VS2 → Not used  
3.3V\_AUX → 3V3



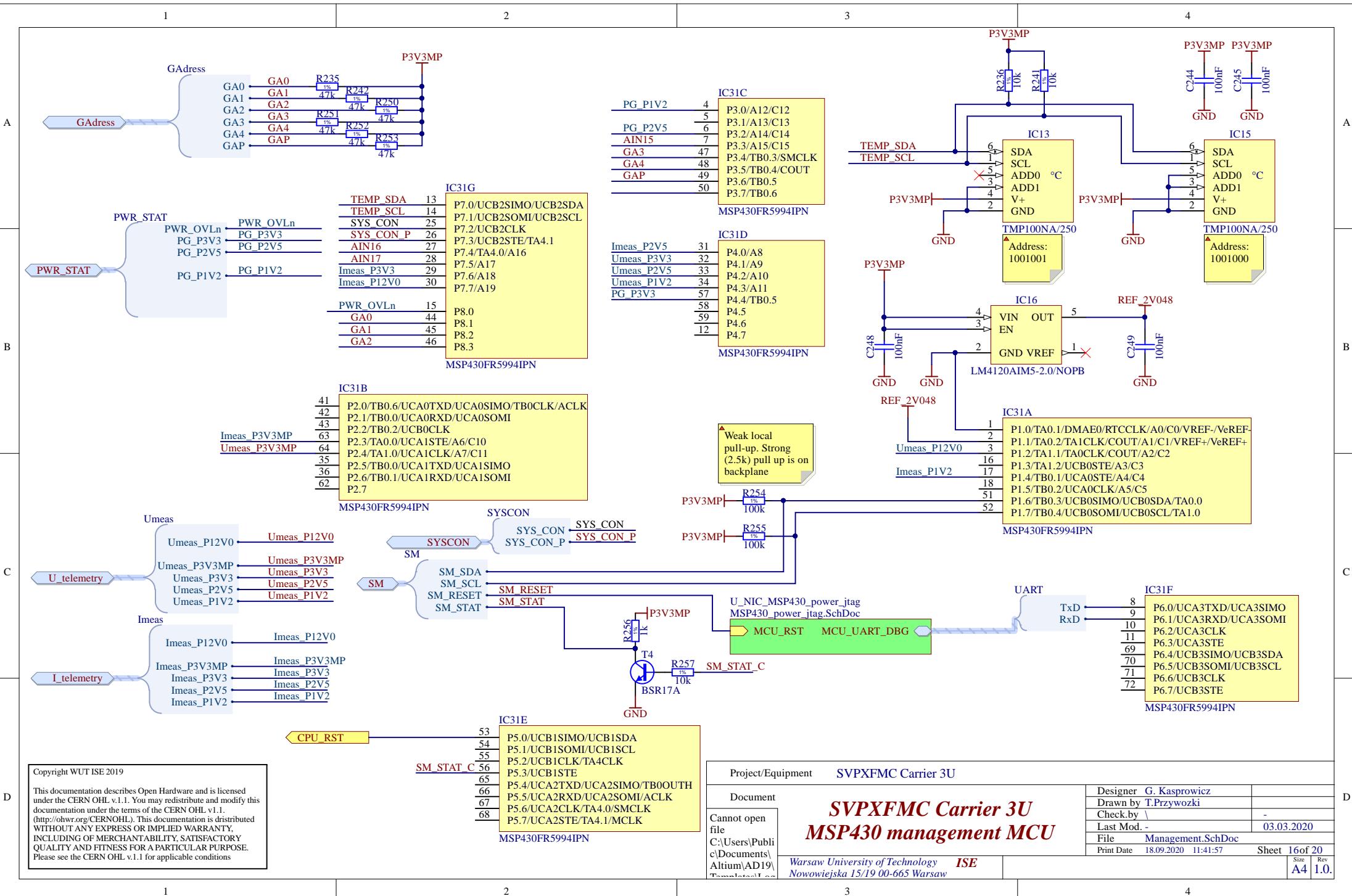
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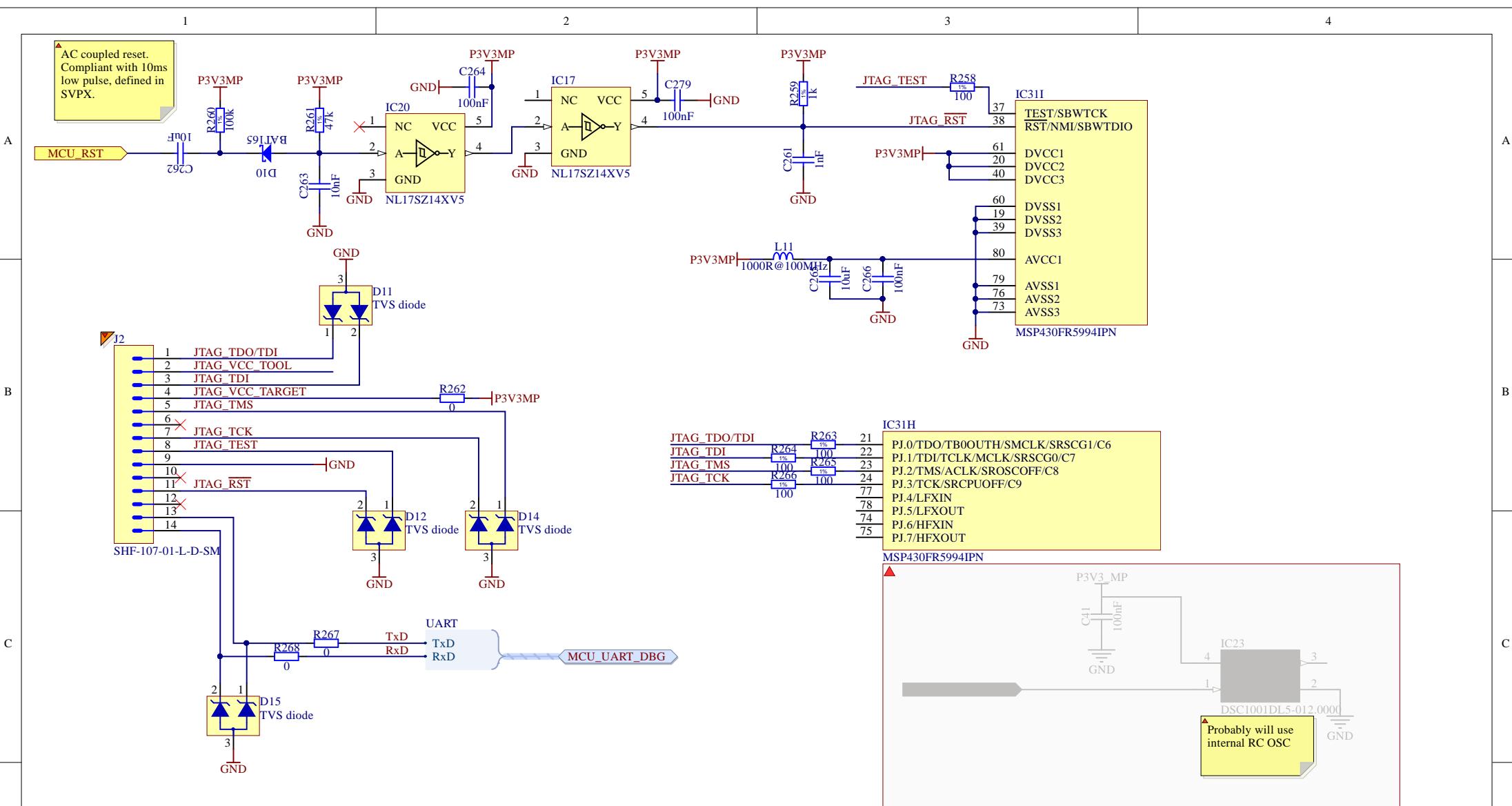


Project/Equipment SVPXFMC Carrier 3U

## SVPXFMC Carrier 3U SpaceVPX P0, SLT3-PAY-1Q2T

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Warsaw University of Technology ISE Nowowiejska 15/19 00-665 Warsaw			
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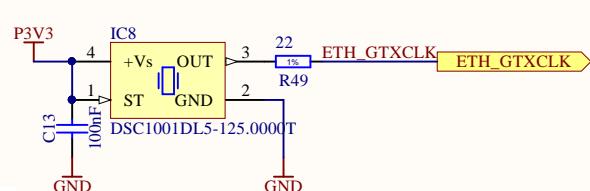
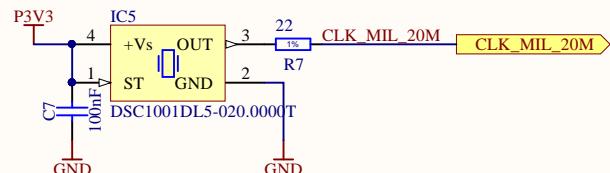
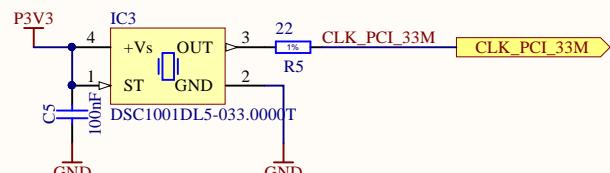
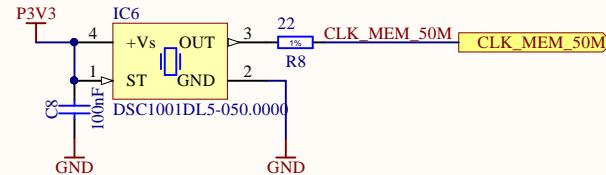
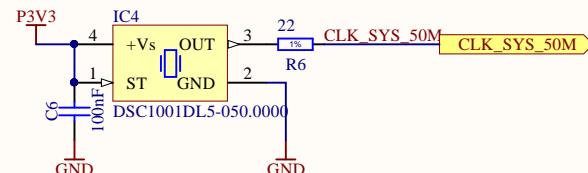
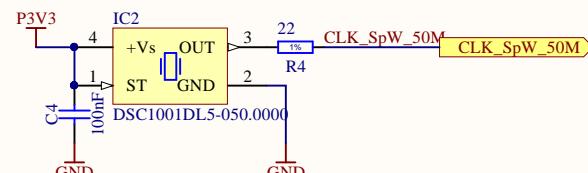


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	File	MSP430_power_jtag.SchDoc	
	Print Date	18.09.2020 11:41:58	Sheet 17 of 20
	Size	A4	Rev 1.0.

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Clock input	Description	Recommended frequency
SYS_CLK	System clock input. A clock based on this clock input via PLL (unless PLL is bypassed) is used to clock the processors, on-chip buses and on-chip peripherals.	50 MHz
MEM_EXTCLK	Alternative memory interface clock. Clock that either directly, or through a PLL, provides an alternative clock for the SDRAM memory interface. See description in table 23, section 3.1.	50 MHz
SPW_CLK	SpaceWire clock. Clock that either directly, or through a PLL (recommended operating mode), provides a clock for the SpaceWire interfaces. See also sections 13.3.1.2 and 13.3.2.	50 MHz
JTAG_TCK	JTAG clock	10 MHz
ETH0_GTXCLK	Ethernet Gigabit MAC 0 clock	125 MHz
ETH0_TXCLK	Ethernet MAC 0 transmit clock	25 MHz
ETH0_RXCLK	Ethernet MAC 0 receive clock	25 MHz (MII) 125 MHz (GMII)
ETH1_GTXCLK	Ethernet Gigabit MAC 1 clock	125 MHz
ETH1_TXCLK	Ethernet MAC 1 transmit clock	25 MHz
ETH1_RXCLK	Ethernet MAC 1 receive clock	25 MHz (MII) 125 MHz (GMII)
PCI_CLK	PCI interface clock	33 MHz
GR1553_CLK	MIL-STD-1553B interface clock	20 MHz

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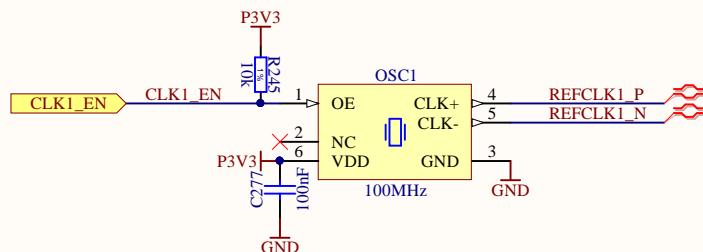
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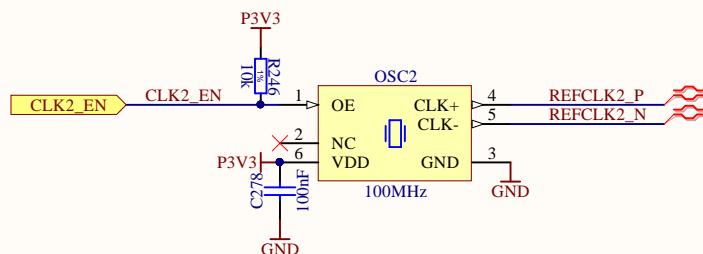
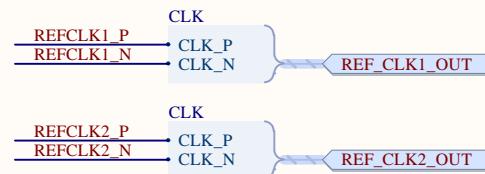
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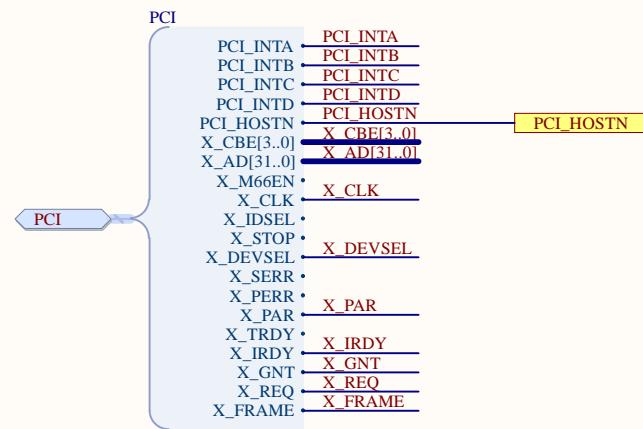
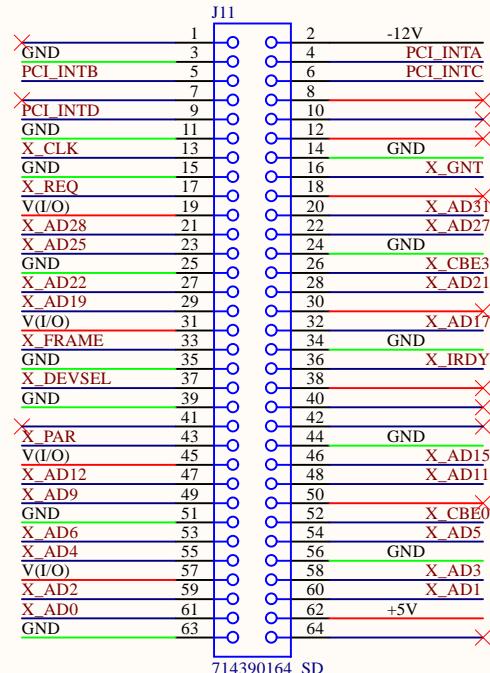
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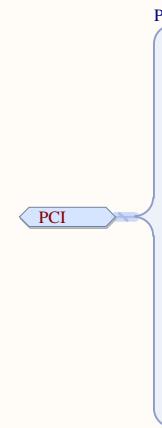
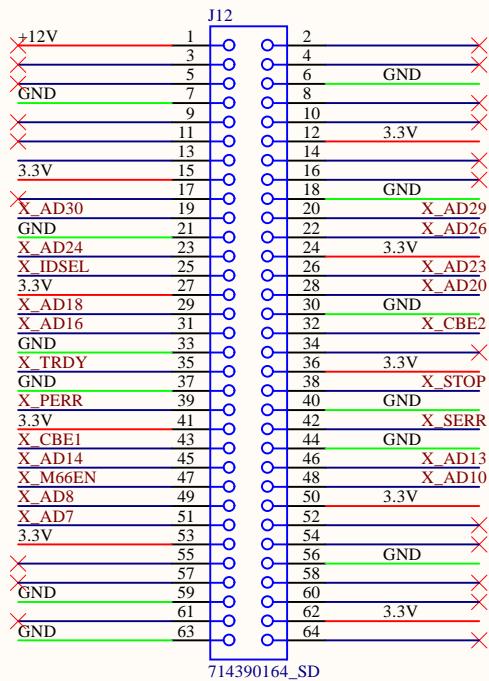
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PCI_INTA	PCI_INTA
PCI_INTB	PCI_INTB
PCI_INTC	PCI_INTC
PCI_INTD	PCI_INTD
PCI_INTE	PCI_HOSTN
PCI_HOSTN	X_CBE[3..0]
X_CBE[3..0]	X_AD[31..0]
X_AD[31..0]	X_M66EN
X_M66EN	X_CLK
X_CLK	X_IDSEL
X_IDSEL	X_STOP
X_STOP	X_DEVSEL
X_DEVSEL	X_SERR
X_SERR	X_PERR
X_PERR	X_PAR
X_PAR	X_TRDY
X_TRDY	X_IRDY
X_IRDY	X_GNT
X_GNT	X_REQ
X_REQ	X_FRAME

3.3V — P3V3  
GND — GND

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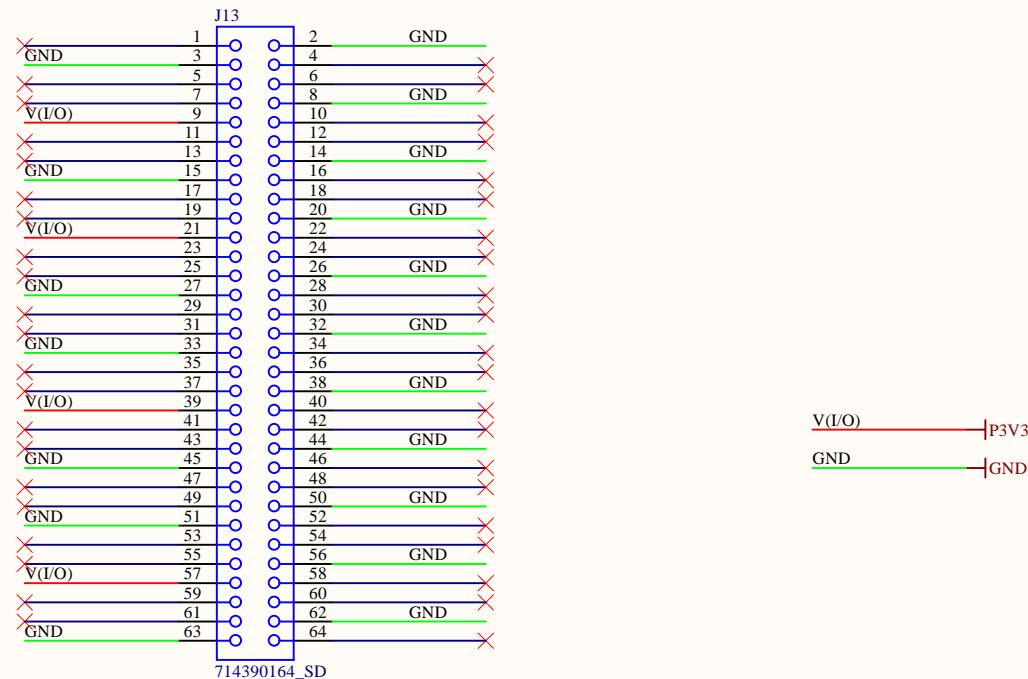
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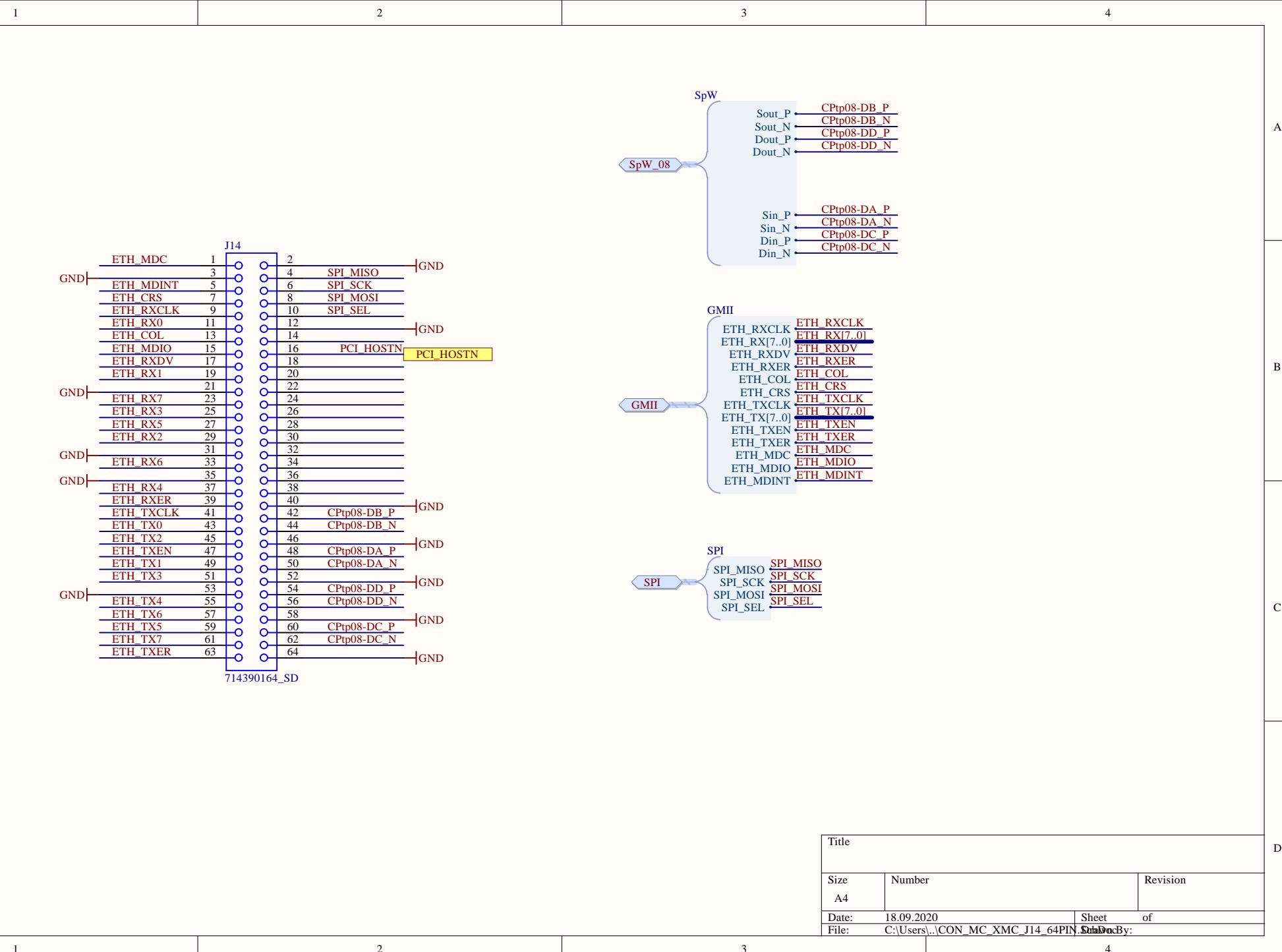
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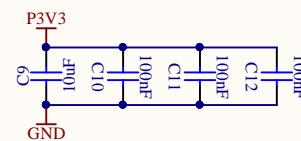
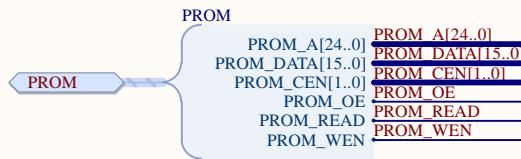
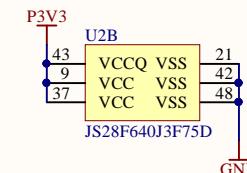
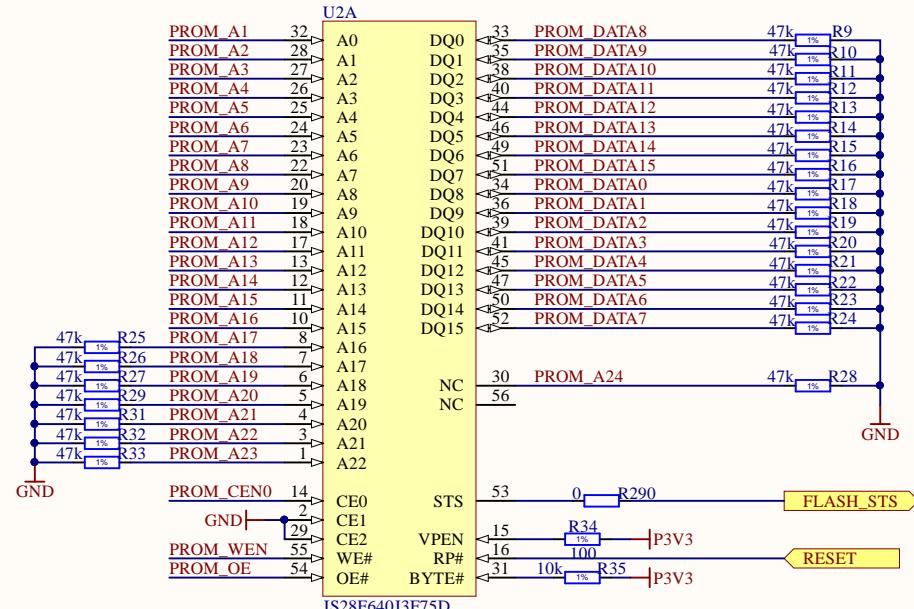
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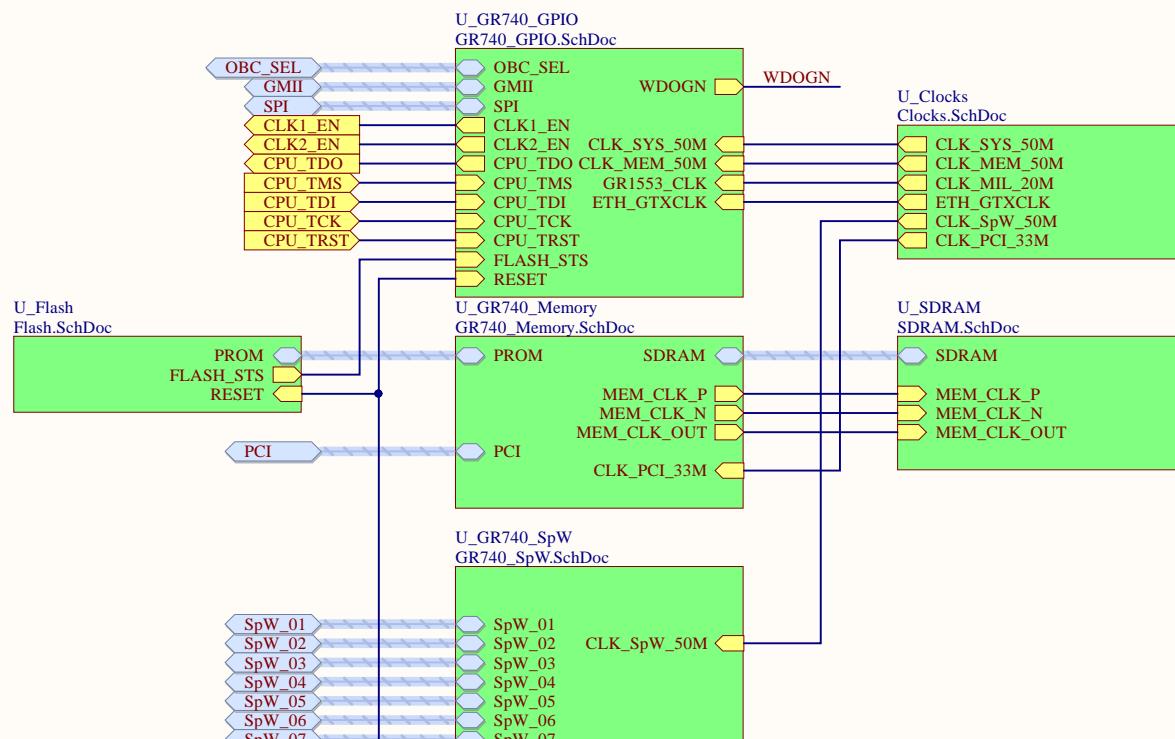
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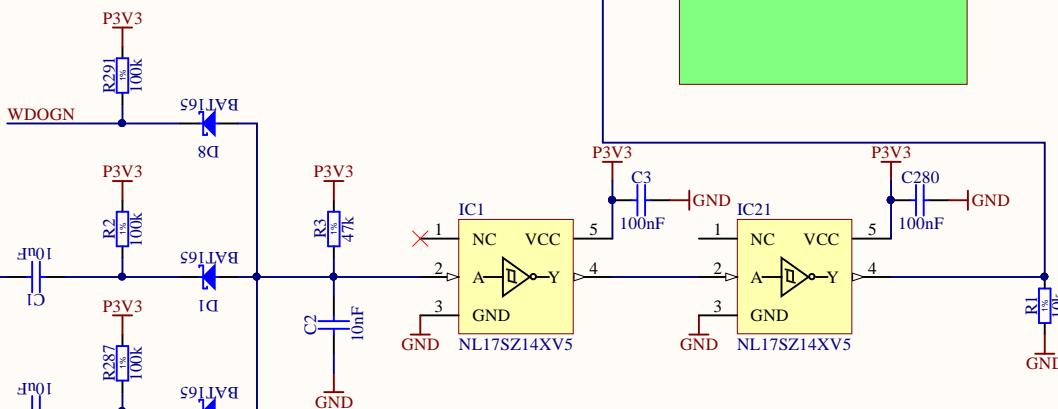
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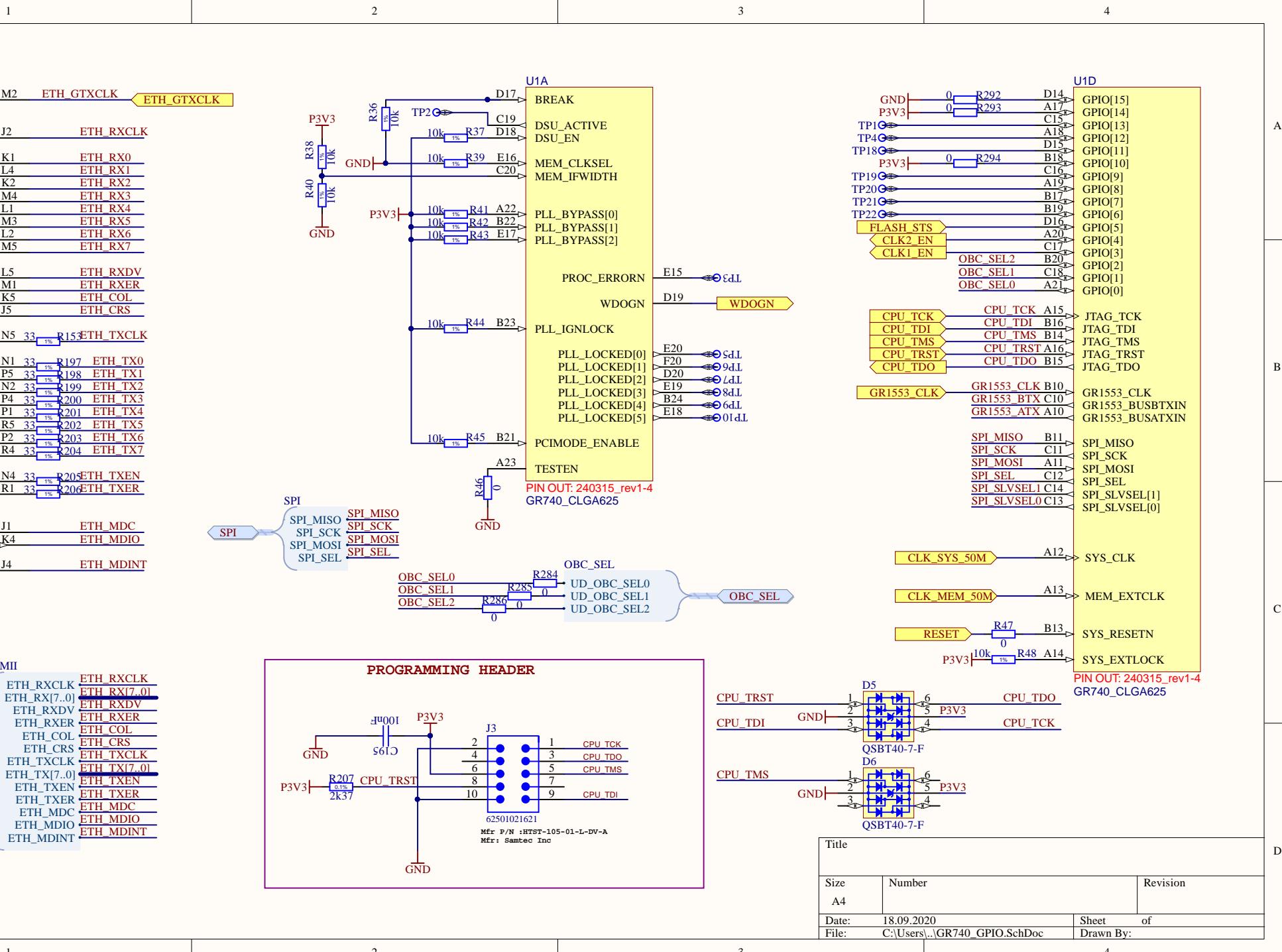


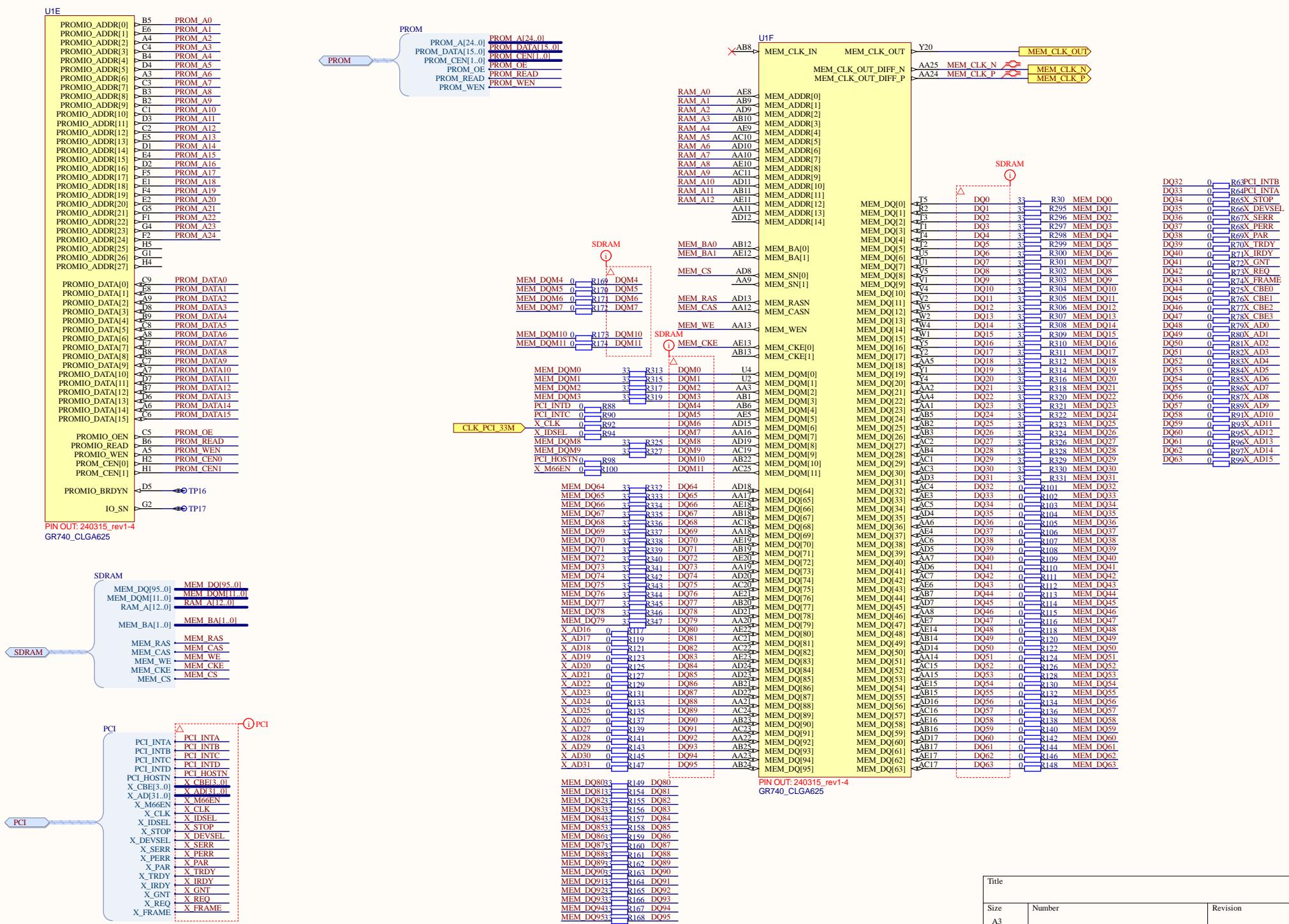
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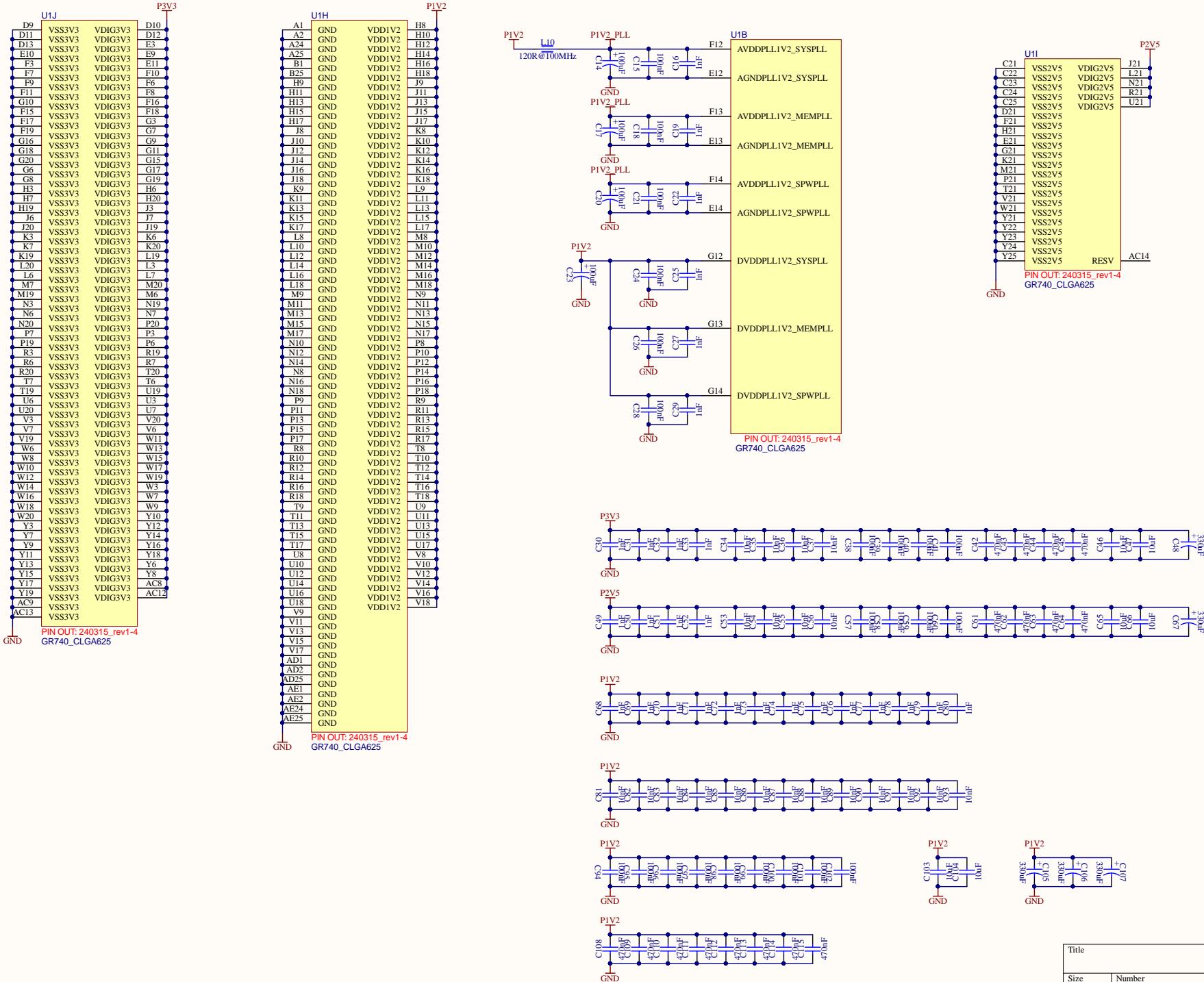
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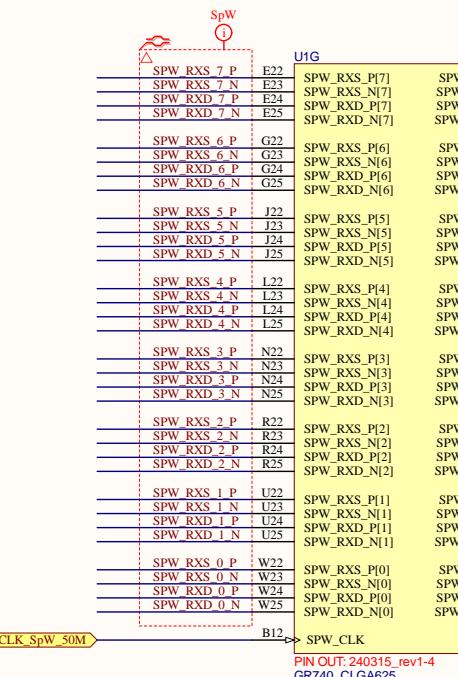




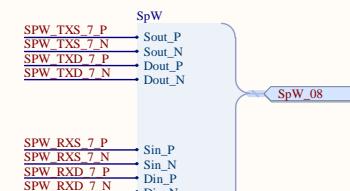
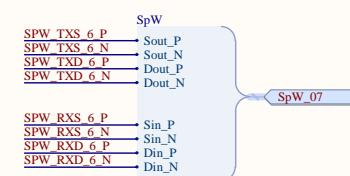
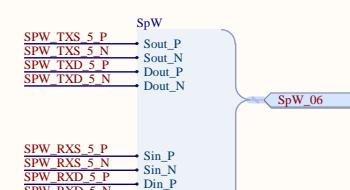
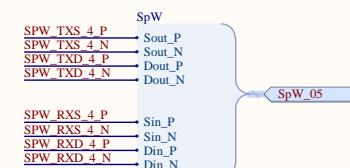
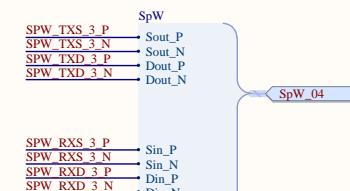
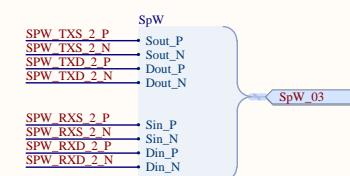
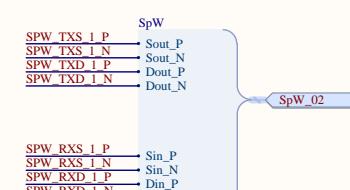
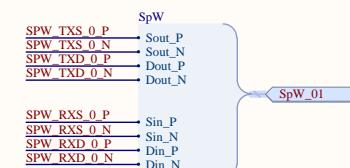
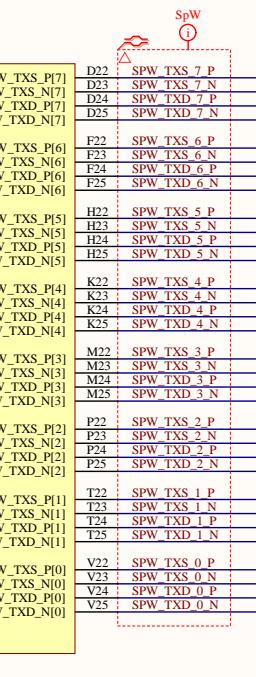


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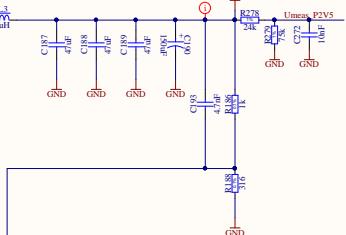
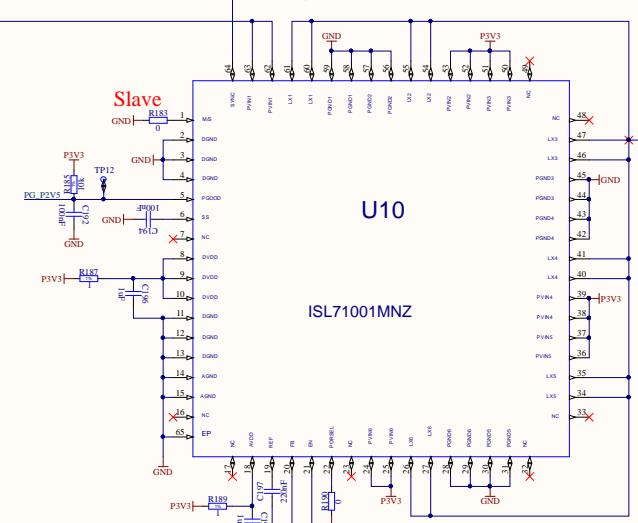
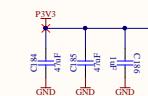
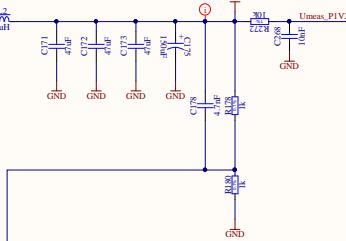
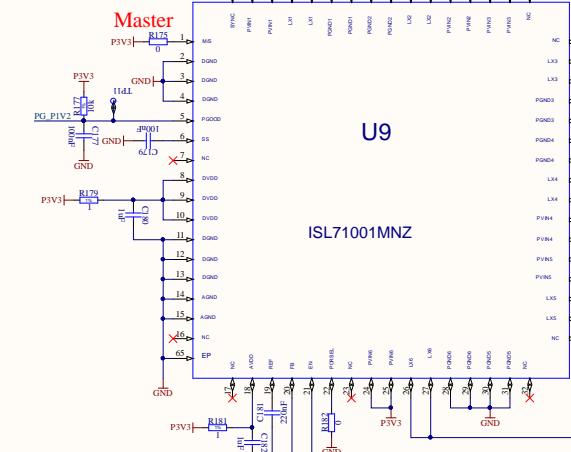
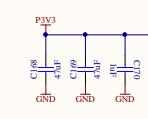
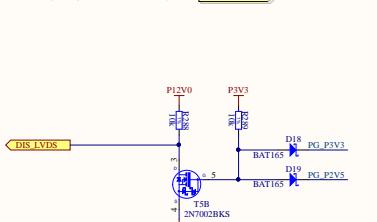
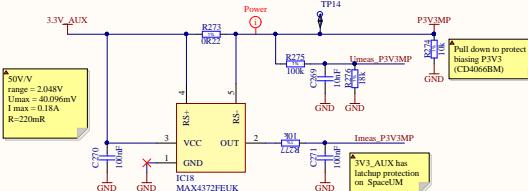
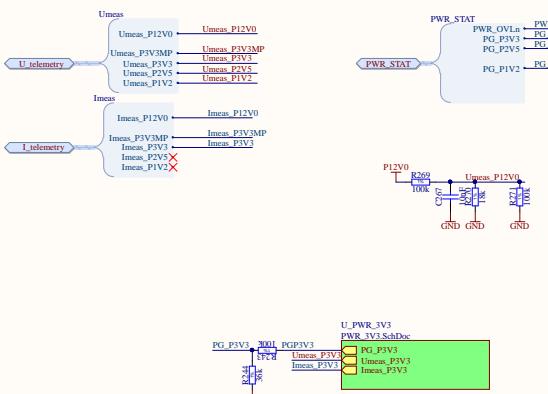


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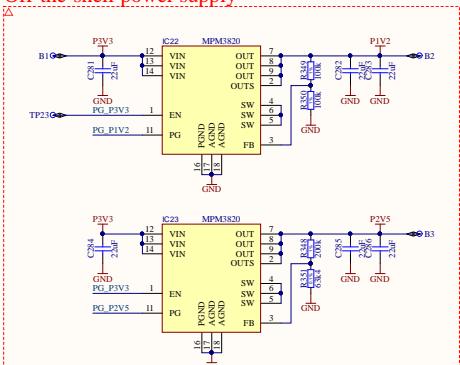


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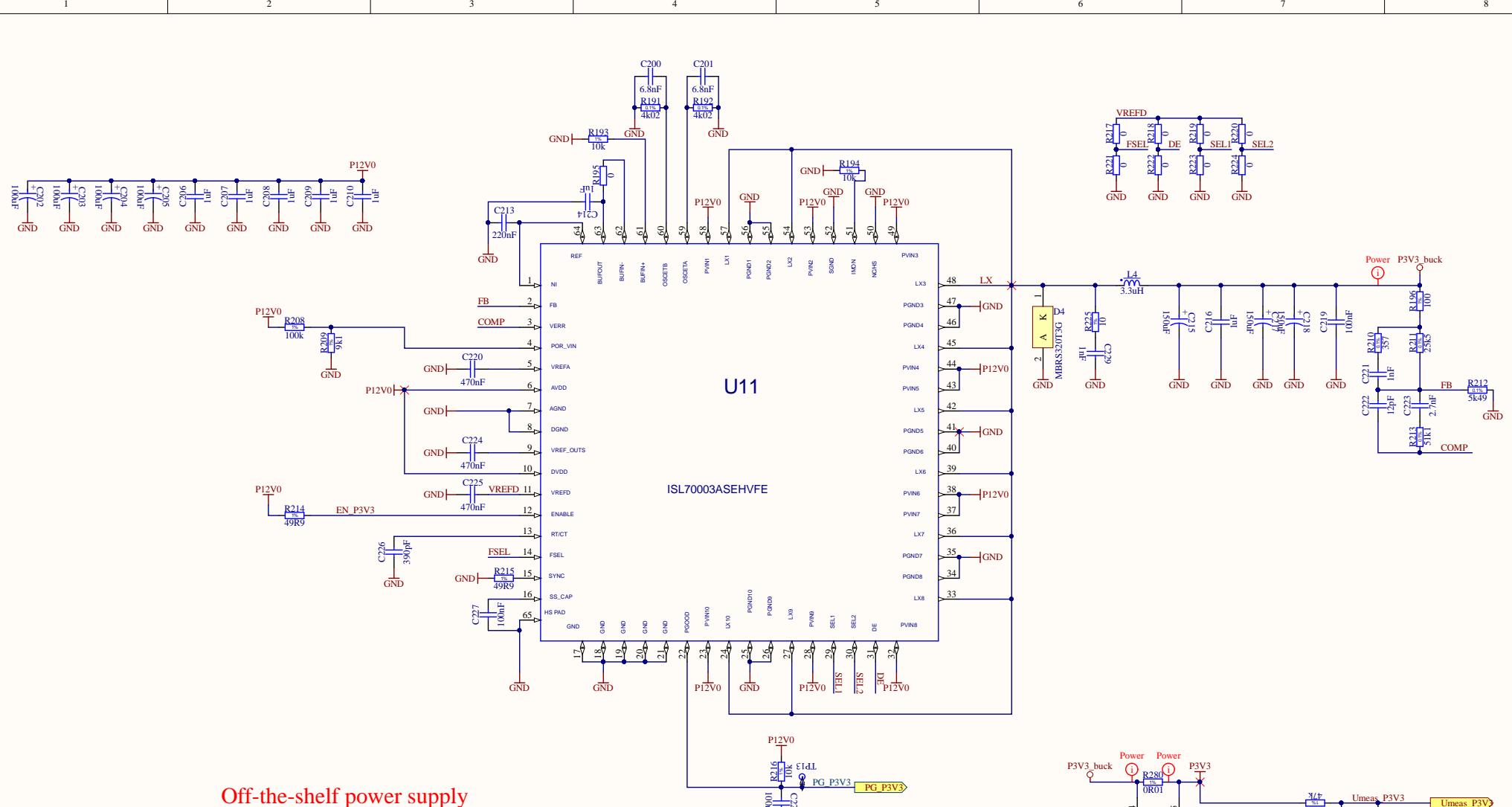
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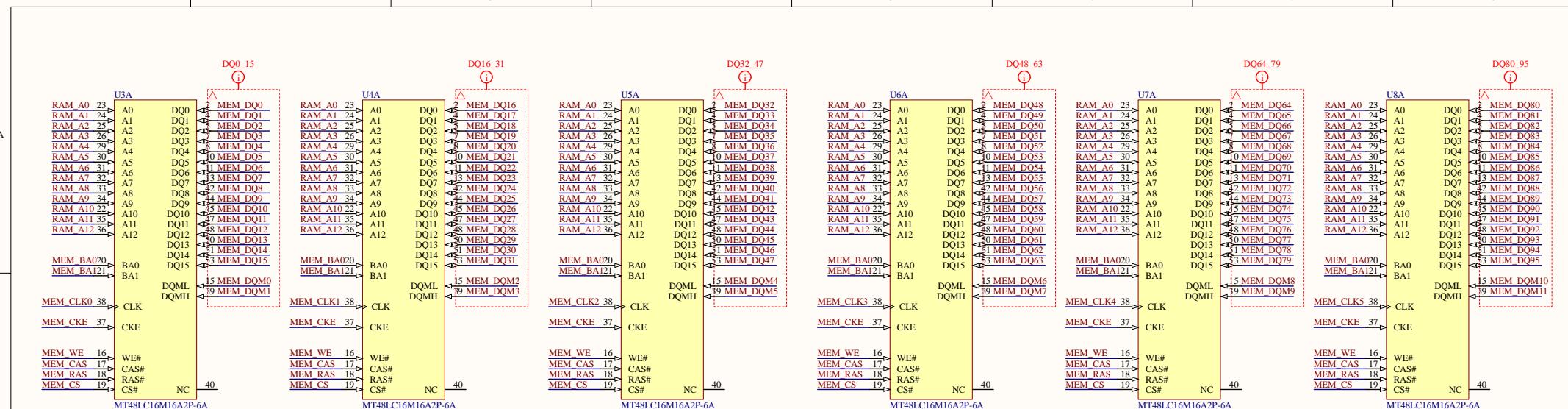
## Off-the-shelf power supply



Title		
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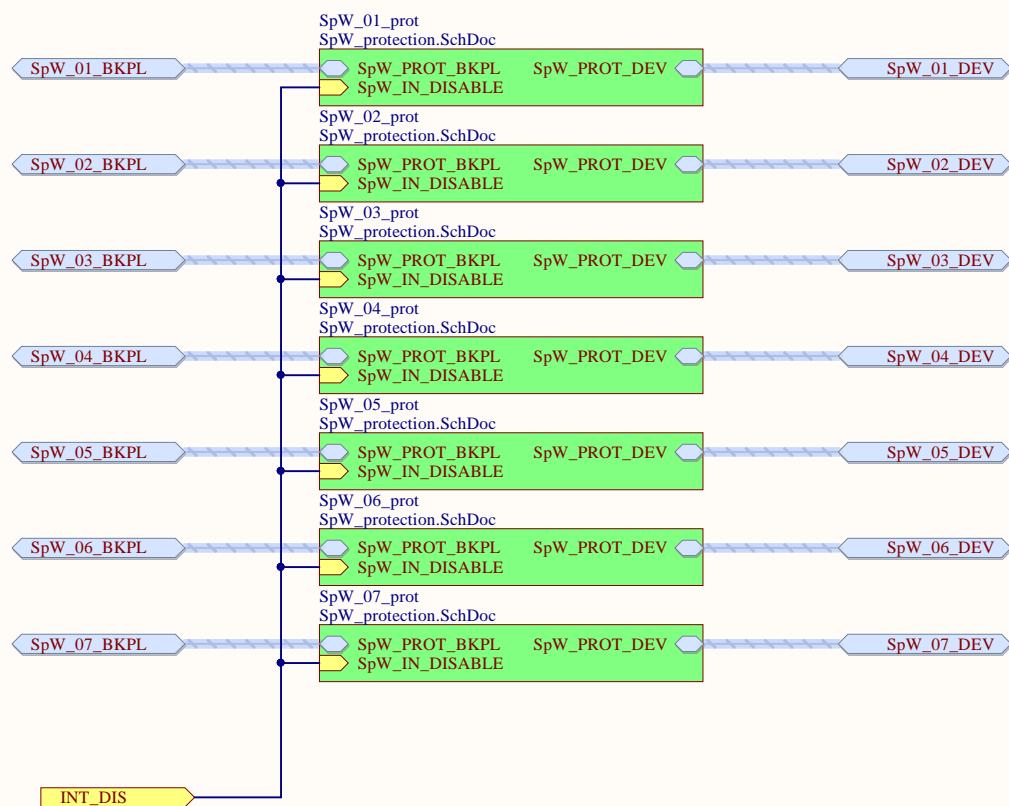
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Title		
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A3		
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File:	C:\Users\...\SDRAM.SchDoc	Drawn By:

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▲ Short incoming LVDS lines to GND in case of latch-up to prevent any input current.

**Title *SpaceVPX interface protection***

Size: **A4** Number: Revision:

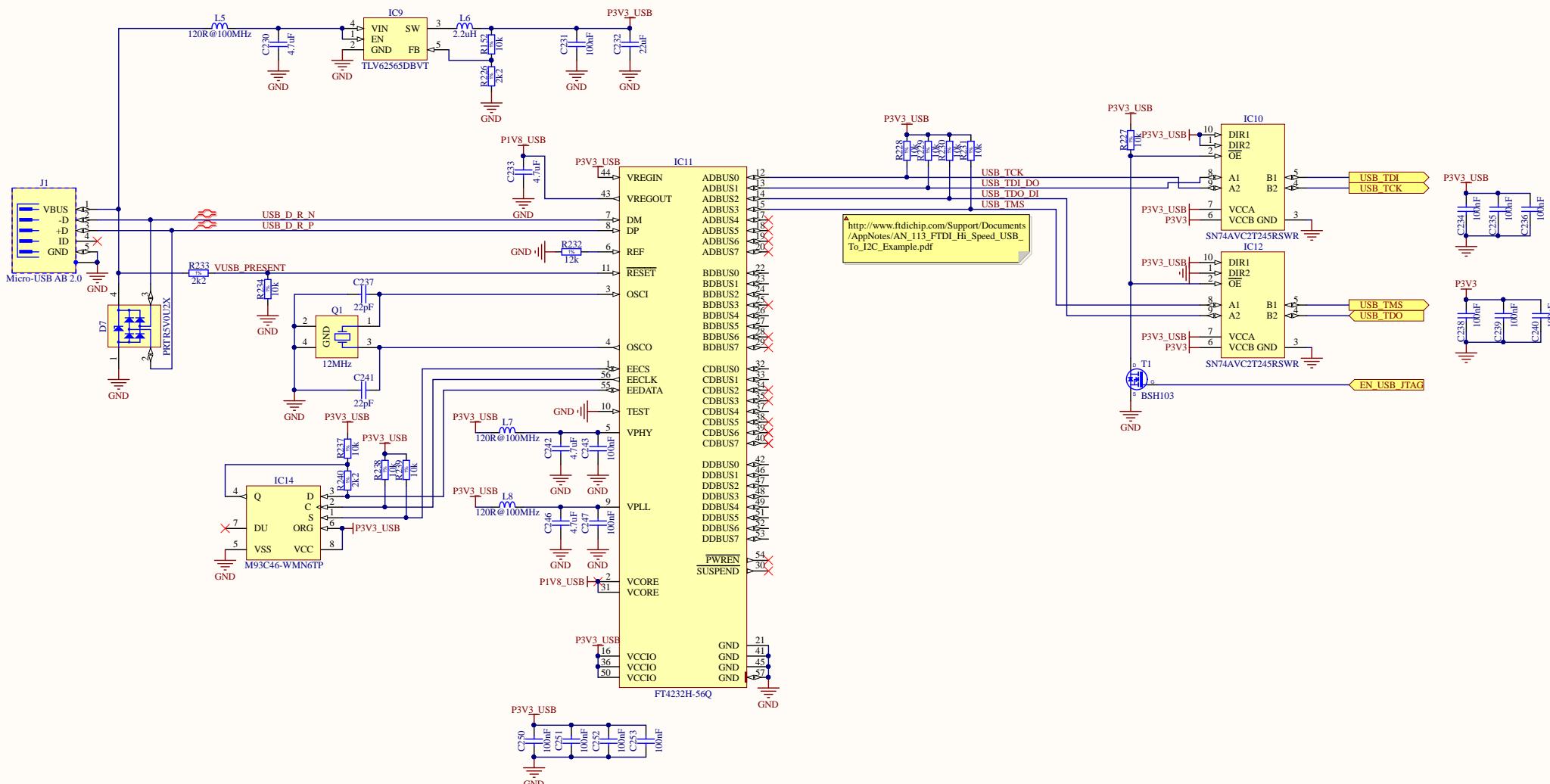
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*Createch Instruments*  
Gen. L. Okulickiego 7/9  
05-500 Piaseczno  
Poland

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Title		
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A3		
Date:	18.09.2020	Sheet of
File:	C:\Users...\USB JTAG.SchDoc	Drawn By: