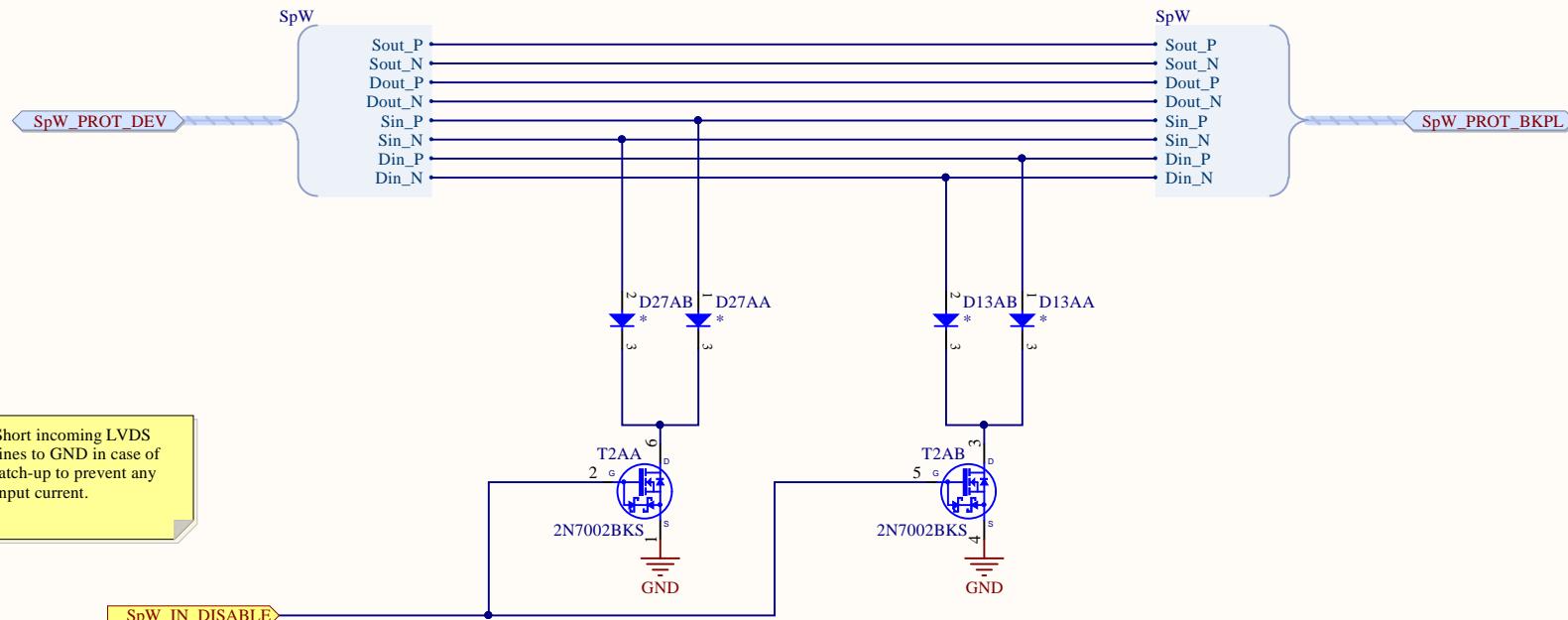


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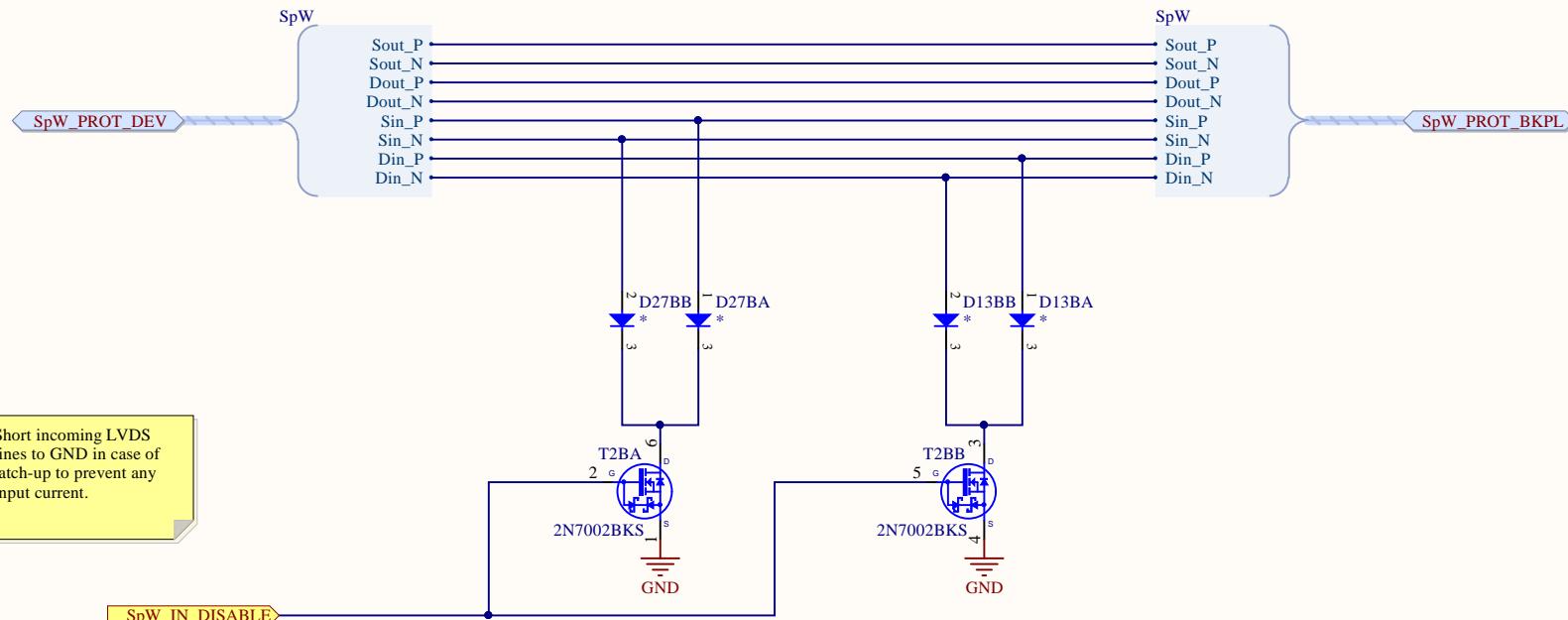
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 Createch Instruments
 Gen. L. Okulickiego 7/9
 05-500 Piaseczno
 Poland

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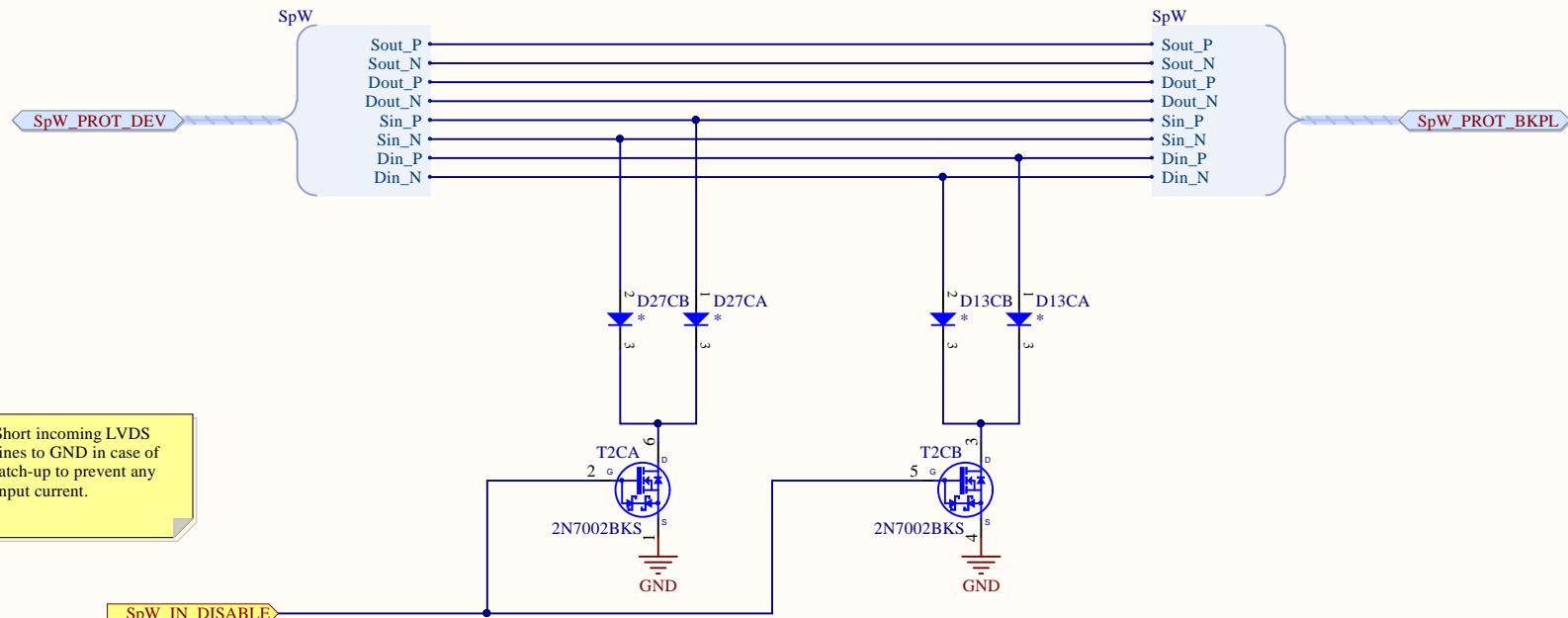
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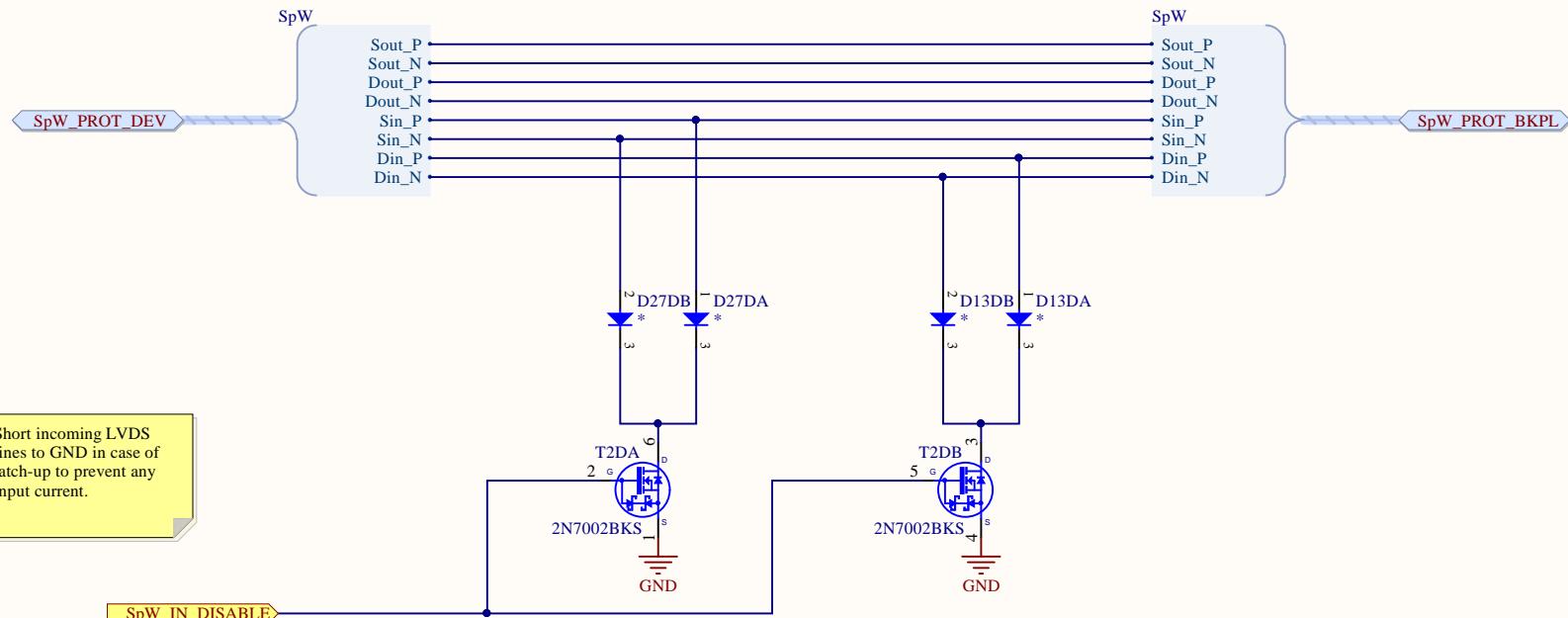
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Gen. L. Okulickiego 7/9
05-500 Piaseczno
Poland

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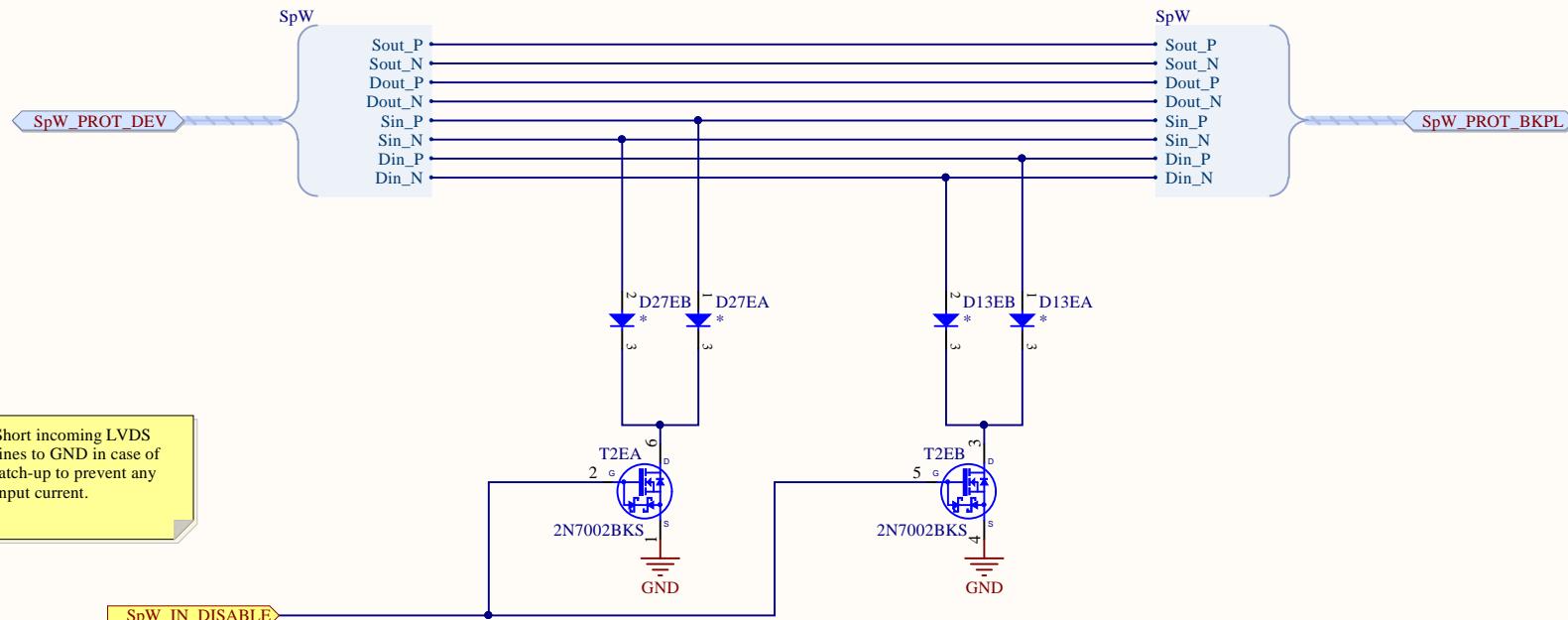
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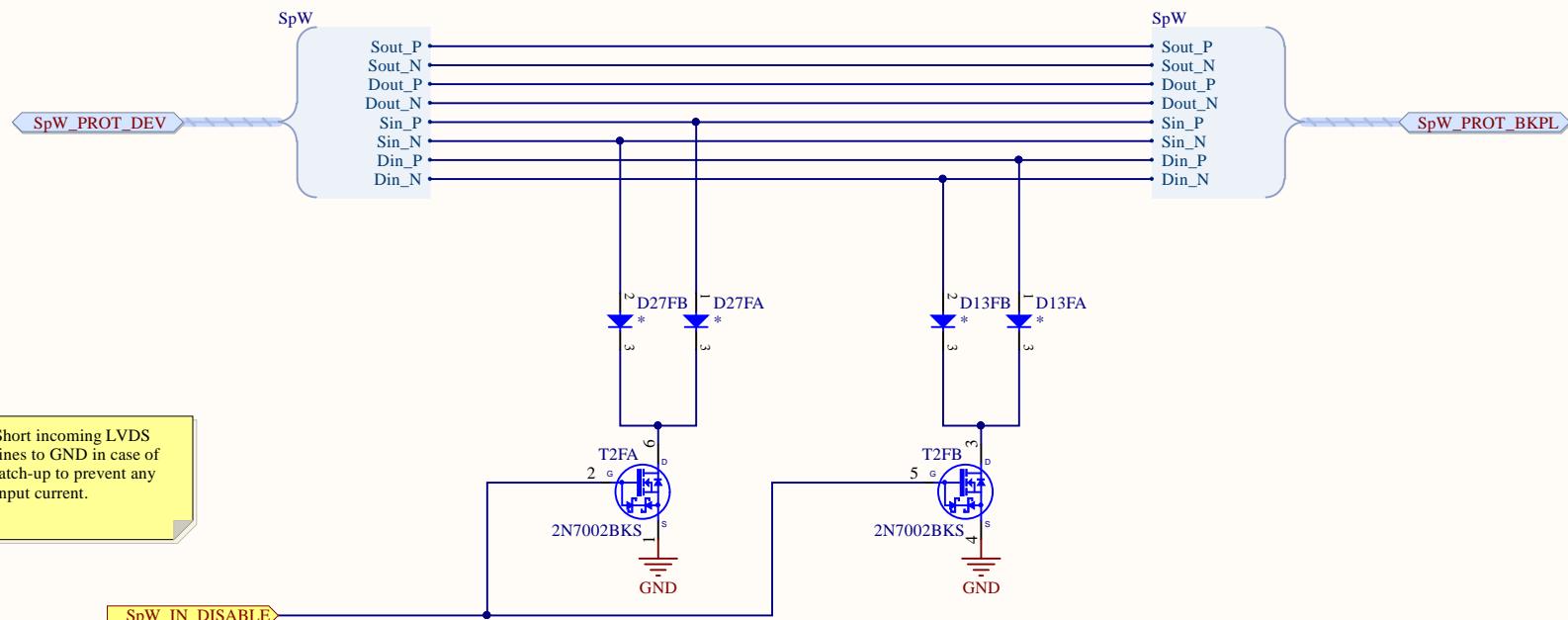
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05-500 Piaseczno
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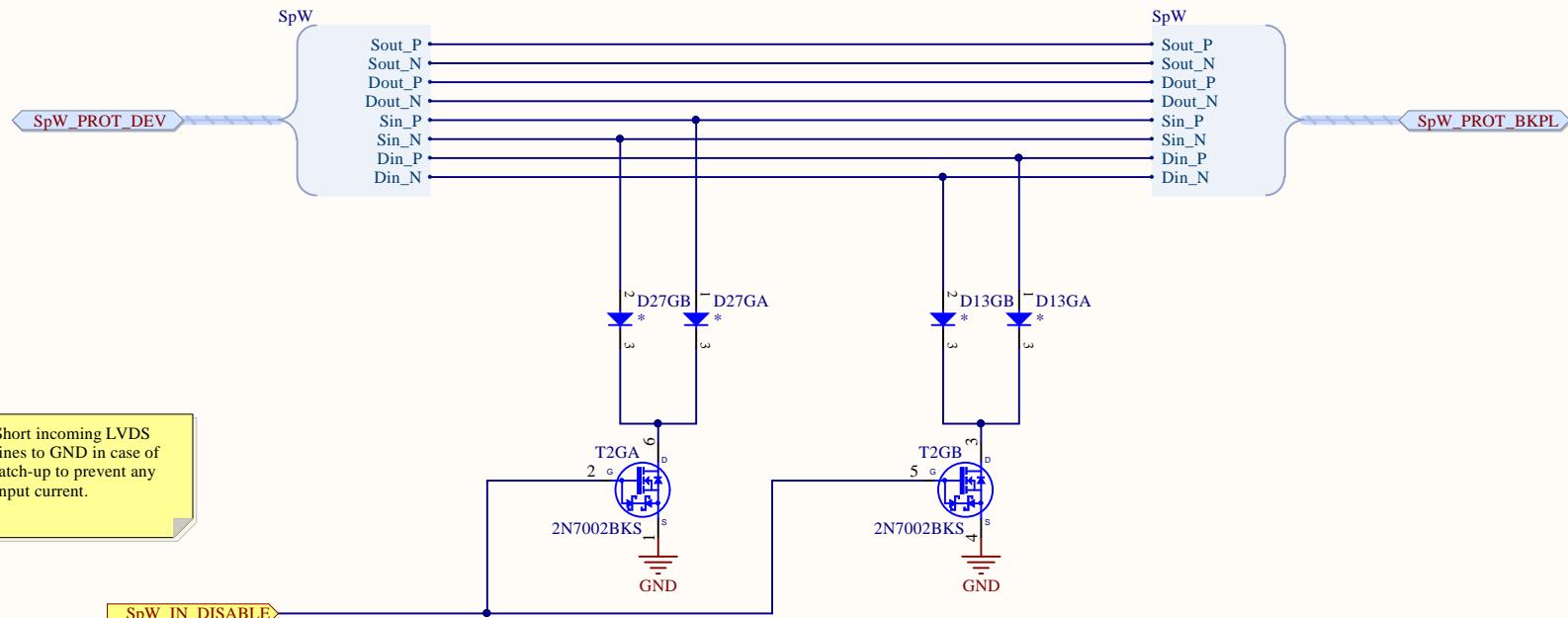
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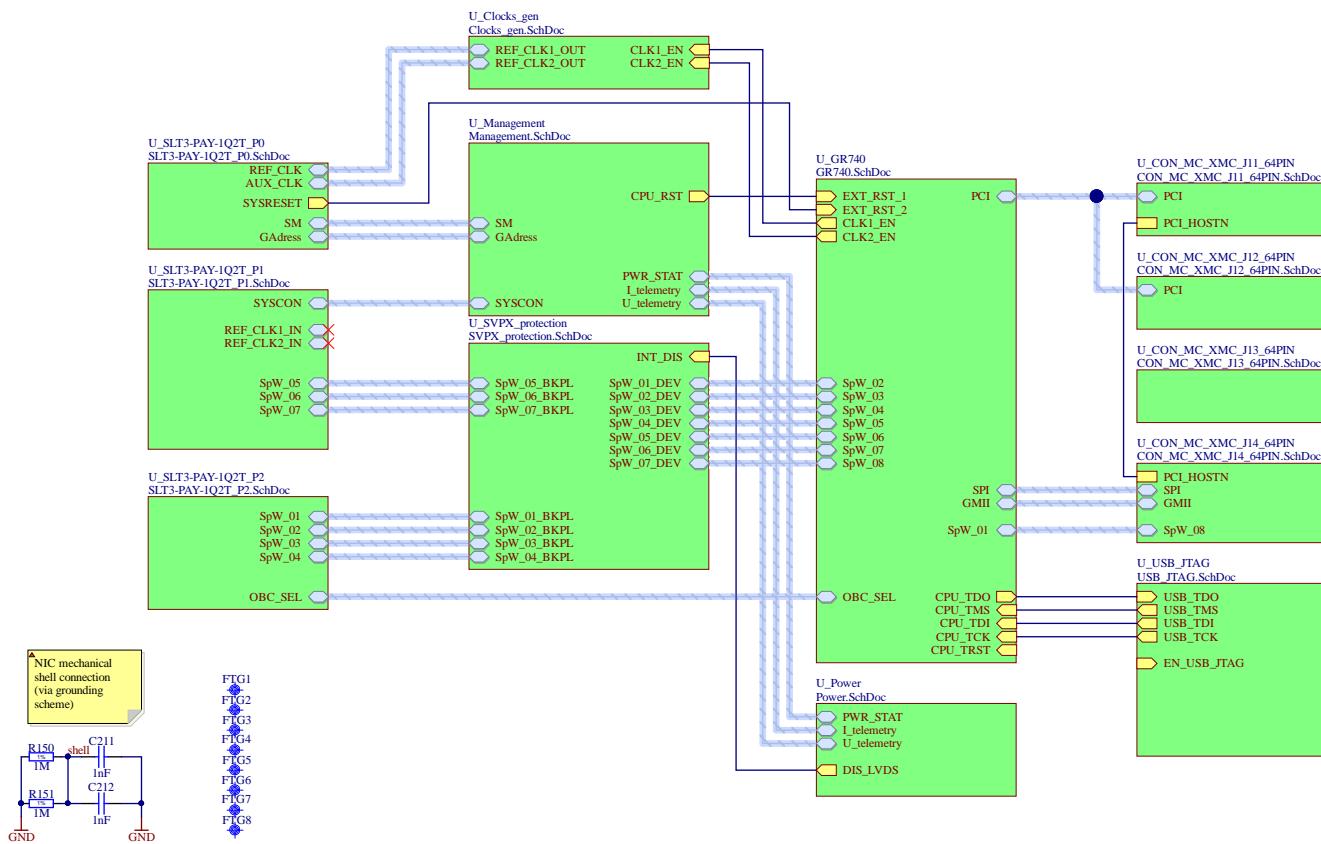
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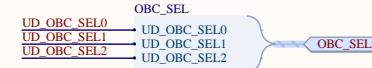
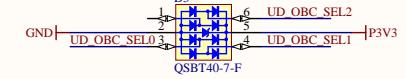
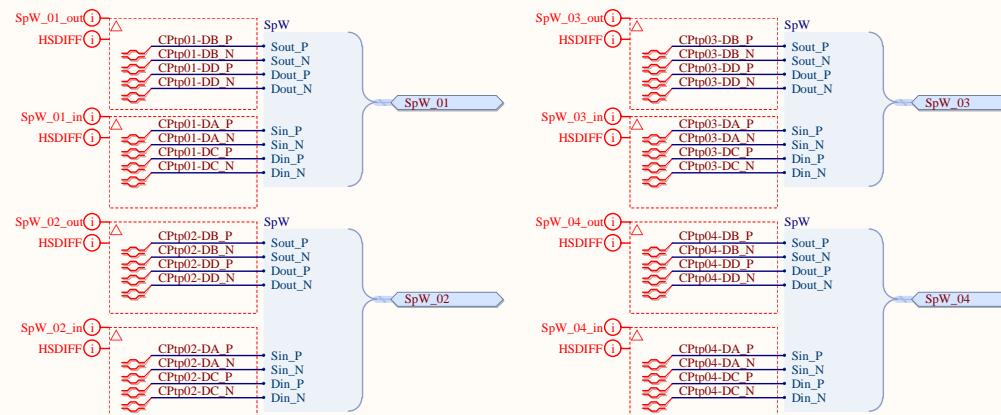
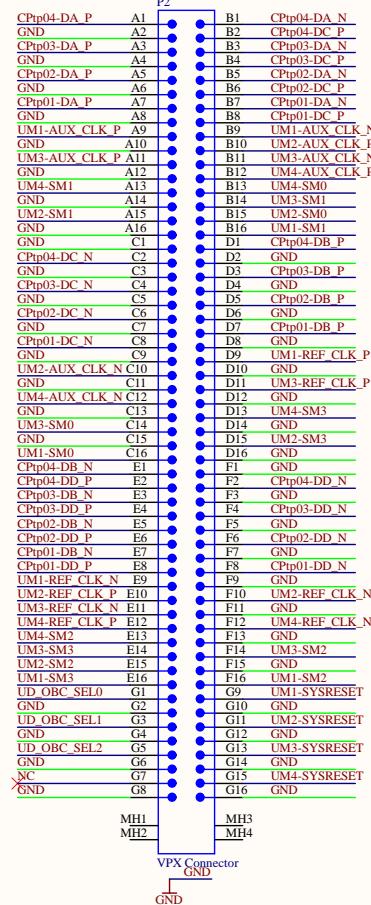


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<http://ohwr.org/CERNOHL>. This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

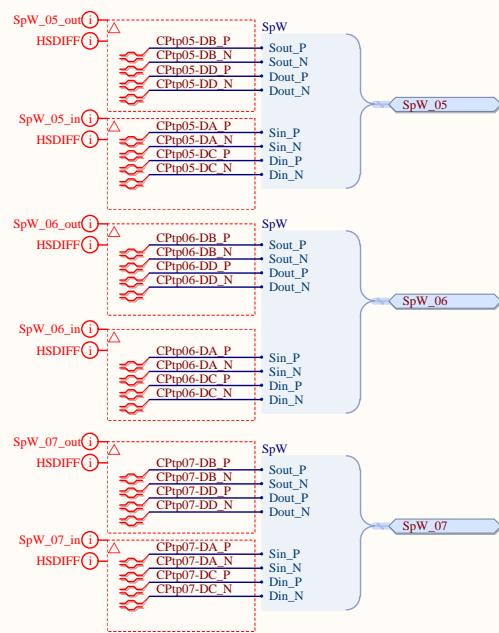
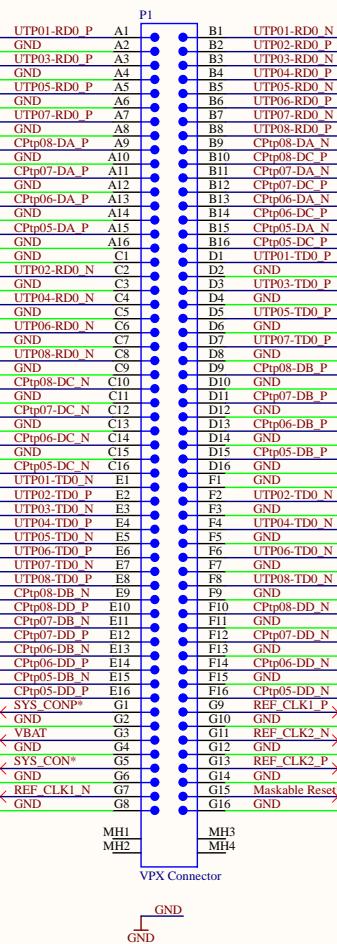
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SVPXFMC Carrier 3U		Top	
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Warsaw University of Technology ISE

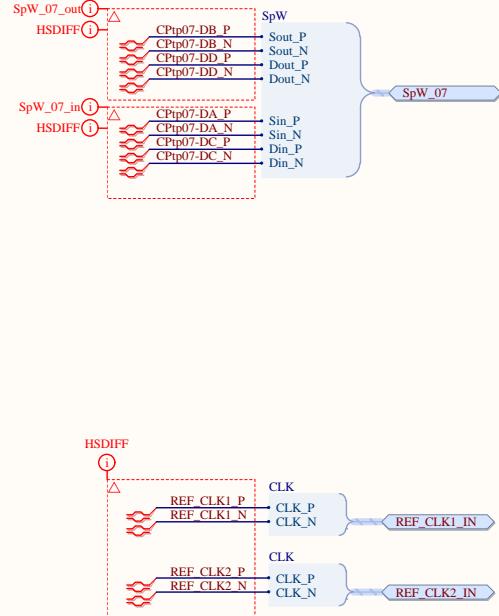
Not connected pins
are not used in
this slot configuration



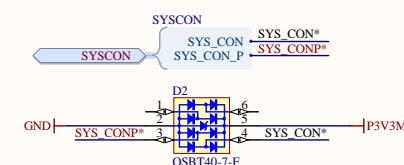
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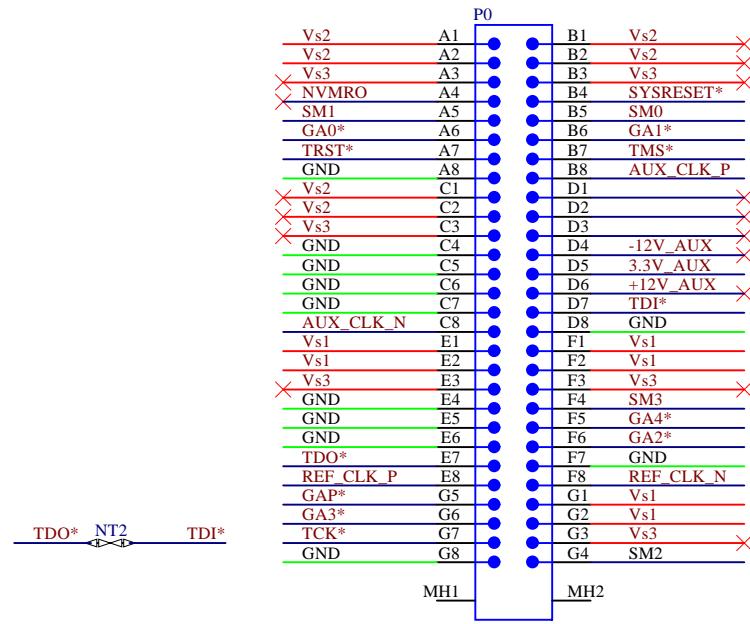


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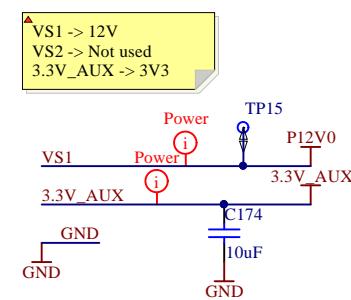


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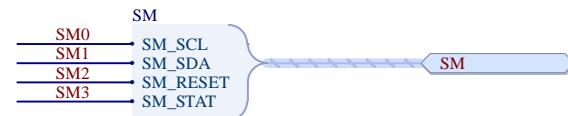
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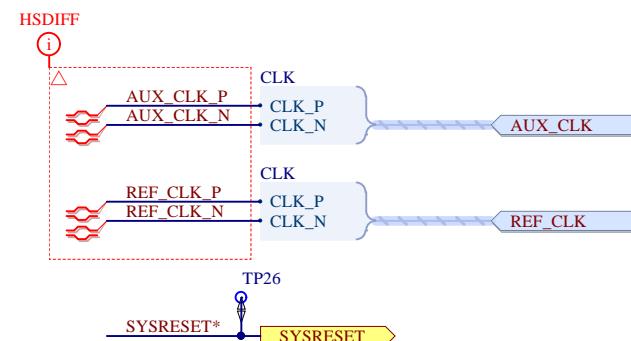
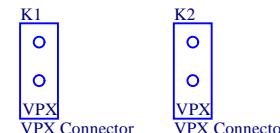
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Pins D1-D3 are not physically connected to pad



C



D

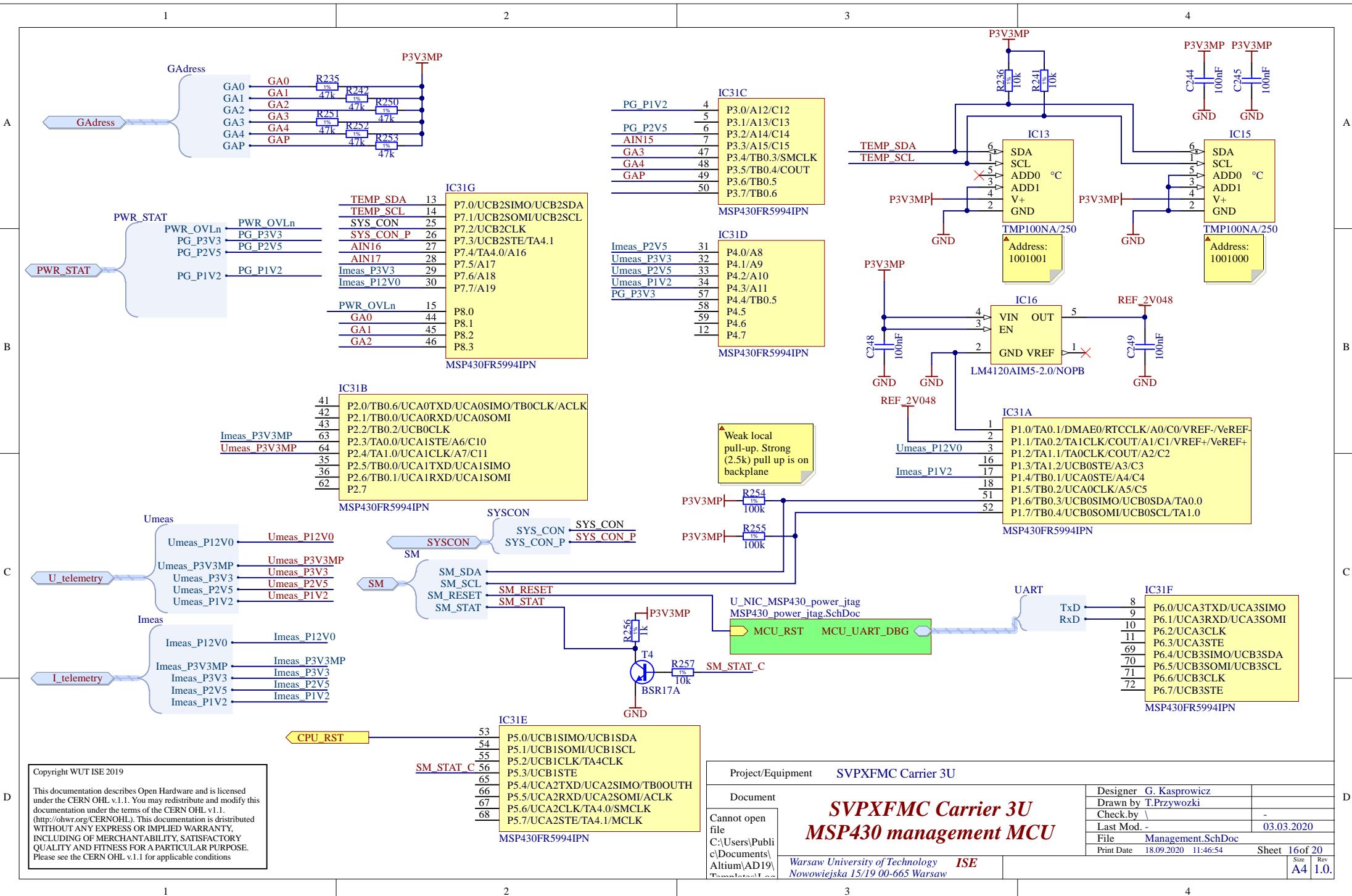
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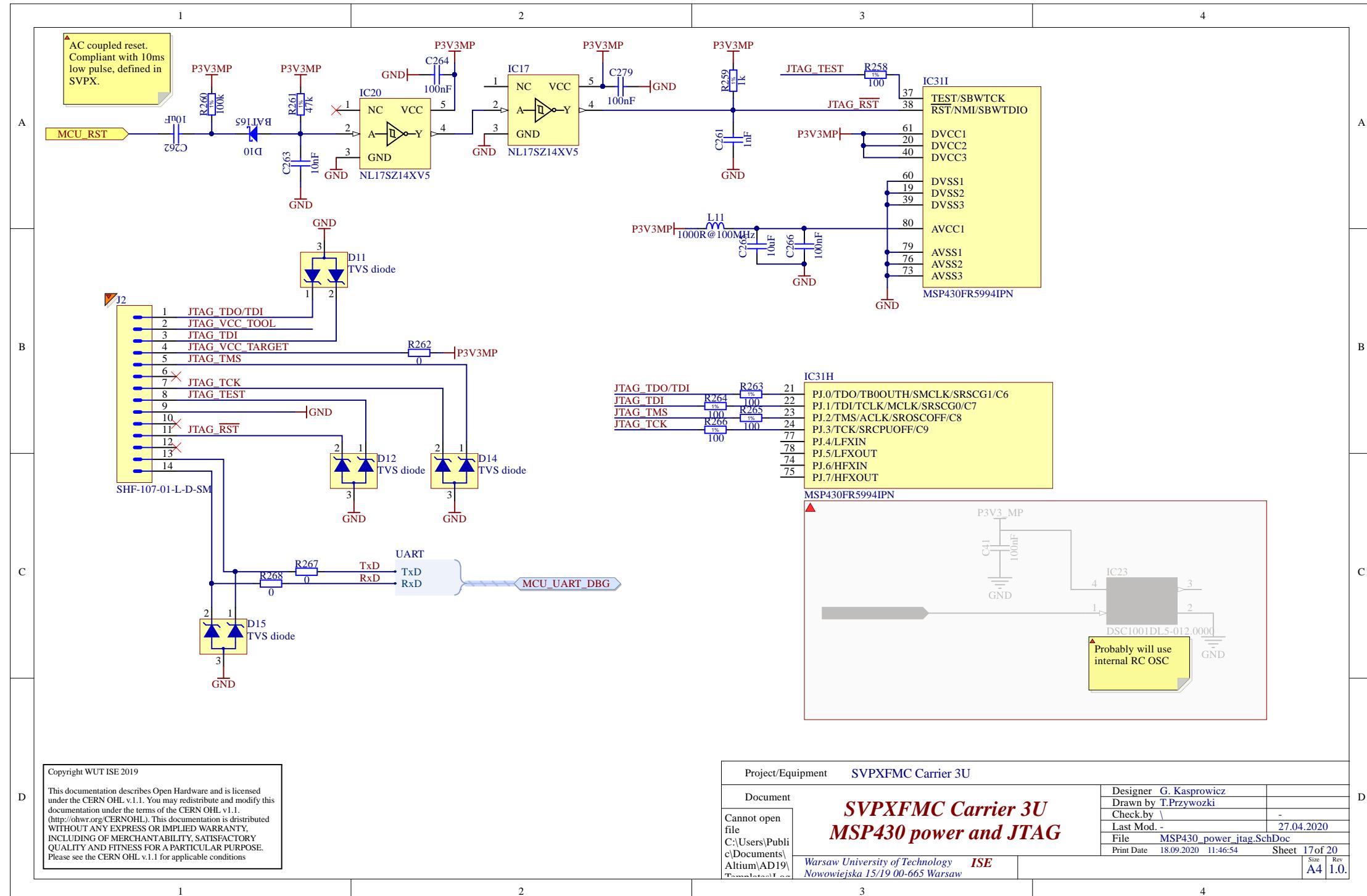
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Project/Equipment SVPXFMC Carrier 3U

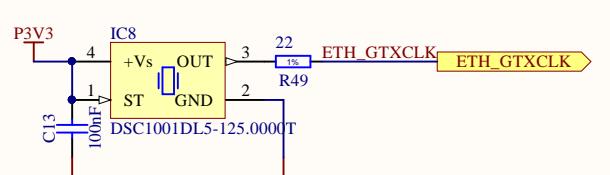
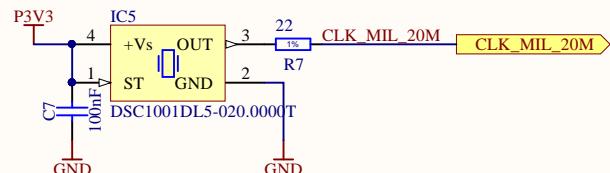
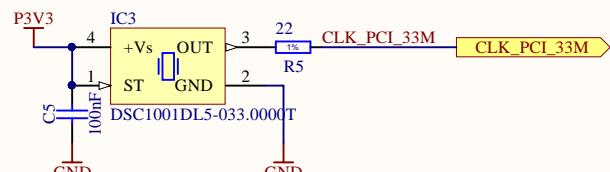
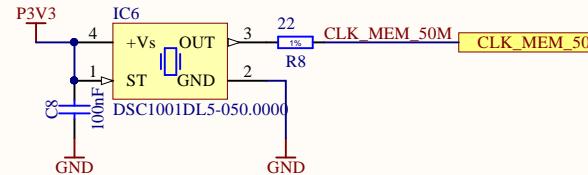
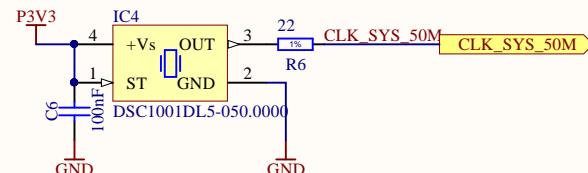
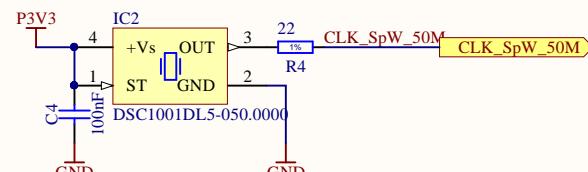
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SpaceVPX P0, SLT3-PAY-1Q2T**

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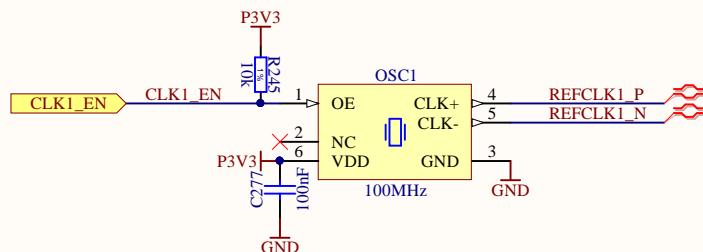
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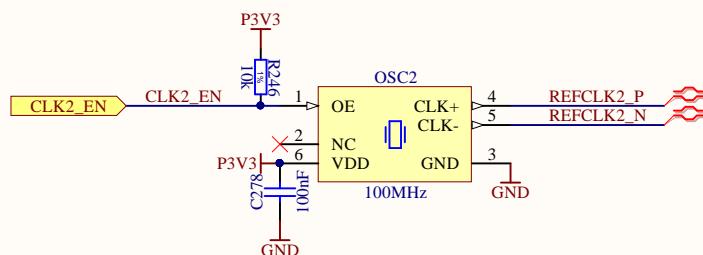
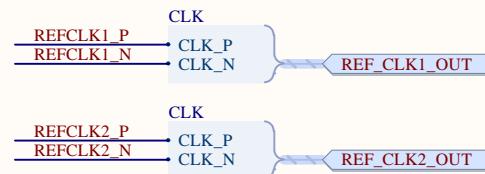
Clock input	Description	Recommended frequency
SYS_CLK	System clock input. A clock based on this clock input via PLL (unless PLL is bypassed) is used to clock the processors, on-chip buses and on-chip peripherals.	50 MHz
MEM_EXTCLK	Alternative memory interface clock. Clock that either directly, or through a PLL, provides an alternative clock for the SDRAM memory interface. See description in table 23, section 3.1.	50 MHz
SPW_CLK	SpaceWire clock. Clock that either directly, or through a PLL (recommended operating mode), provides a clock for the SpaceWire interfaces. See also sections 13.3.1.2 and 13.3.2.	50 MHz
JTAG_TCK	JTAG clock	10 MHz
ETH0_GTXCLK	Ethernet Gigabit MAC 0 clock	125 MHz
ETH0_TXCLK	Ethernet MAC 0 transmit clock	25 MHz
ETH0_RXCLK	Ethernet MAC 0 receive clock	25 MHz (MII) 125 MHz (GMII)
ETH1_GTXCLK	Ethernet Gigabit MAC 1 clock	125 MHz
ETH1_TXCLK	Ethernet MAC 1 transmit clock	25 MHz
ETH1_RXCLK	Ethernet MAC 1 receive clock	25 MHz (MII) 125 MHz (GMII)
PCI_CLK	PCI interface clock	33 MHz
GR1553_CLK	MIL-STD-1553B interface clock	20 MHz

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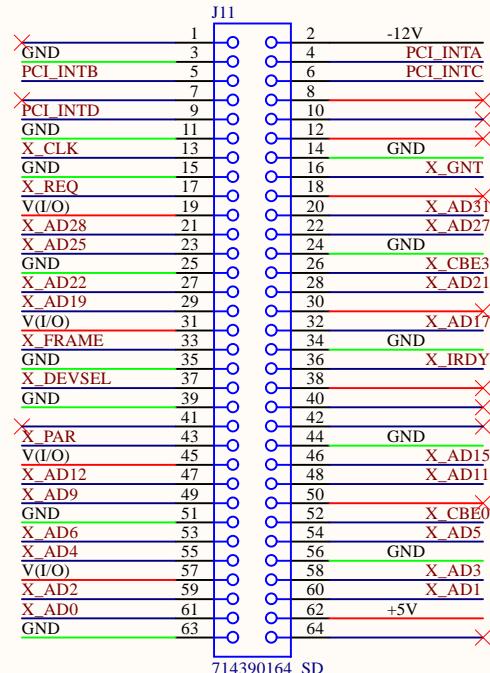
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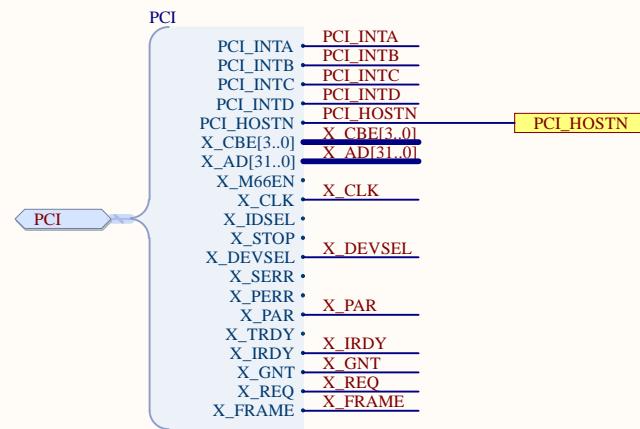
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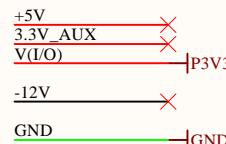
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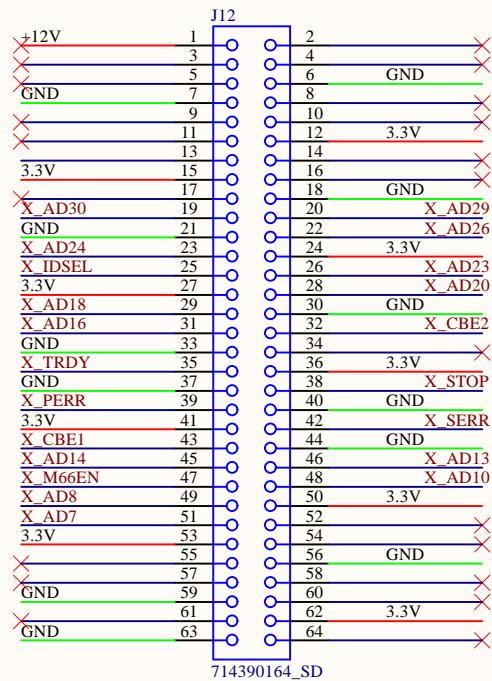
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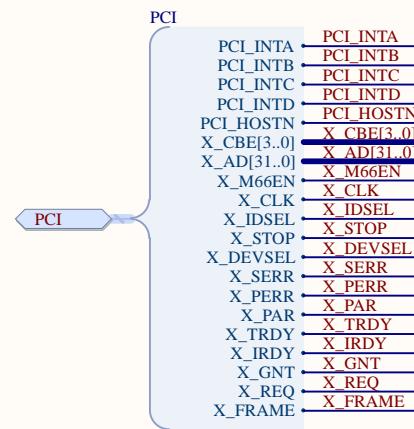
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C

3.3V — P3V3
GND — GND

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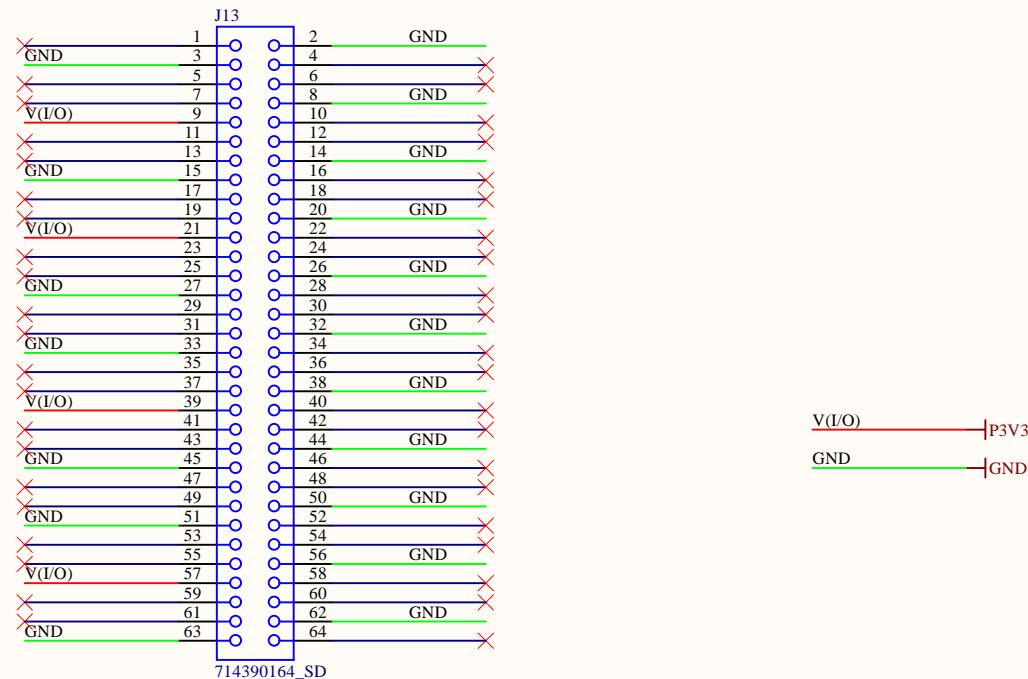
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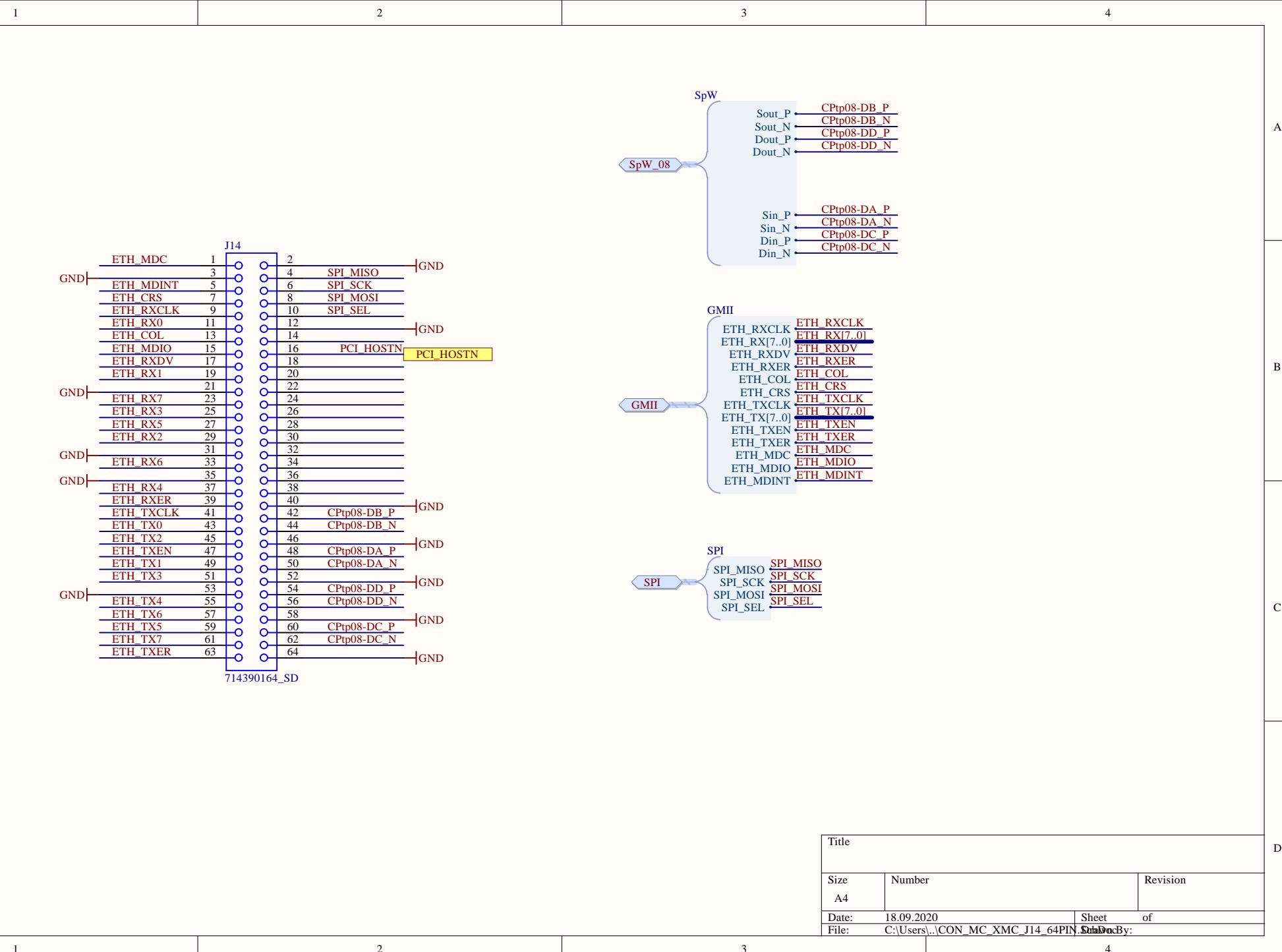
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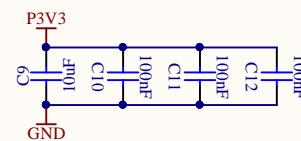
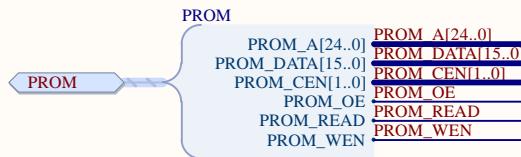
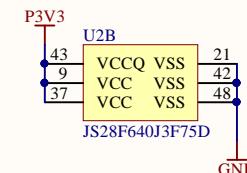
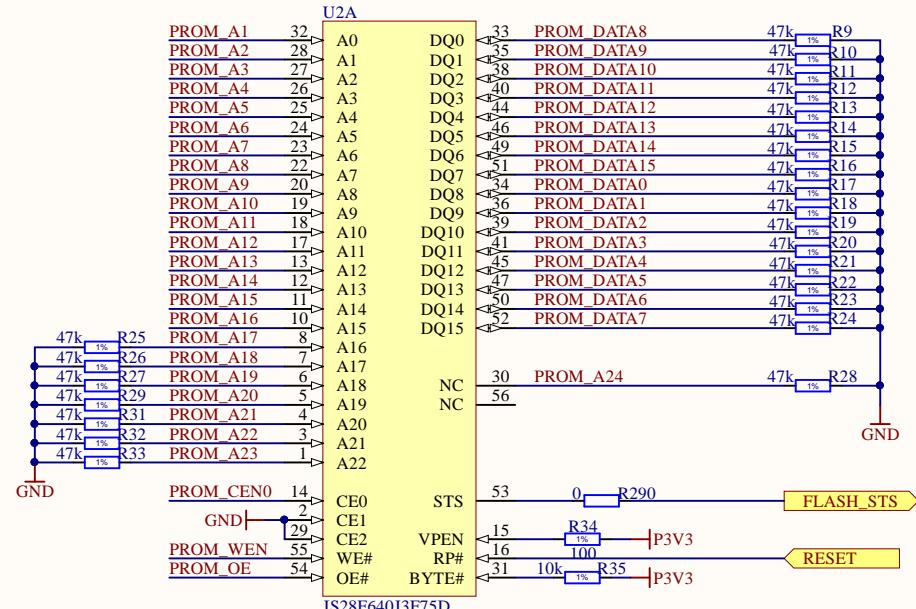
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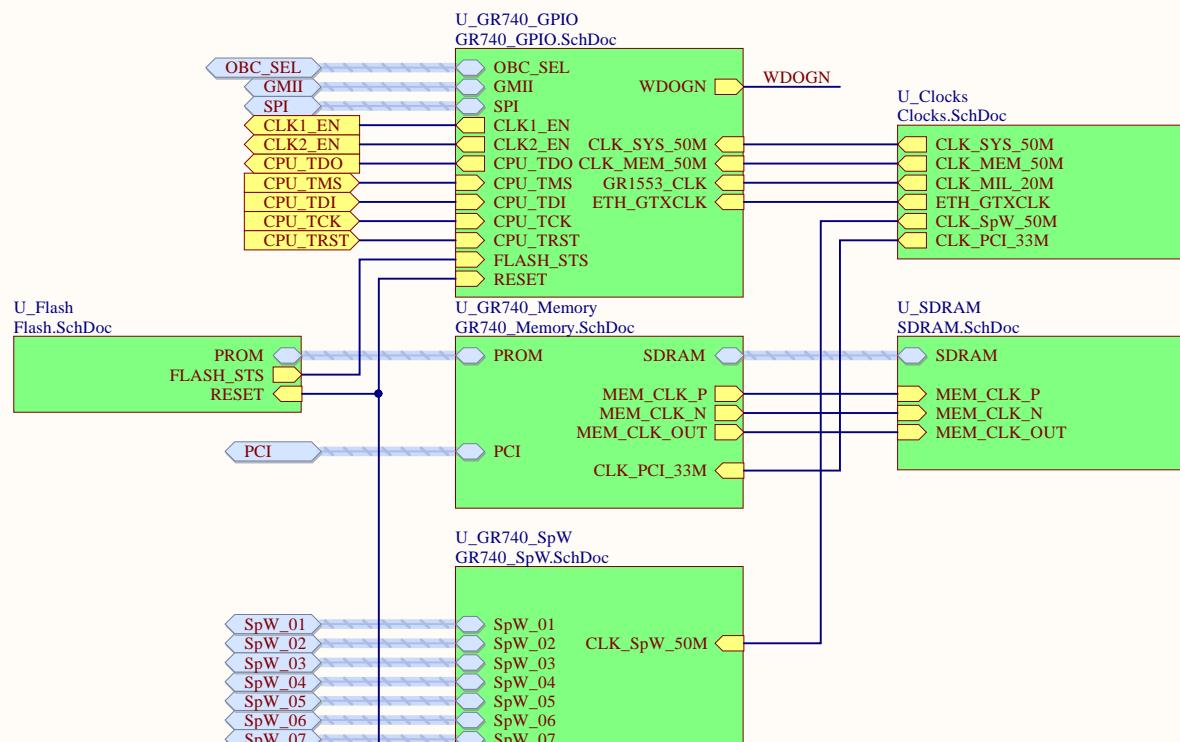
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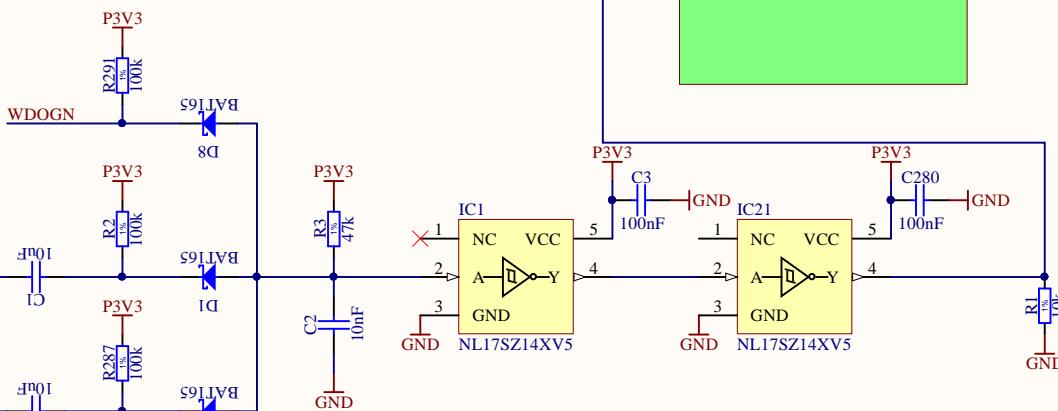
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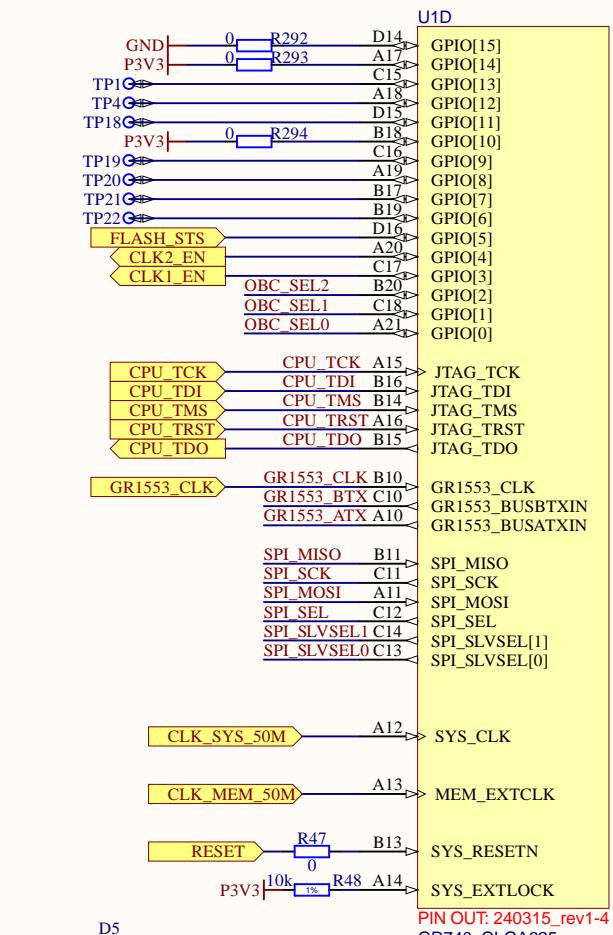
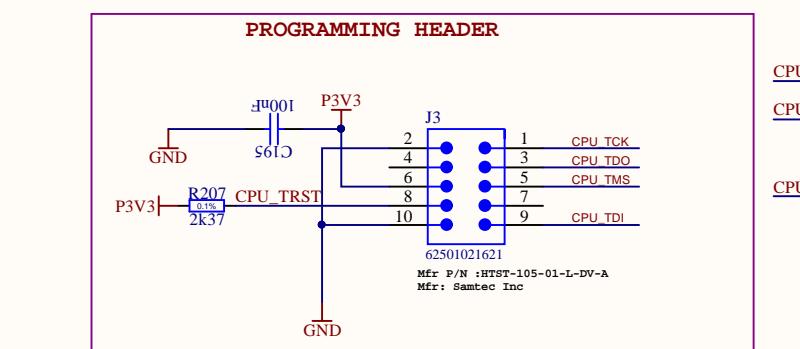
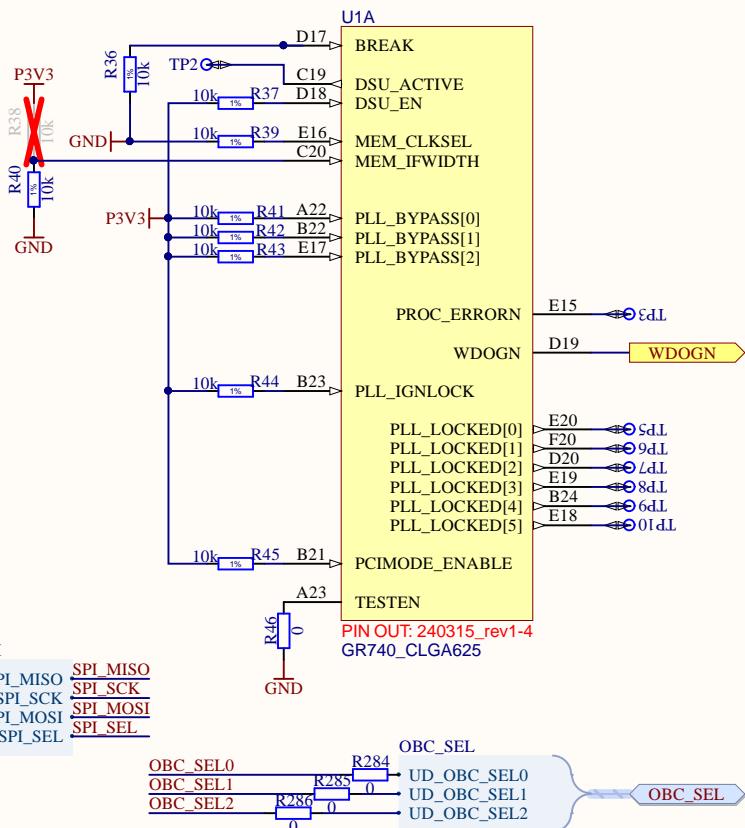
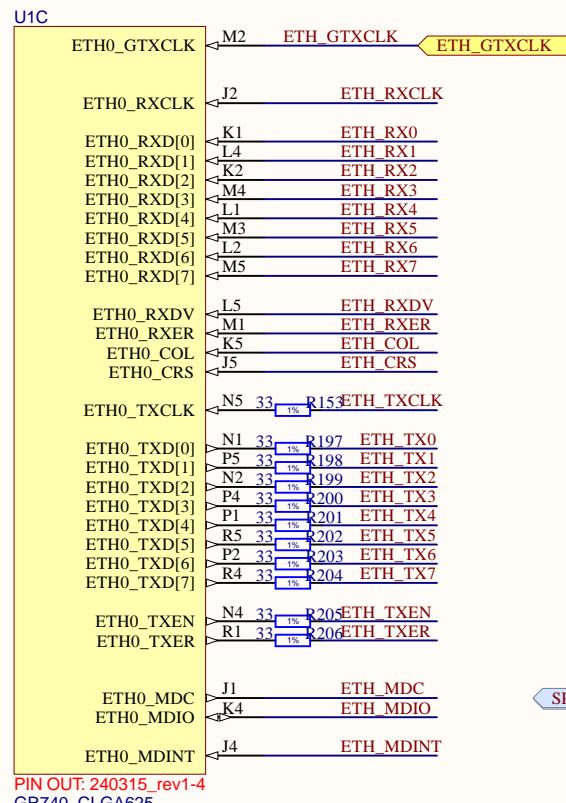
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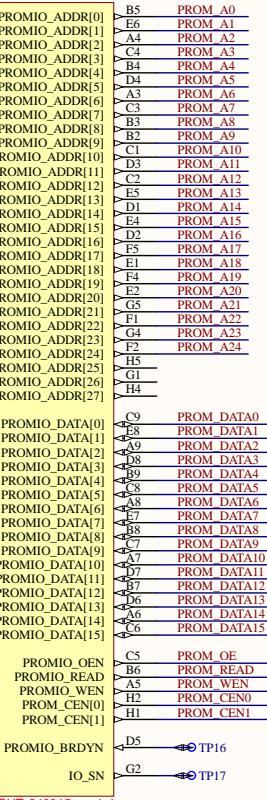
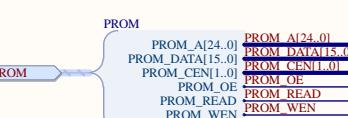
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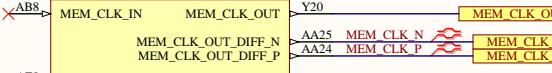
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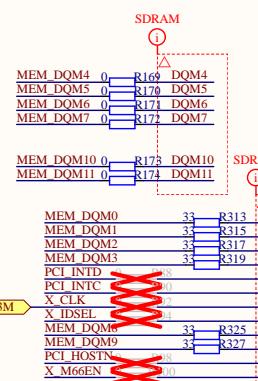
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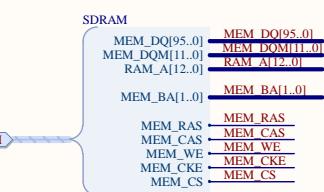
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RAM_A3 AB10
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AA25 MEM CLK_N
AA24 MEM CLK_P

SDRAM



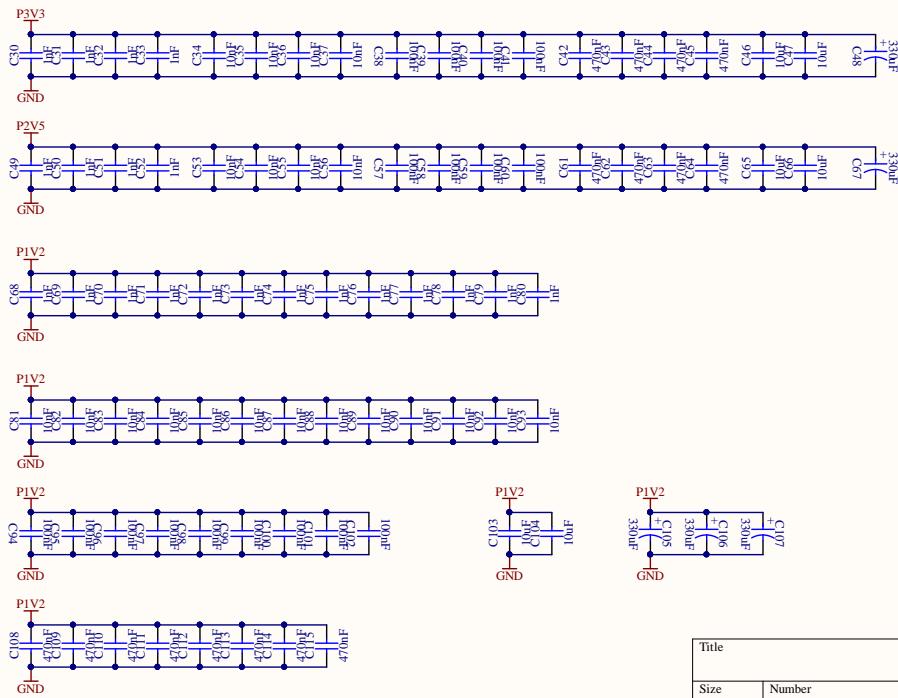
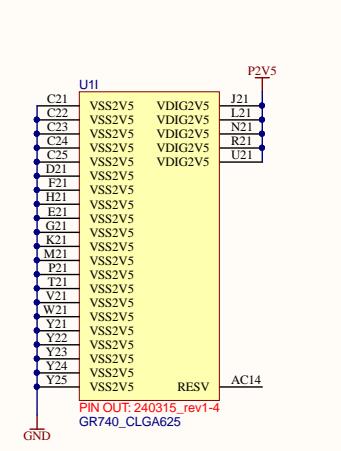
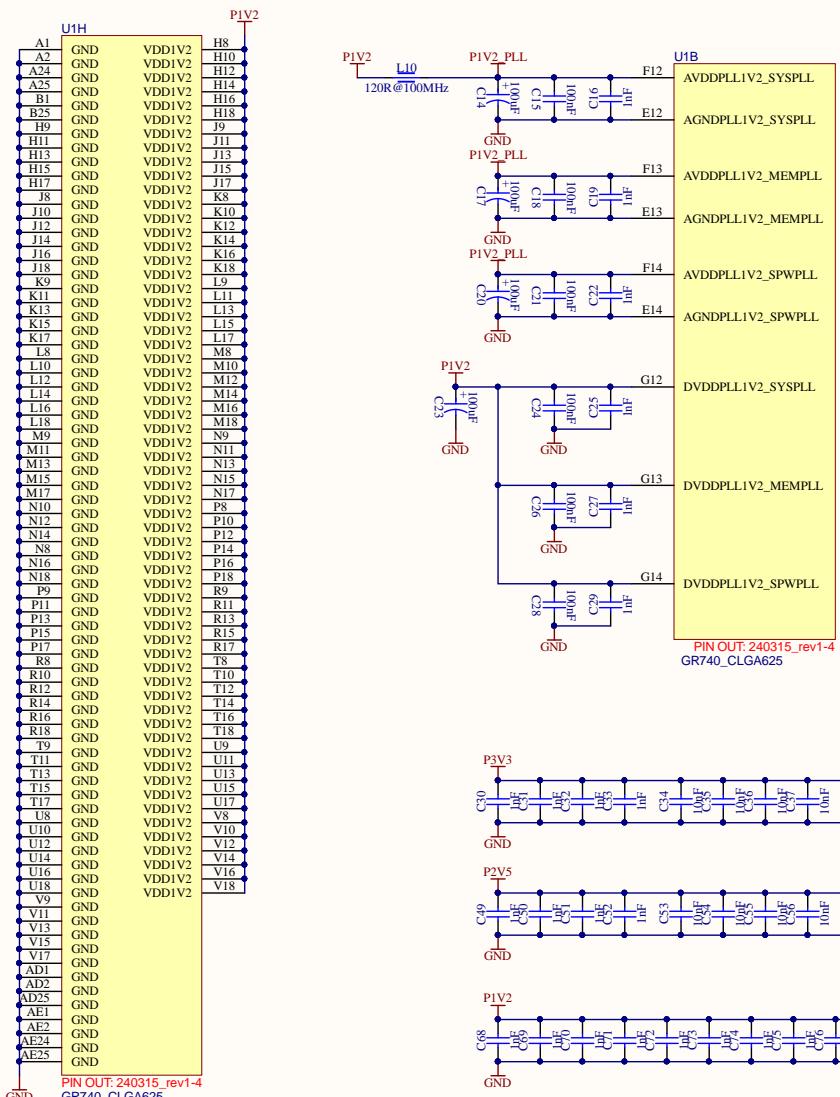
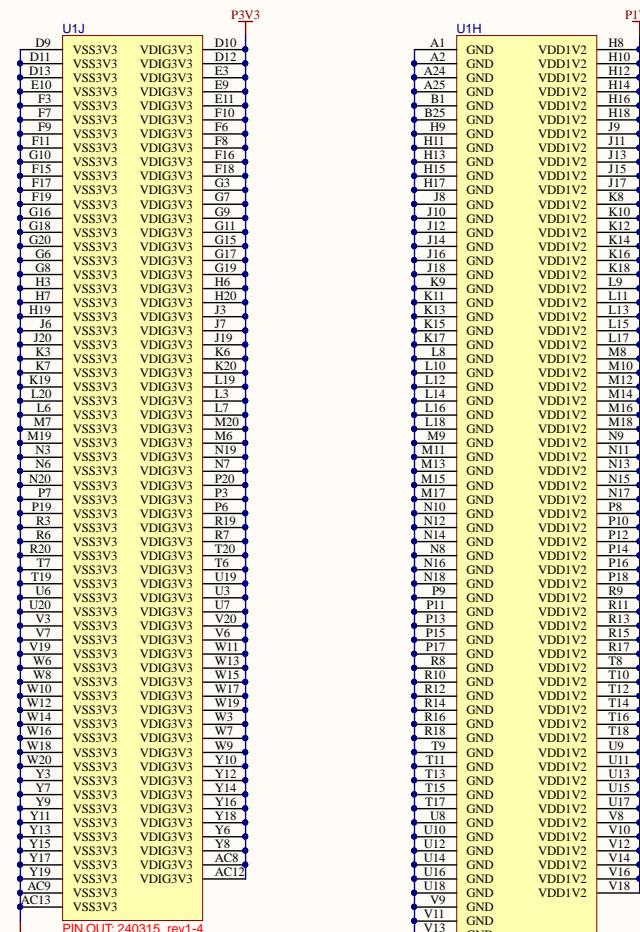
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- X_SERR
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- X_GNT
- X_REQ
- X_FRAME
- X_CBE0
- X_CBE1
- X_CBE2
- X_CBE3
- X_ADI
- X_ADI2
- X_M66
- X_CLK
- X_IDSEL
- X_STOP
- X_DEVSEL
- X_SERR
- X_PERR
- X_PAR
- X_TDY
- X_IRDY
- X_GNT
- X_REQ
- X_FRAME
- X_CBE4
- X_CBE5
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- X_CBE7
- X_CBE8
- X_CBE9
- X_CBE10
- X_CBE11
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- X_CBE63



PIN OUT: 240315_rev1-4
GR740_CLGA625

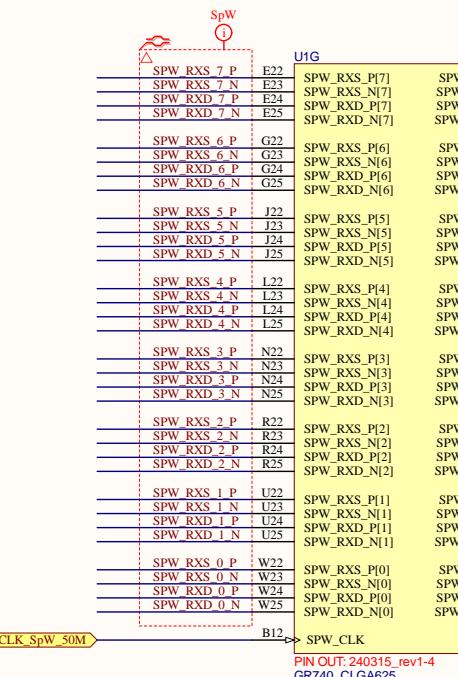
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MEM_DQ903 R163 DQ90
MEM_DQ913 R164 DQ91
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MEM_DQ933 R166 DQ93
MEM_DQ943 R167 DQ94
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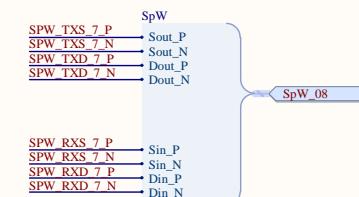
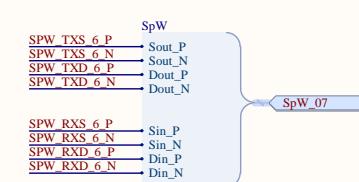
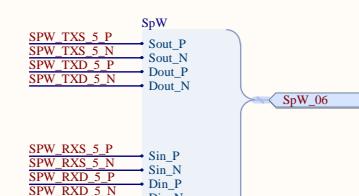
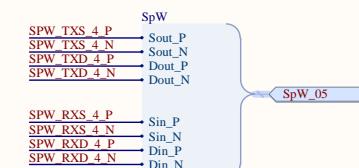
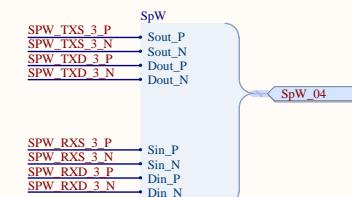
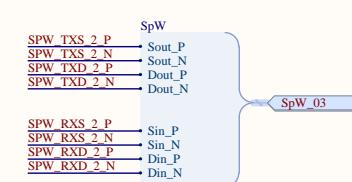
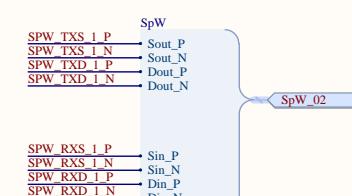
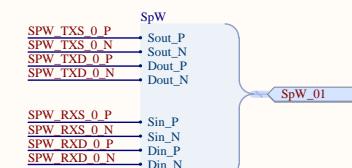
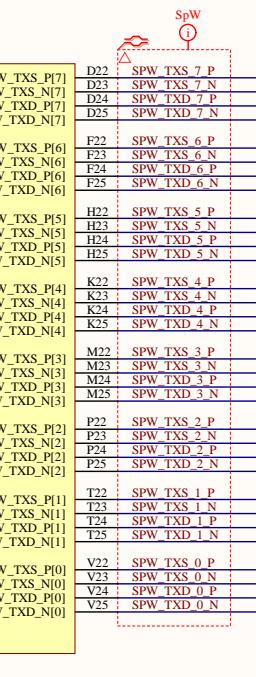


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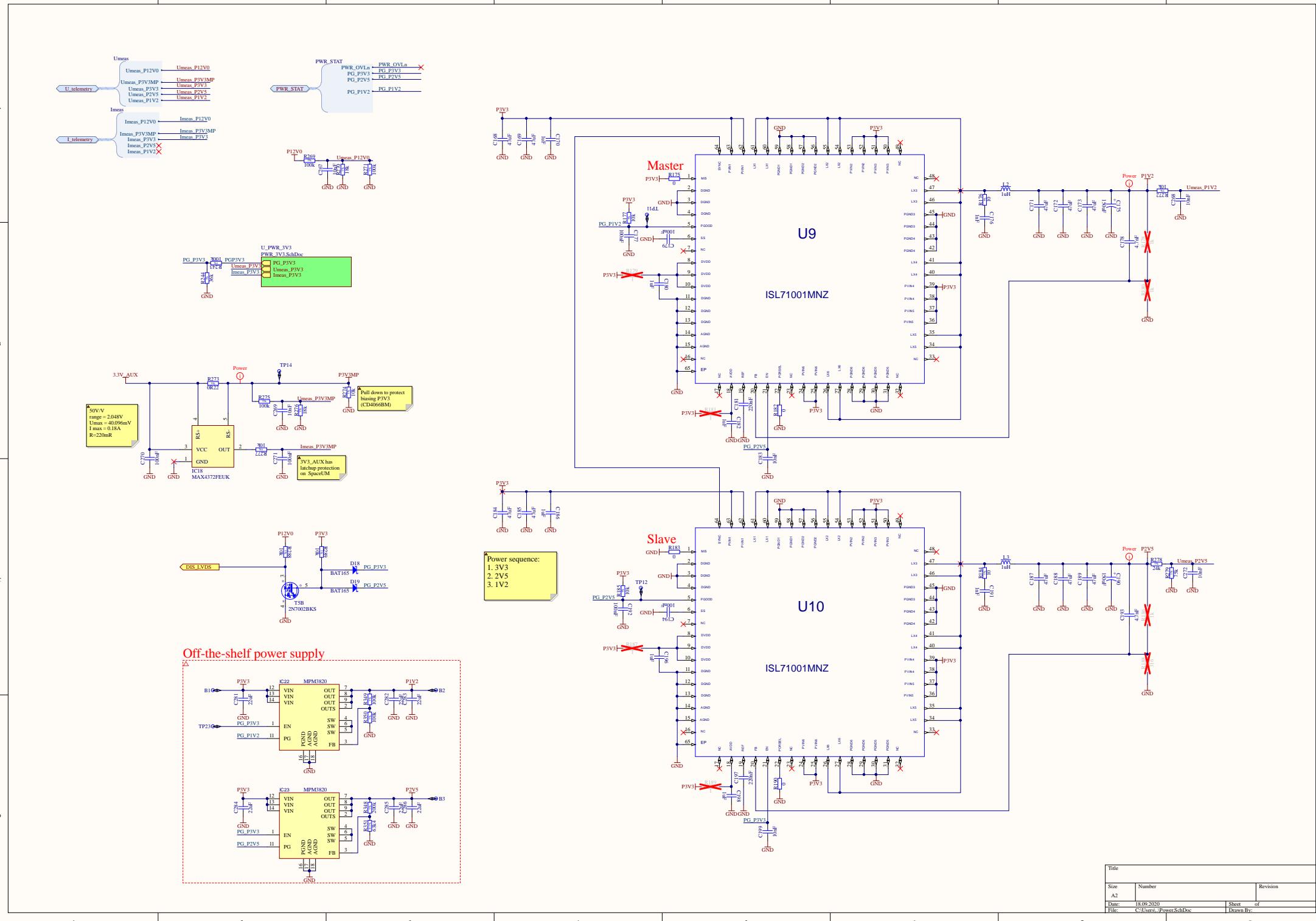
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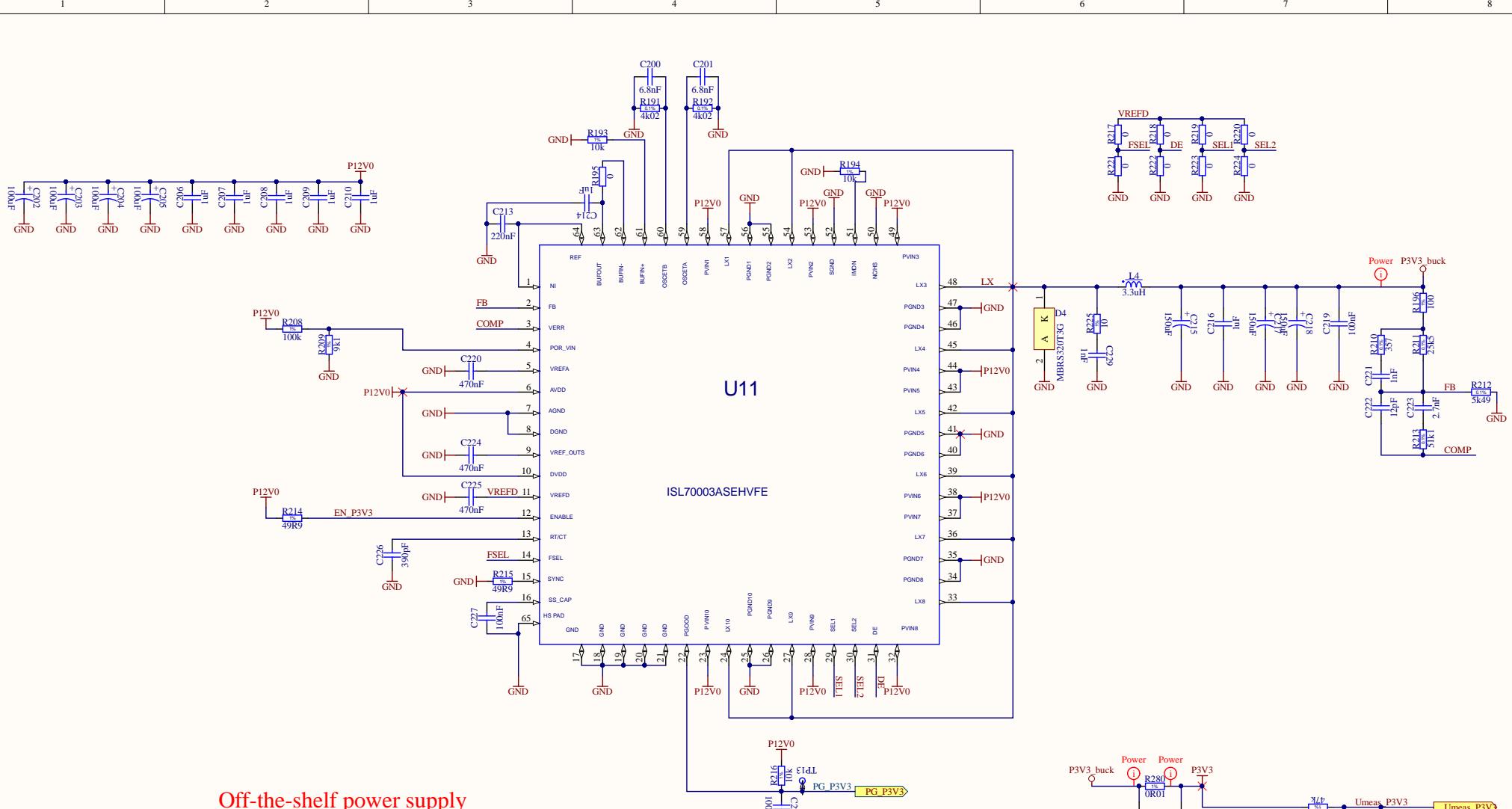
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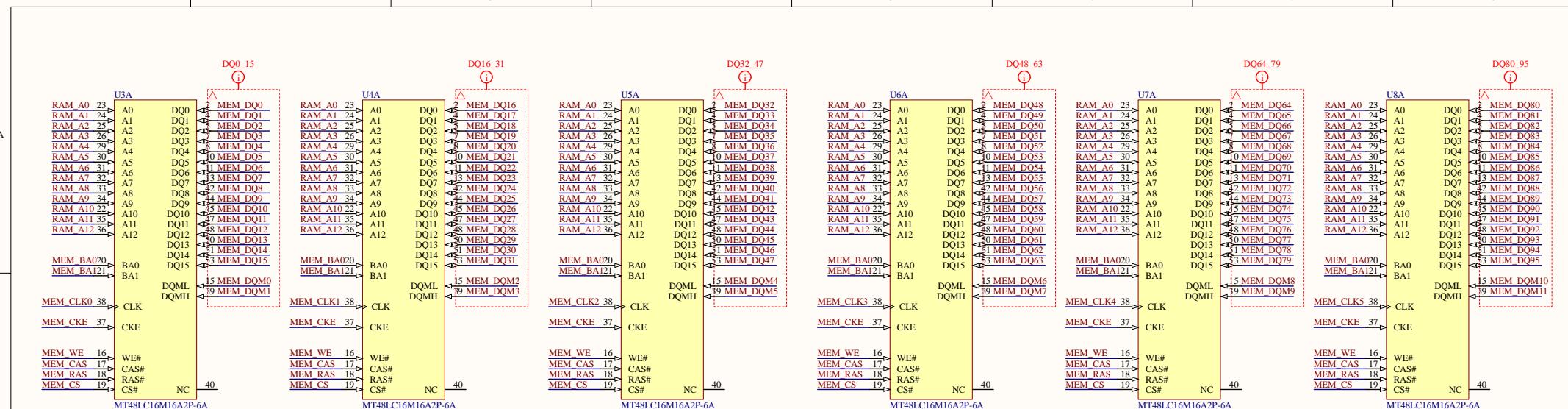
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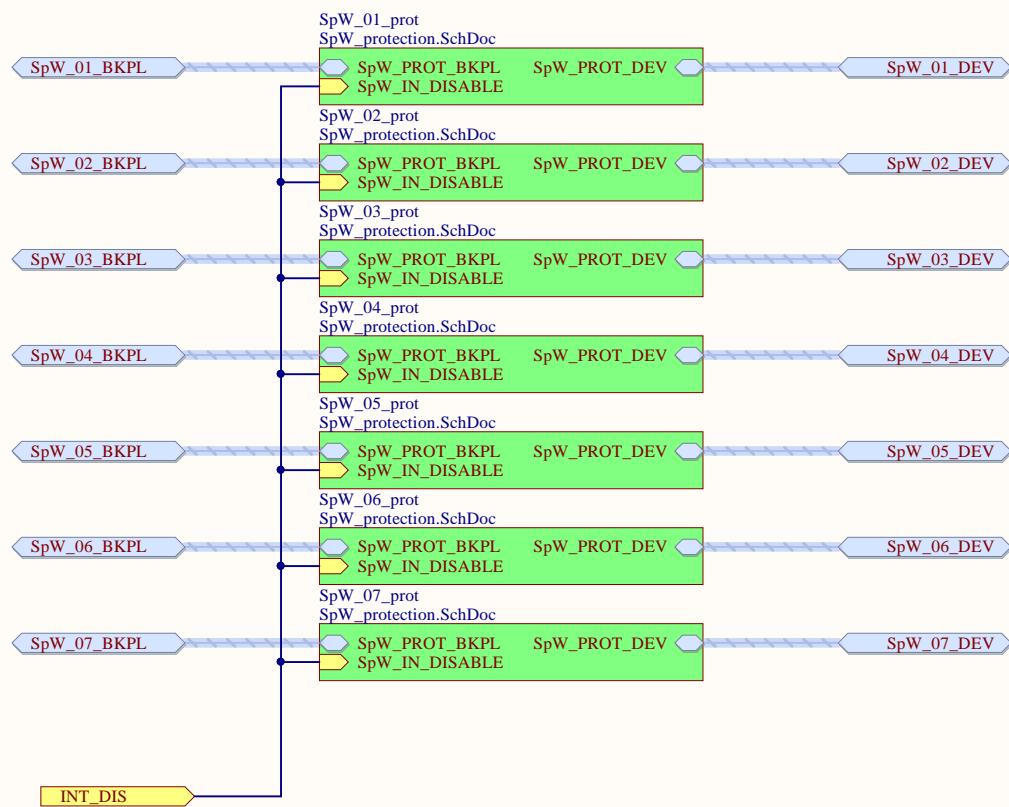
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A

A



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C

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▲ Short incoming LVDS lines to GND in case of latch-up to prevent any input current.

Title *SpaceVPX interface protection*

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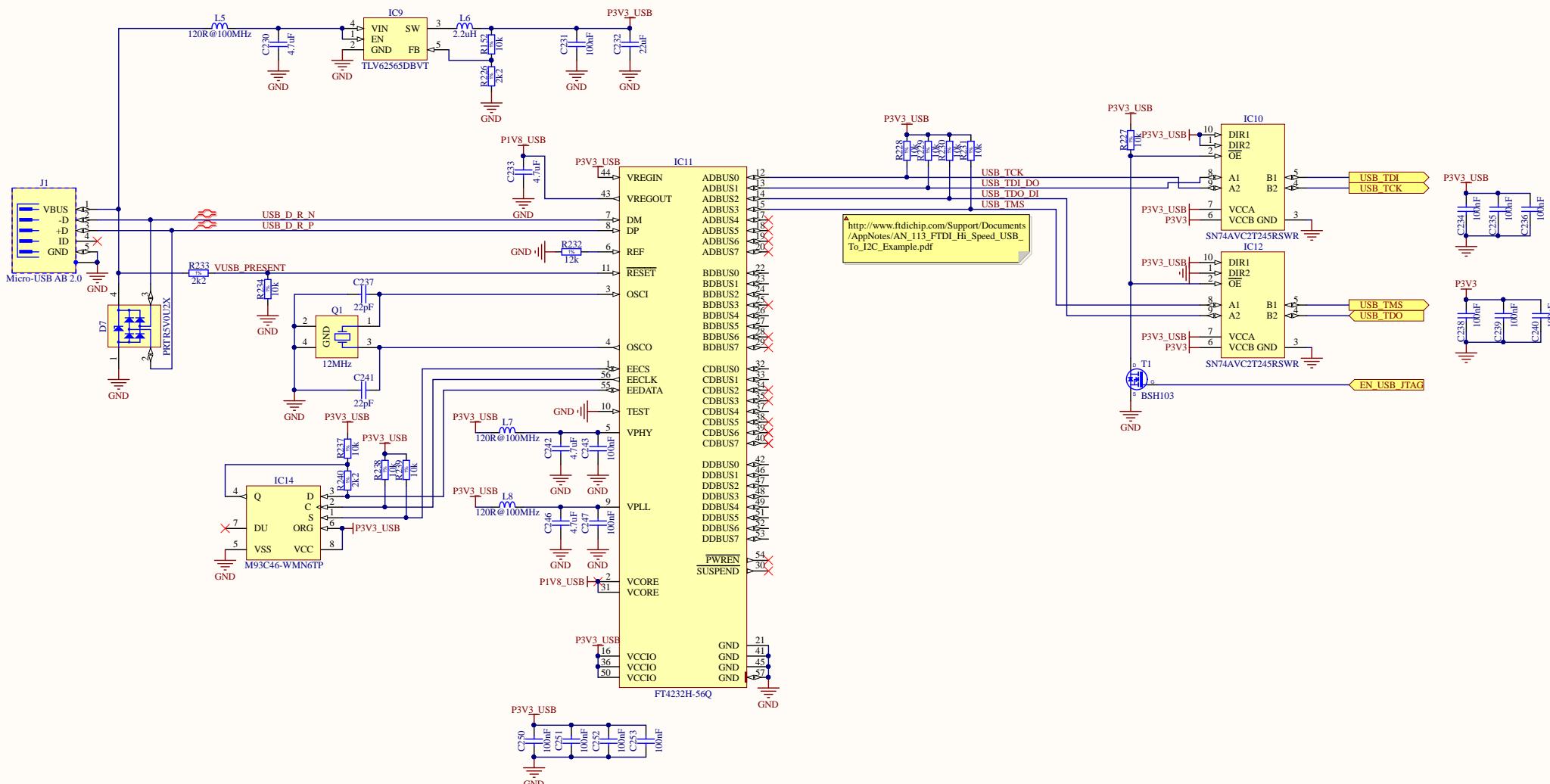
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Gen. L. Okulickiego 7/9
05-500 Piaseczno
Poland

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NESANS01\Workbench\Altium\HyperSat_Templates\CT

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