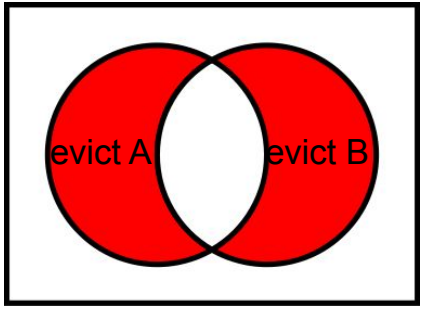
MP4 Final presentation

By Derek, Michal, and Max

Unique Design Considerations



Complimentary features:

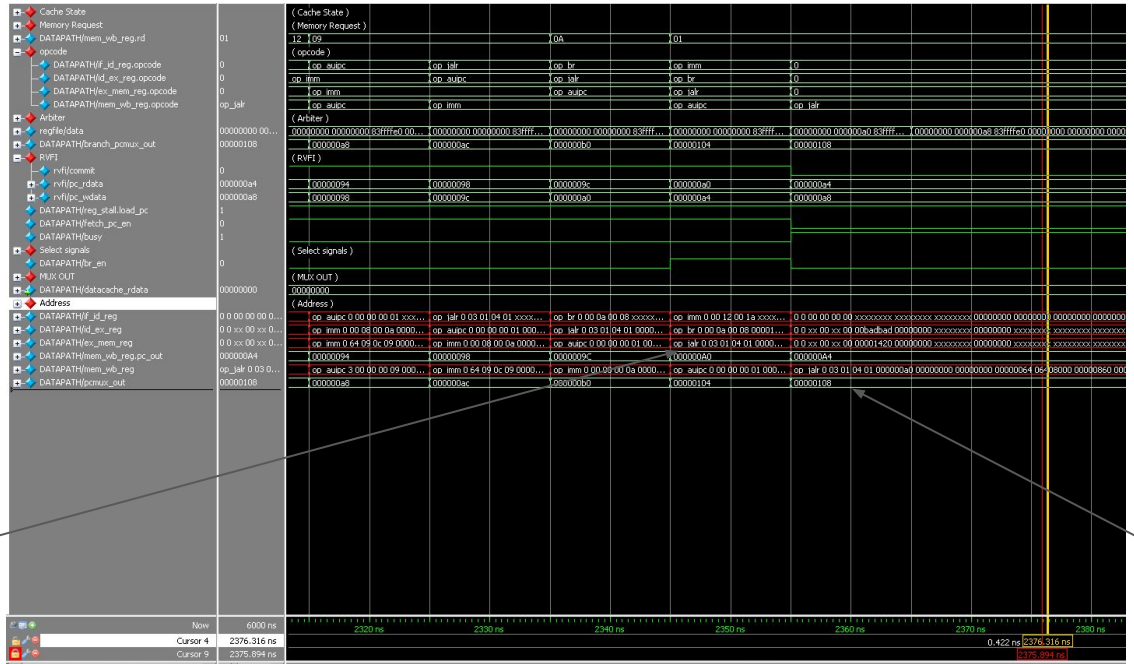
- pLRU
  - probability is your friend
- Eviction Write buffer
  - trapeze net for caches.
- L2 cache
  - carpool lane
- Pipeline L1 caches
  - no need to wait for everyone's food to be ready if your food is.
- Tournament branch predictor
  - more robust branch prediction
- Return address stack
  - exploit predictability
  - extra care?

Temporary storage between L2 and main memory.
MAT(L1) < MAT(L2) << MAT(Memory)

Quantitative results

	Time (ns)	Power (mW)	Score
Comp1	655645	512.14	3.787e-11
Comp2	4299205	485.32	9.0834e-9
Comp3	3616065	471.10	4.94365e-9

Geometric Mean: 1.193502e-

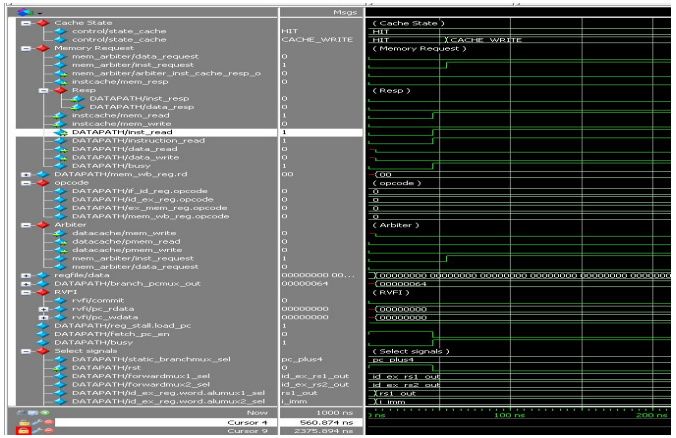


before

after

If we had a time machine to 3/18/21

- **Bugs, lots and lots of bugs(took more time than should have):**
  - **Stores after loads hazard**
  - **Arbiter(Easiest = Deception, Complex = error-prone)**
  - **Control ROM**
  - **RISC-V Manual is King(Instruction specific bugs)**
- **What We learned**
  - **Occam's Razor:** simpler = better = easier debug
    - CPU designs are complicated. Keep it simple.
  - **Communication is important**
    - Everyone has to be on the same page.
    - Explaining Skills: who does what best
  - **Debugging Skills**
    - Waveforms are tricky and time consuming(Debugging checkpoint code is pain :()
    - Tunnel vision
    - "Give me six hours to chop down a tree and I will spend the first four sharpening the axe."
  - **Read the Docs carefully!(Even if it is painful and boring)**
    - RISC-V Manual
    - MP4 Docs
    - http://chipverify.com/systemverilog/systemverilog-tutorial
  - **Avoid Assumptions**
    - Didn't thoroughly examine intermediate/final register contents, assumed 600d600d = GOOD!
    - Beware undefined/inferred behavior
      - Programming for hardware != Programming for software



(10s to add waves of interest)*(1000 runs) = 2.8 hrs clicking labels

Any Questions?