FPGA- PART 1 FINAL REPORT

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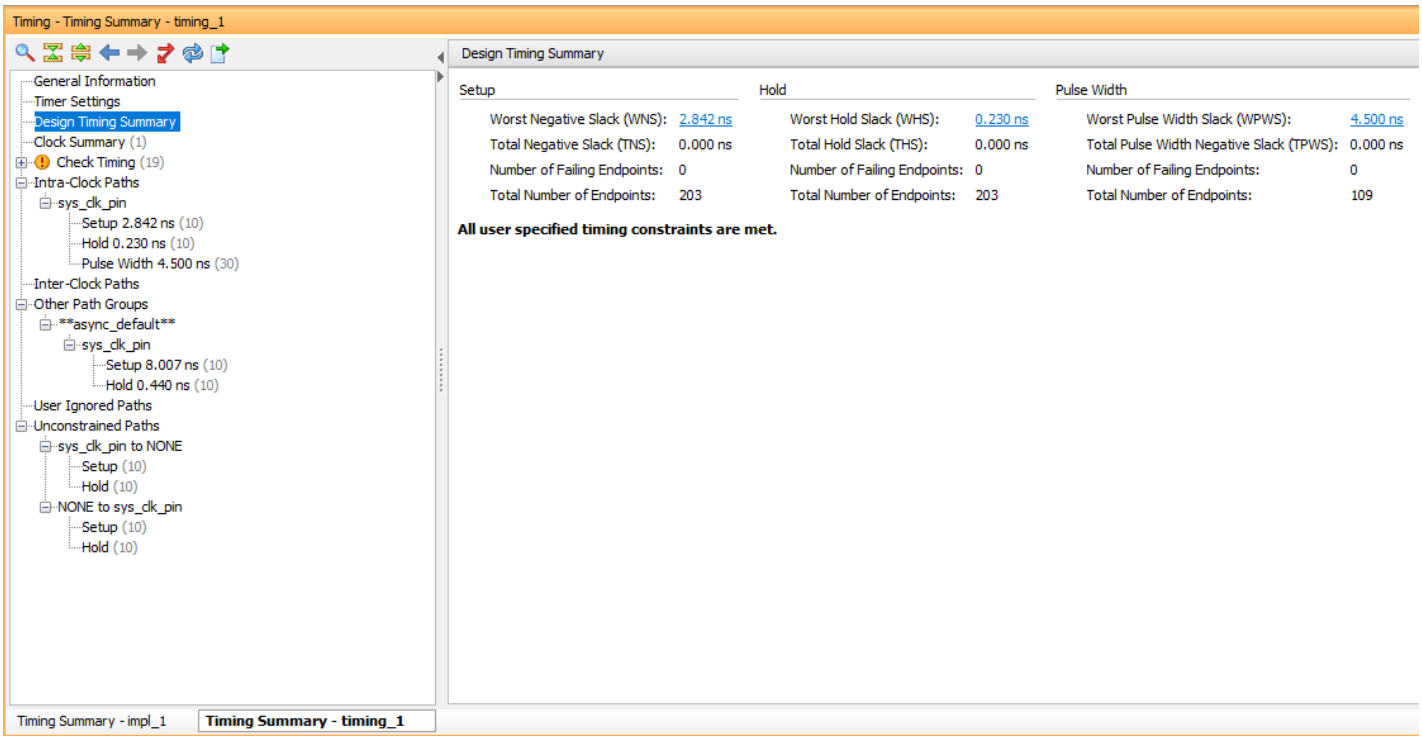
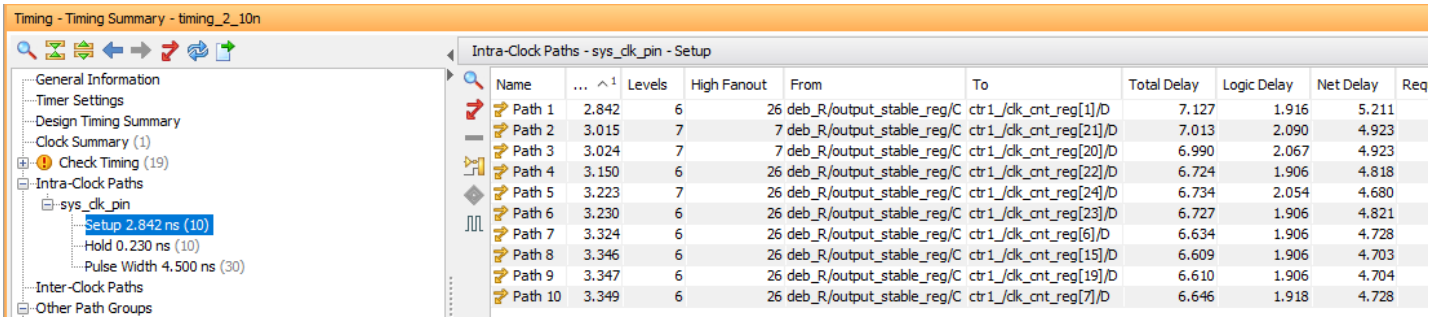
Q13

13.c.i.



13.c.ii.

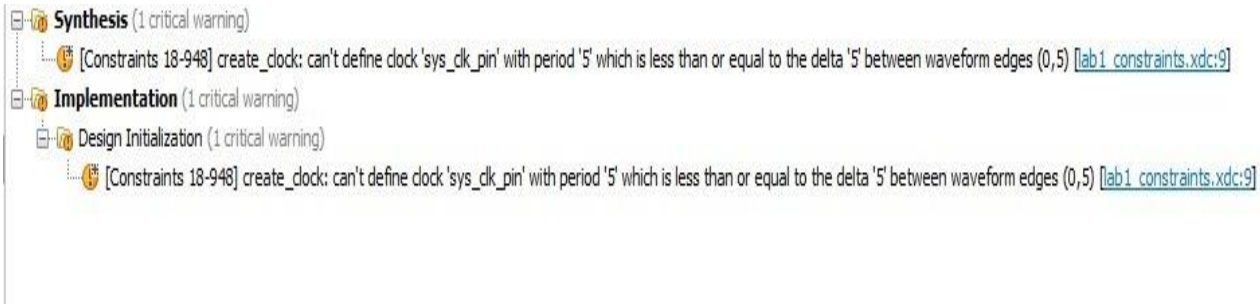


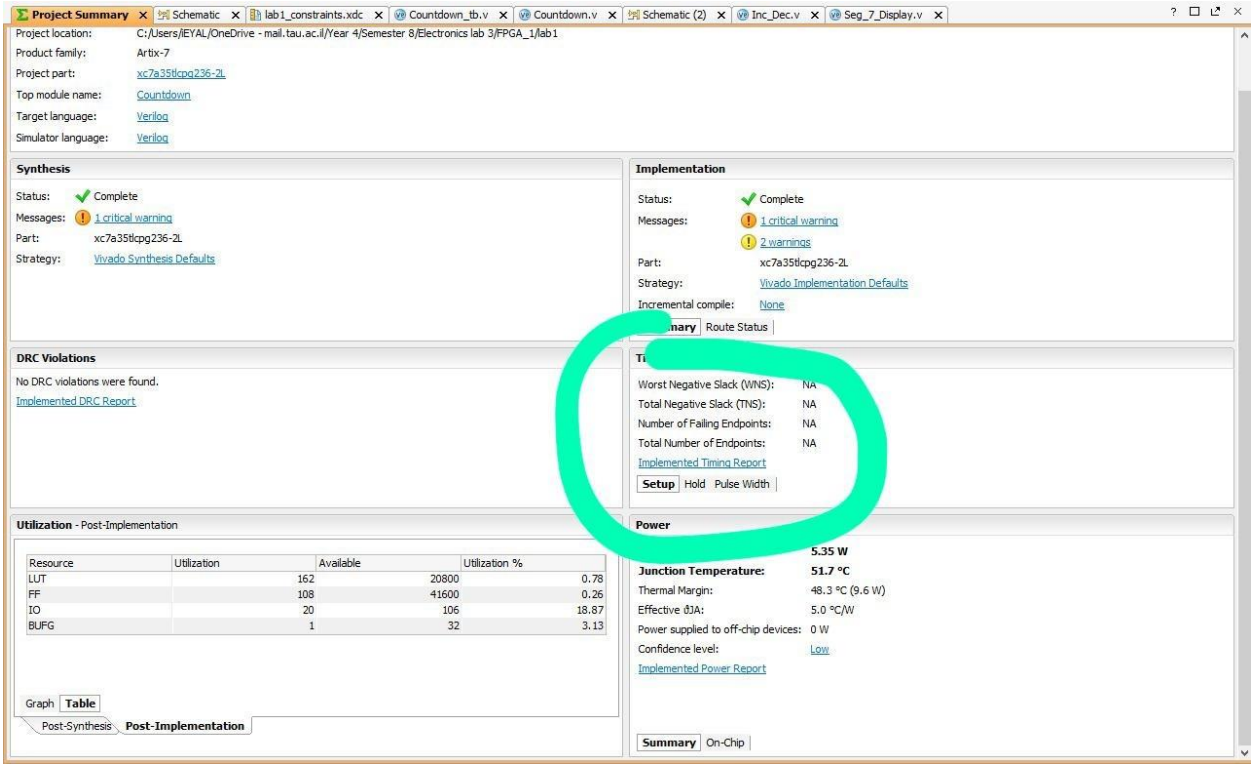
critical setup length = T - min(slacks) = 10ns - 2.842ns = 7.158ns

13.c.iii.

If we change the timing constraint to 5nsec instead of 10nsec, the setup procedure of the ‘sys_clk_pin’ (which requires 8.007ns) will not be able to complete. setup must be shorter than the time_period. If it isn’t, the signal won't be ready in time for the next cycle. Thus, using a too short cycle results in ‘sys_clk_pin’ not being defined properly .

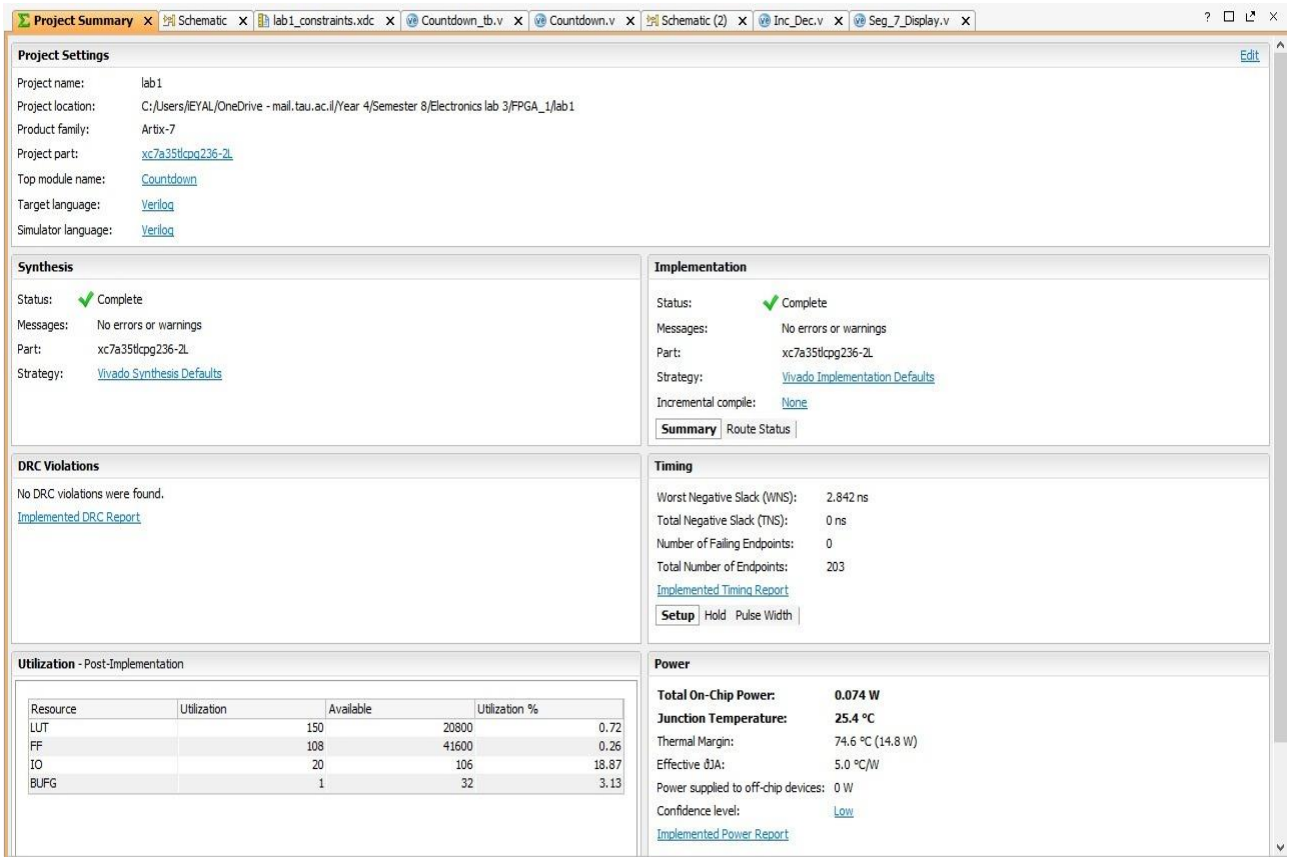
For further exploration, we tried running ‘implementation’ under 5nsec time constraints. As a result, the following critical warning appeared, and the timing in the project summary clearly indicates that something went wrong.





Q14

14.d.i.



14.d.ii.

During our first synthesis attempt, we had a critical warning because we assigned values to the same register from two different always blocks (in the counter module)

We easily fixed that after realizing one assignment was not necessary and removing it.

Another type of warning we encountered was of the form “the signal ___ should be on the sensitivity list”.

Those warnings were fixed by adding the mentioned signals to the argument of the always block they appeared in.

The instructor said that our implementation worked well and told us to proceed ☺