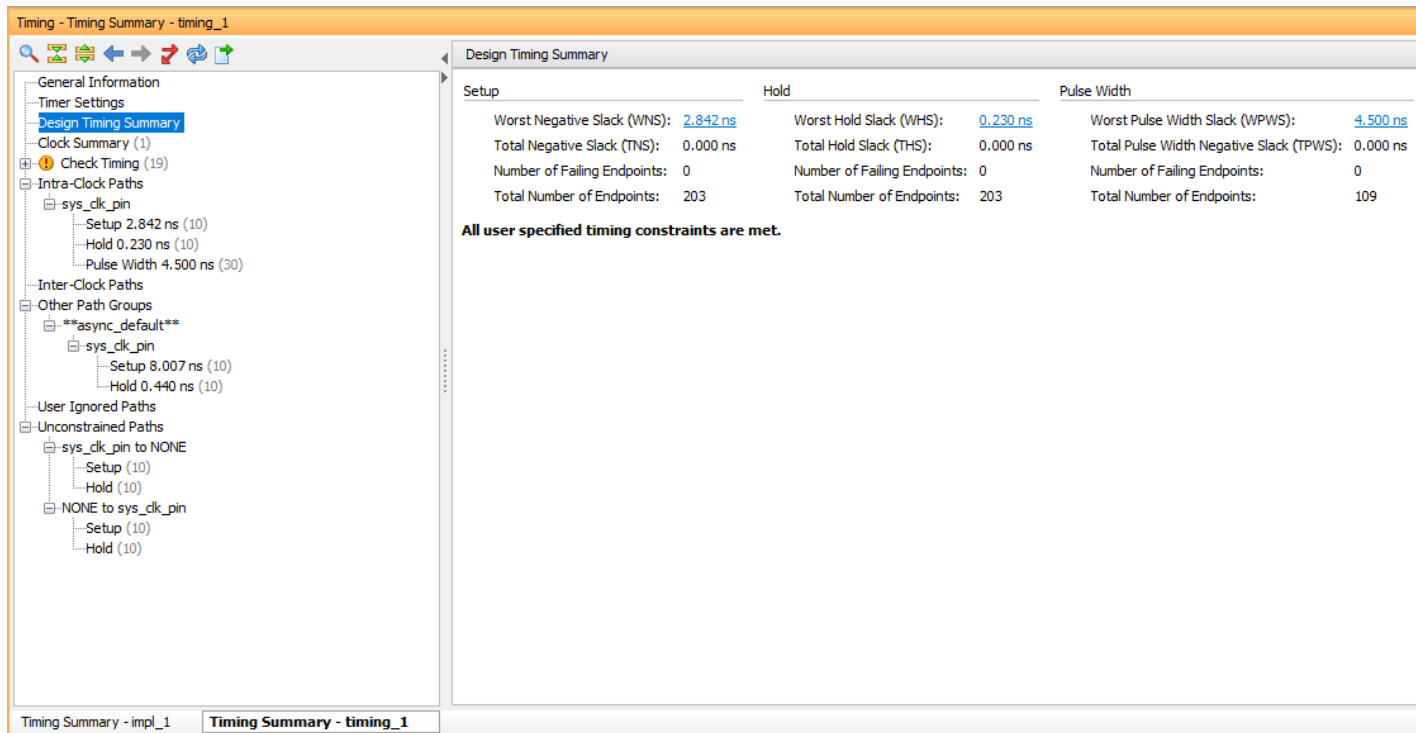


# FPGA- PART 1 FINAL REPORT

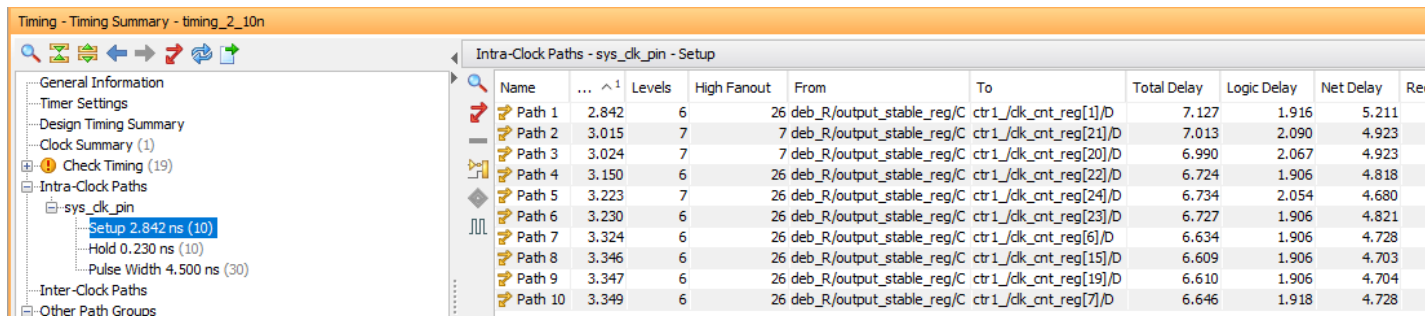
Michal Keren (204783161) & Itamar Eyal (302309539)

Q13

13.c.i.



13.c.ii.



critical setup length =  $T - \min(\text{slacks}) = 10\text{ns} - 2.842\text{ns} = 7.158\text{ns}$

13.c.iii.

If we change the timing constraint to 5nsec instead of 10nsec, the setup procedure of the 'sys\_clk\_pin' (which requires 8.007ns ) will not be able to complete. setup must be shorter than the time\_period. If it isn't, the signal won't be ready in time for the next cycle. Thus, using a too short cycle results in 'sys\_clk\_pin' not being defined properly .

For further exploration, we tried running 'implementation' under 5nsec time constraints. As a result, the following critical warning appeared, and the timing in the project summary clearly indicates that something went wrong.

The image shows the Vivado IDE interface. At the top, a project tree lists 'Synthesis (1 critical warning)', 'Implementation (1 critical warning)', and 'Design Initialization (1 critical warning)'. Each item has a warning icon and a message: '[Constraints 18-948] create\_clock: can't define clock 'sys\_clk\_pin' with period '5' which is less than or equal to the delta '5' between waveform edges (0,5) [lab1\_constraints.xdc:9]'. Below this is the 'Project Summary' window. It shows project details like location, family (Artix-7), part (xc7a35t1cpq236-2L), and target language (Verilog). The 'Synthesis' section shows 'Status: Complete' and 'Messages: 1 critical warning'. The 'Implementation' section shows 'Status: Complete' and 'Messages: 1 critical warning, 2 warnings'. A red circle highlights the 'Timing' section in the Implementation tab, which shows 'Worst Negative Slack (WNS): NA', 'Total Negative Slack (TNS): NA', 'Number of Failing Endpoints: NA', and 'Total Number of Endpoints: NA'. Below this is the 'Power' section showing 'Junction Temperature: 51.7 °C'. At the bottom, there is a table for 'Utilization - Post-Implementation'.

Resource	Utilization	Available	Utilization %
LUT	162	20800	0.78
FF	108	41600	0.26
IO	20	106	18.87
BUFG	1	32	3.13

## Q14

### 14.d.i.

The screenshot shows the Vivado IDE Project Summary window for a project named 'lab1'. The window is divided into several sections:

- Project Settings:** Project name: lab1, Project location: C:/Users/IEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA\_1/lab1, Product family: Artix-7, Project part: xc7a35t1cpq236-2L, Top module name: Countdown, Target language: Verilog, Simulator language: Verilog.
- Synthesis:** Status: Complete, Messages: No errors or warnings, Part: xc7a35t1cpq236-2L, Strategy: Vivado Synthesis Defaults.
- Implementation:** Status: Complete, Messages: No errors or warnings, Part: xc7a35t1cpq236-2L, Strategy: Vivado Implementation Defaults, Incremental compile: None. Buttons: Summary, Route Status.
- DRC Violations:** No DRC violations were found. Button: Implemented DRC Report.
- Timing:** Worst Negative Slack (WNS): 2.842 ns, Total Negative Slack (TNS): 0 ns, Number of Failing Endpoints: 0, Total Number of Endpoints: 203. Button: Implemented Timing Report. Buttons: Setup, Hold, Pulse Width.
- Utilization - Post-Implementation:** A table showing resource utilization.
- Power:** Total On-Chip Power: 0.074 W, Junction Temperature: 25.4 °C, Thermal Margin: 74.6 °C (14.8 W), Effective  $\theta_{JA}$ : 5.0 °C/W, Power supplied to off-chip devices: 0 W, Confidence level: Low. Button: Implemented Power Report.

Resource	Utilization	Available	Utilization %
LUT	150	20800	0.72
FF	108	41600	0.26
IO	20	106	18.87
BUFG	1	32	3.13

### 14.d.ii.

During our first synthesis attempt, we had a critical warning because we assigned values to the same register from two different always blocks (in the counter module)

We easily fixed that after realizing one assignment was not necessary and removing it.

Another type of warning we encountered was of the form “the signal \_\_\_\_ should be on the sensitivity list”.

Those warnings were fixed by adding the mentioned signals to the argument of the always block they appeared in.

The instructor said that our implementation worked well and told us to proceed 😊