FPGA- PART 1 PRELIMINARY REPORT

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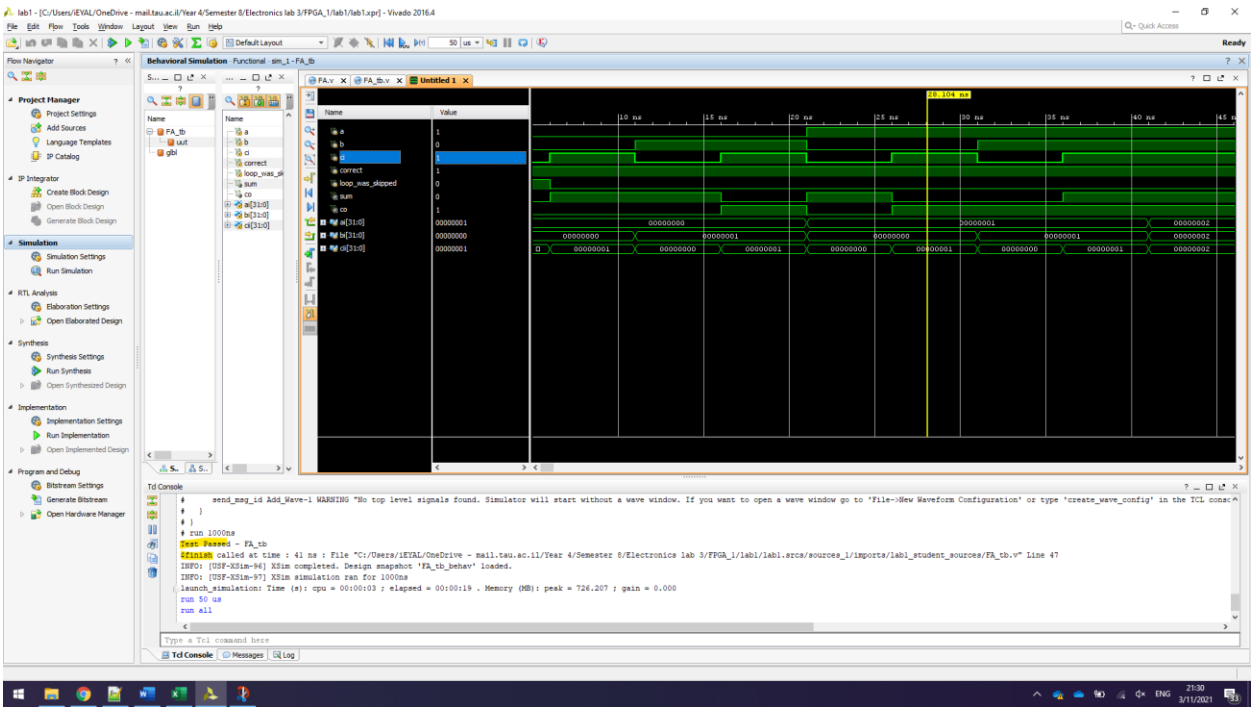
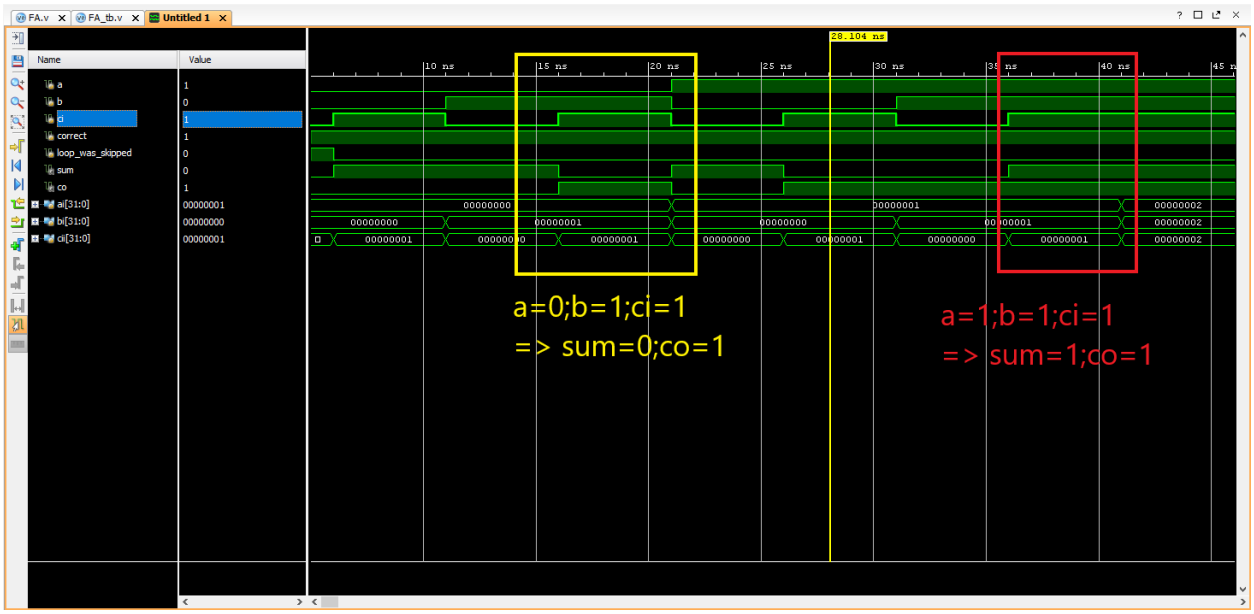
Q2

2.d.

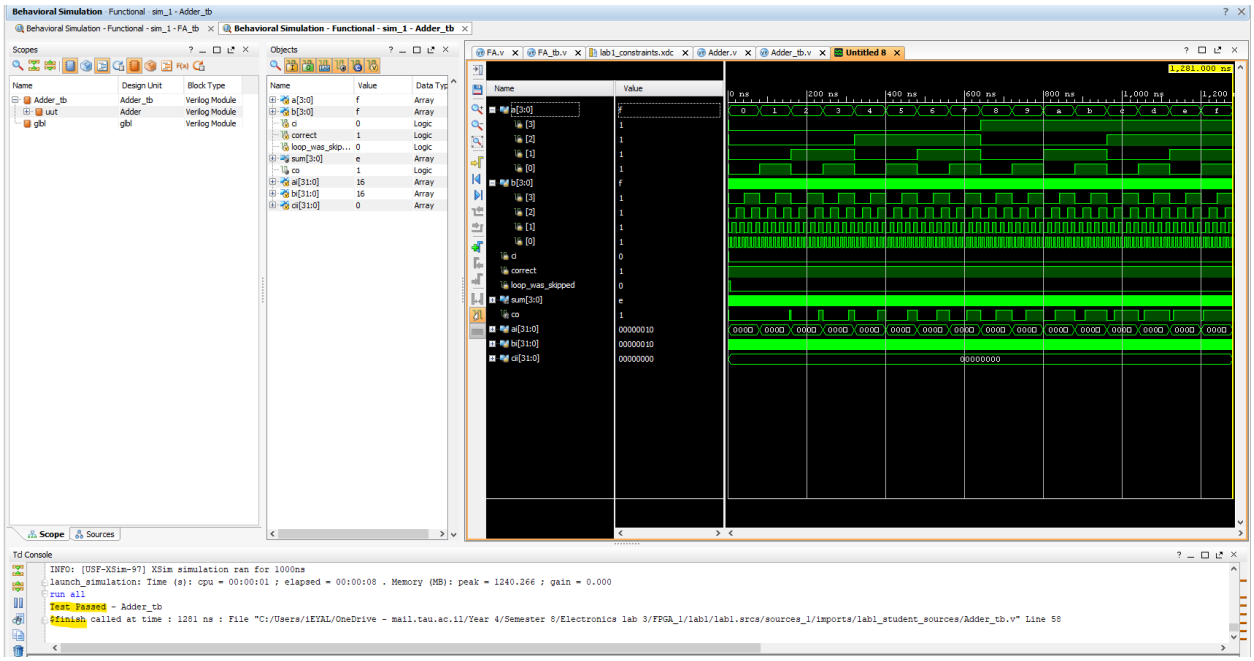




Q3

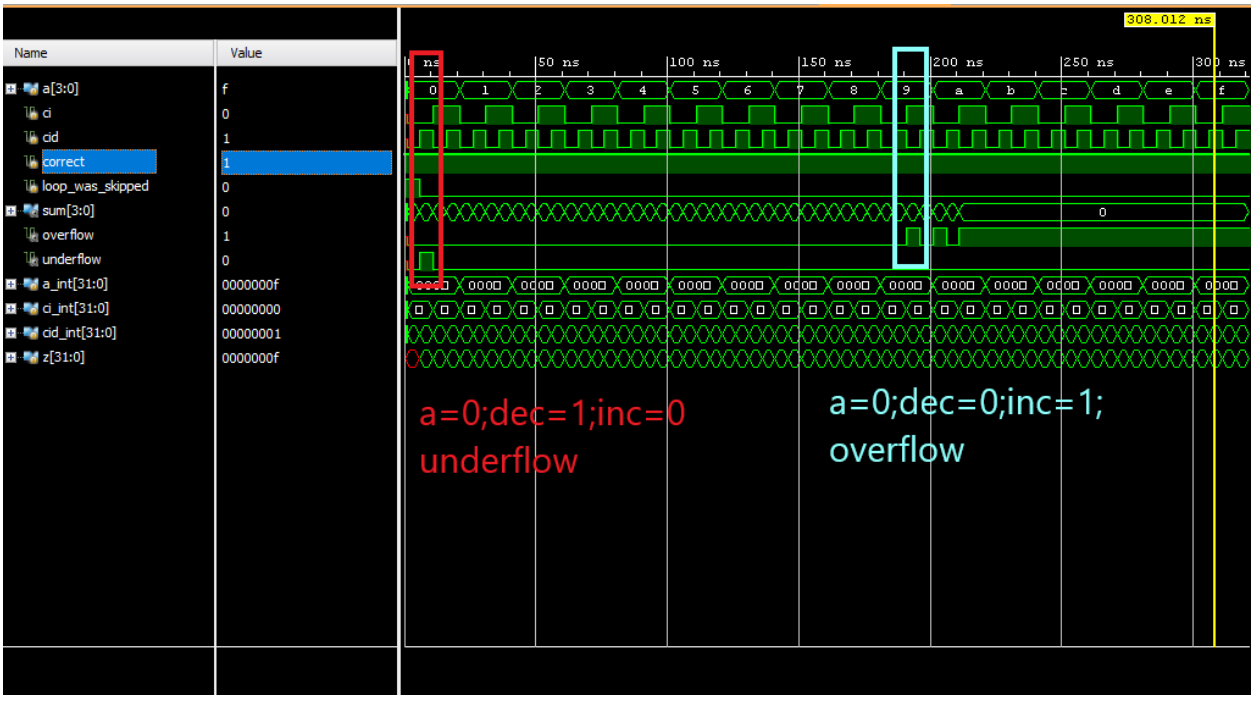
3.d.

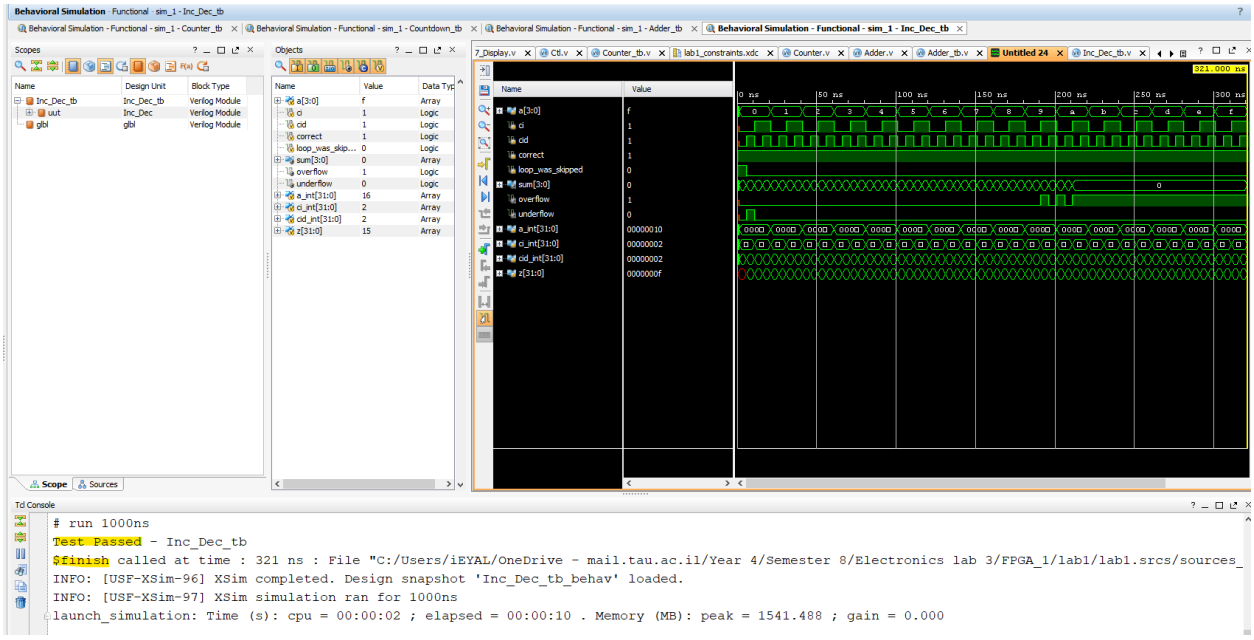

Name
Value
a[3:0]
f
b[3:0]
f
ci
0
correct
1
loop_was_skipped
0
sum[3:0]
e
co
1
ai[31:0]
00000010
bi[31:0]
00000010
cii[31:0]
00000000
1,281.000 ns
1,220 ns
1,230 ns
1,240 ns
1,250 ns
1,260 ns
1,270 ns
0000000f
00000000
f+f=e+co


Behavioral Simulation - Functional - sim_1 - Adder_tb
Behavioral Simulation - Functional - sim_1 - FA_tb
Behavioral Simulation - Functional - sim_1 - Adder_tb
Scopes
Objects
FA.v
FA_tb.v
lab1_constraints.xdc
Adder.v
Adder_tb.v
Untitled 8
Scope
Sources
Tcl Console
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:01 ; elapsed = 00:00:08 . Memory (MB): peak = 1240.266 ; gain = 0.000
run all
Test Passed - Adder_tb
$finish called at time : 1281 ns : File "C:/Users/iEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.srcs/sources_1/imports/lab1_student_sources/Adder_tb.v" Line 58

Q4

4.d.


Name
Value
a[3:0]
ci
cid
correct
loop_was_skipped
sum[3:0]
overflow
underflow
a_int[31:0]
ci_int[31:0]
cid_int[31:0]
z[31:0]
f
0
1
1
0
0
1
0
0000000f
00000000
00000001
0000000f
308.012 ns
a=0;dec=1;inc=0
underflow
a=0;dec=0;inc=1;
overflow


Tcl Console
run 1000ns
Test Passed - Inc_Dec_tb
$finish called at time : 321 ns : File "C:/Users/iEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.srcs/sources_
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Inc_Dec_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:10 . Memory (MB): peak = 1541.488 ; gain = 0.000

Q5

5.a.

First, we shall implement an inc-dec(100MHz) in order to update the clock count (clk_cnt).

The ‘inc’ input to this instance will be high from the moment that count_enabled was switched to high, and the clock count will be reset to zero at that moment as well. (‘dec’ input is set to zero)

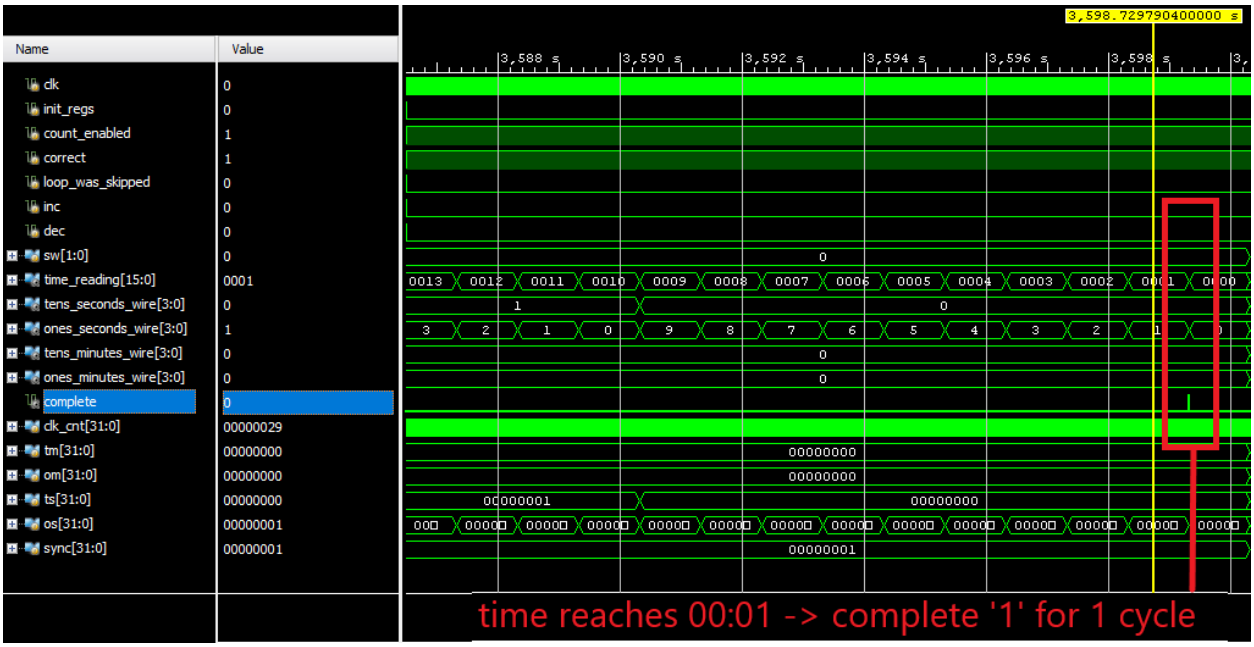
Whenever clk_cnt equals the clock frequency minus 1 (minus 1 because we count from zero), we know that a full clock cycle is complete and therefore a decrease of the seconds should accrue.

So, by implementing an inc-dec(10) for the single seconds (ones_sec) , fed by ‘dec’ input that equals the condition : (clk_cnt = CLK_FREQ-1), the single second will be decreased every 100MHz clock cycle as desired.

In order to update the rest of the time reading, we will implement three additional inc-dec(L) instances. (L=6 for the tens_sec & tens_min ; L=10 for the ones_min)

We will use the ‘underflow’ output of the previous instance to feed the ‘dec’ input of the next. (ones_sec -> tens_sec -> ones_min -> tens_min).

5.e.i.



5.e.ii.

5.e.ii.

Theoretically, the test bench will still test the counting from 59:59 to 00:00, but in practice, the number of iterations required to complete this counting is much larger than the iterations limit.

let's denote the num of tb iteration,when CLK_FREQ= 100Hz, by itr.

if we increase CLK_FREQ to 100MHz, the number of tb iteration will be (iter*M) which is obviously a very large number.

this explains the error received when trying to run the tb after the changes:

```
FATAL_ERROR: Iteration limit 10000 is reached. Possible zero delay oscillation detected where simulation time
```

note:

if we change the timescale as well as the CLK_FREQ by the same factor (CLK_FREQ multiplied by 1M and time res divided by 1M), the delay times (#) will behave exactly like before (since the CLK_PERIOD_IN_TIMEUNITS is divided by 1Msec and the time scale is also decreased by 1Msec).

Q6

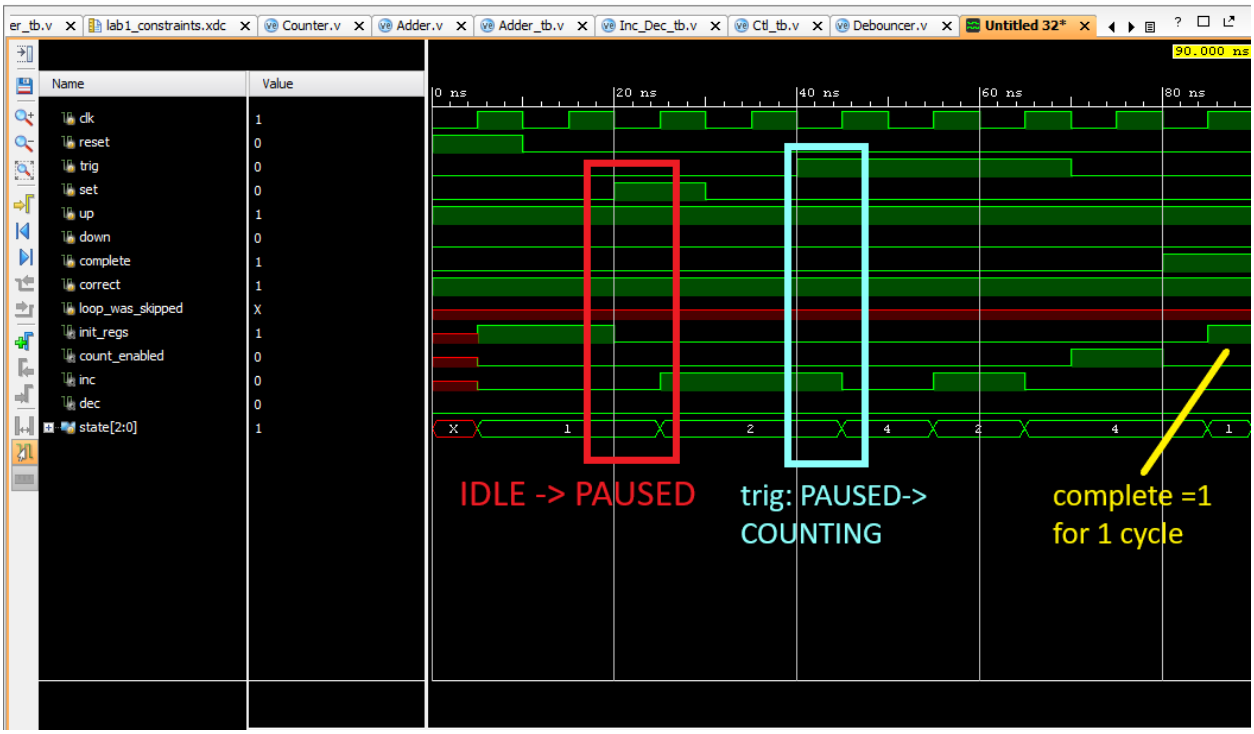
6.d.i.

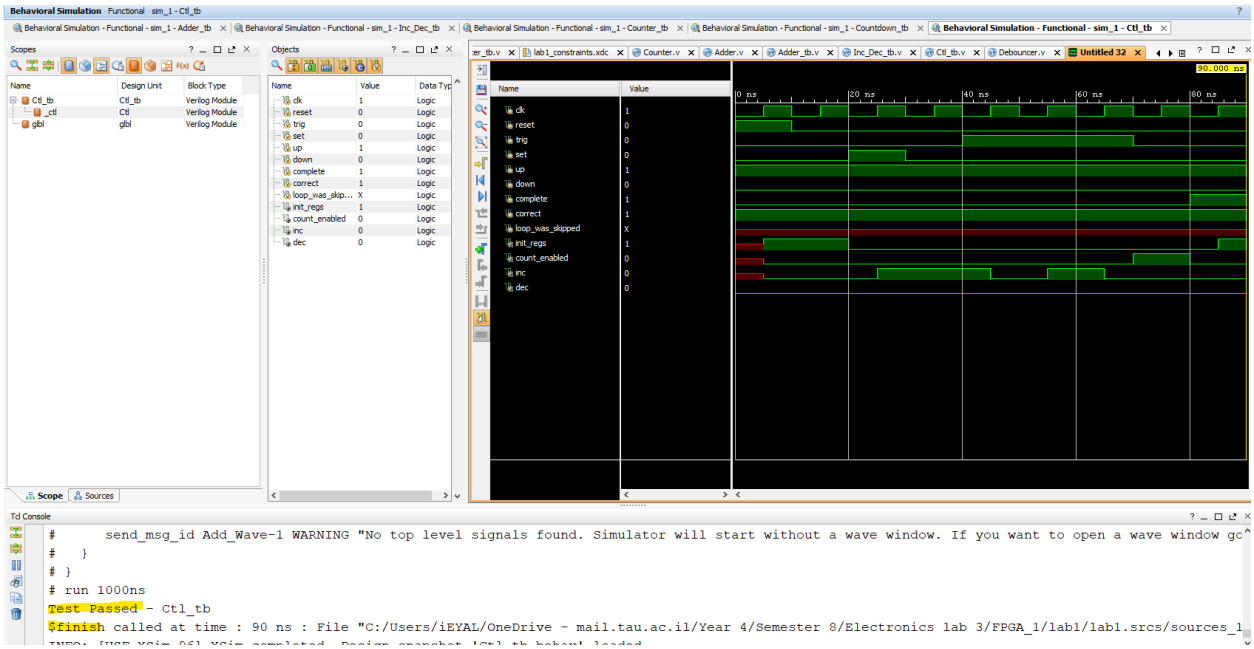
This FSM is **not** a pure Moore FSM.

The output at time t depends on the state at time t and also on the inputs at time t.

For example, if state(t) = ‘IDLE’, output(t) = ‘0000’ or ‘1000’ depending on inputs(t).

6.d.ii.




Behavioral Simulation - Functional - sim_1 - Ctl_tb
Behavioral Simulation - Functional - sim_1 - Adder_tb
Behavioral Simulation - Functional - sim_1 - Inc_Dec_tb
Behavioral Simulation - Functional - sim_1 - Counter_tb
Behavioral Simulation - Functional - sim_1 - Countdown_tb
Behavioral Simulation - Functional - sim_1 - Ctl_tb
Scopes
Objects
Name
Design Unit
Block Type
Ctl_tb
Ctl_tb
Verilog Module
_ctl
Ctl
Verilog Module
glbl
glbl
Verilog Module
Value
Data Typ
clk
reset
trig
set
up
down
complete
correct
loop_was_skip...
init_regs
count_enabled
inc
dec
Logic
Scope
Sources
lab1_constraints.xdc
Counter.v
Adder.v
Adder_tb.v
Inc_Dec_tb.v
Ctl_tb.v
Debouncer.v
Untitled 32
90.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
loop_was_skipped
Tcl Console
send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go
}
}
run 1000ns
Test Passed - Ctl_tb
$finish called at time : 90 ns : File "C:/Users/iEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.srcs/sources_1

Q7

7.c.

Discuss the tradeoff between choosing high and low values for the counter, and how is this related to the low-pass-filter debouncing?

By selecting a high value for the counter we make it more sensitive (it’s closer to the threshold). Meaning a short press on the btn will be enough to trigger a stable single-cycle output.

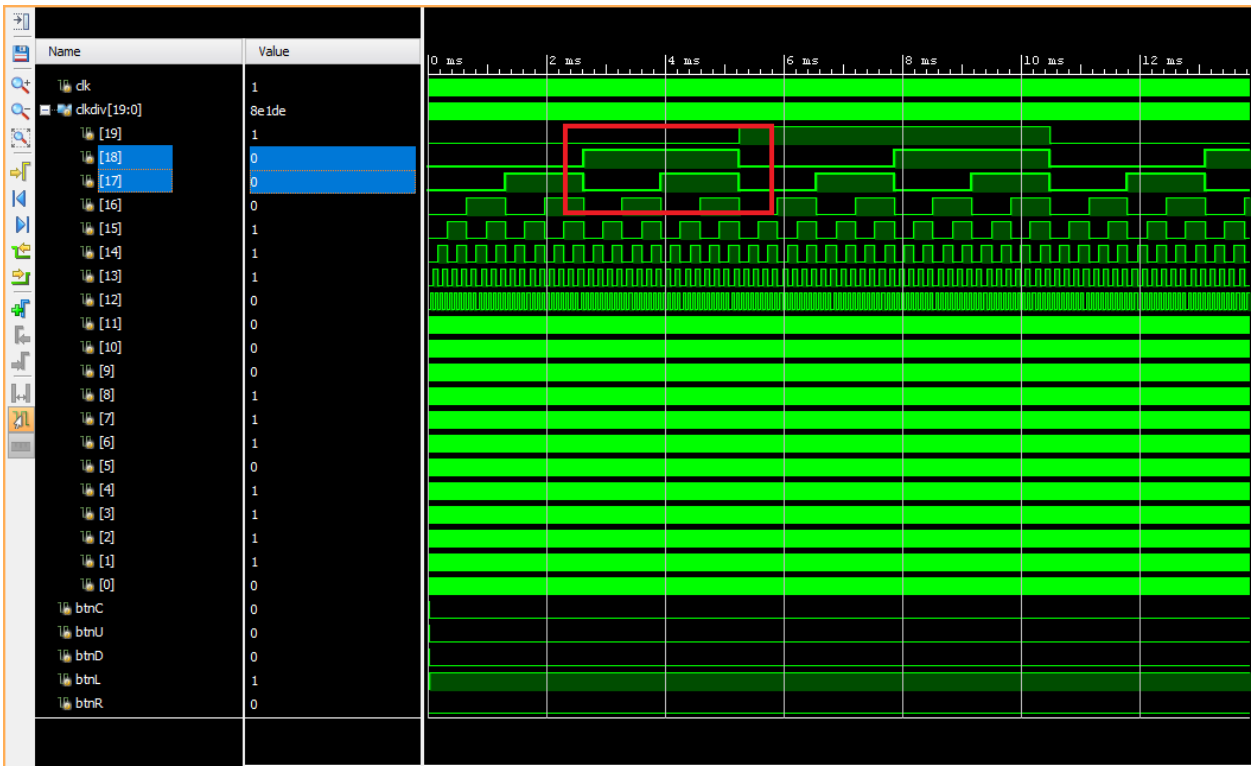
However, it also means that 2 close-together presses intended as one press might be interpreted by the Debouncer as 2 distinctive presses. In addition, some noises might also trigger a stable output.

the tradeoff for a low value counter will be in the very low sensitivity it might have, Making the user press for a longer period of time in order to trigger a reaction. It makes the btn more robust to toggling.

Making the btn less sensitive is decreasing the frequency of it's toggling time, thus making the circuit more LPF by shortening it’s BW.

Q8

8.c



clkdiv has a ratio of 2:1 time_period for every bit from LSB to MSB. the LSB is changing at 100MHZ thus making it's time_period=10^-8sec.

in order to achieve a flashing time_period between 1-16msec, we chose bits [18:17]. these bits allow the display to change as follows:

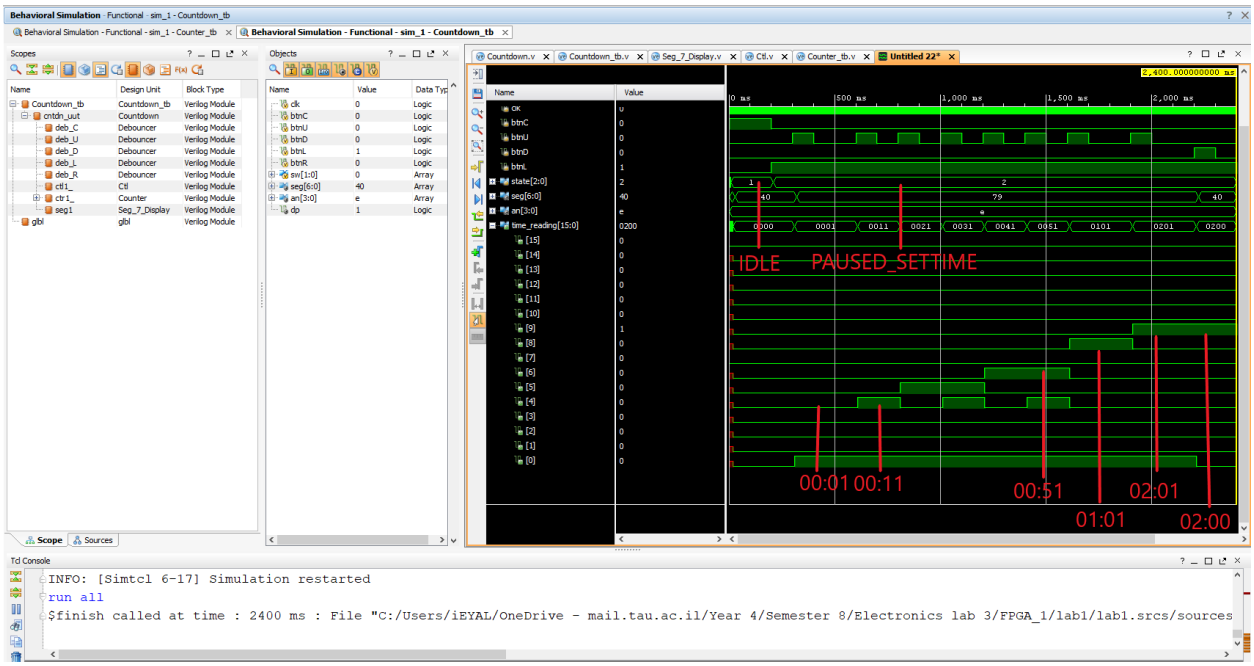
bit17period= (100M)^-1 * 2^17 = 1.31 msec

bit18 period= (100M)^-1 * 2^18 = 2.62 msec

The signal simulation above shows the same results.

Q10

10.d.i.



10.d.ii.

In our Countdown_tb simulation we wanted to check the following functions of Countdown:

- switching from state IDLE to PAUSED_SETTIME using reset & set
- changing the displayed time using the UP & DOWN btns
- expected time_reading value displayed after incrementing / decrementing

We did so by initializing the FSM to IDLE (btn reset), then set it to PAUSED_SETTIME (btn set) and afterwards setting the time displayed (btns up/down).

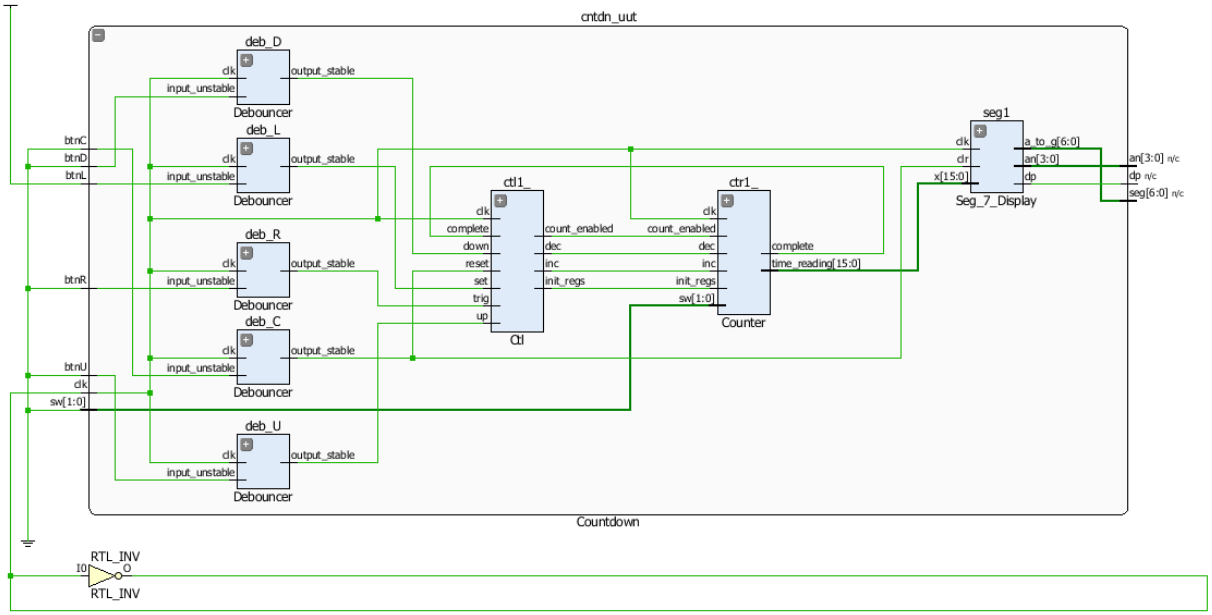
The btns were simulated by regs and the outputs by wires.

Also, we wanted to make sure that incrementing a digit over limit (tens_sec over 5 for example, will trigger a shift in the next digit and set the overflowing digit to 0). we did so by incrementing sec_tens 6 times, watching it change to 0 and min_ones incrementing to 1.

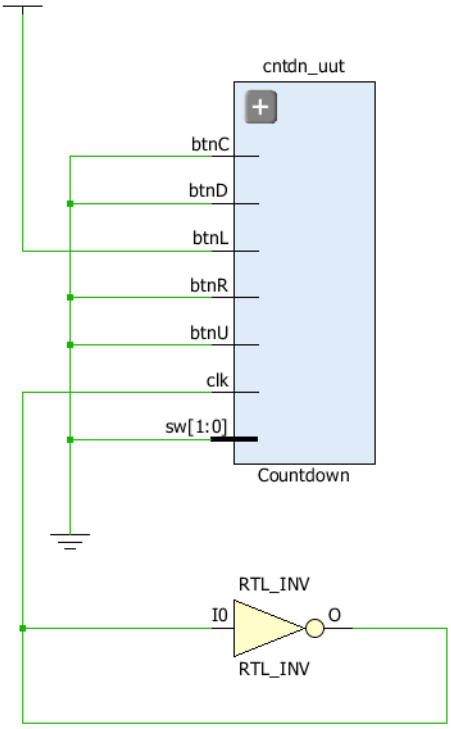
All these were examined in out TB and displayed in the behavioral simulation.

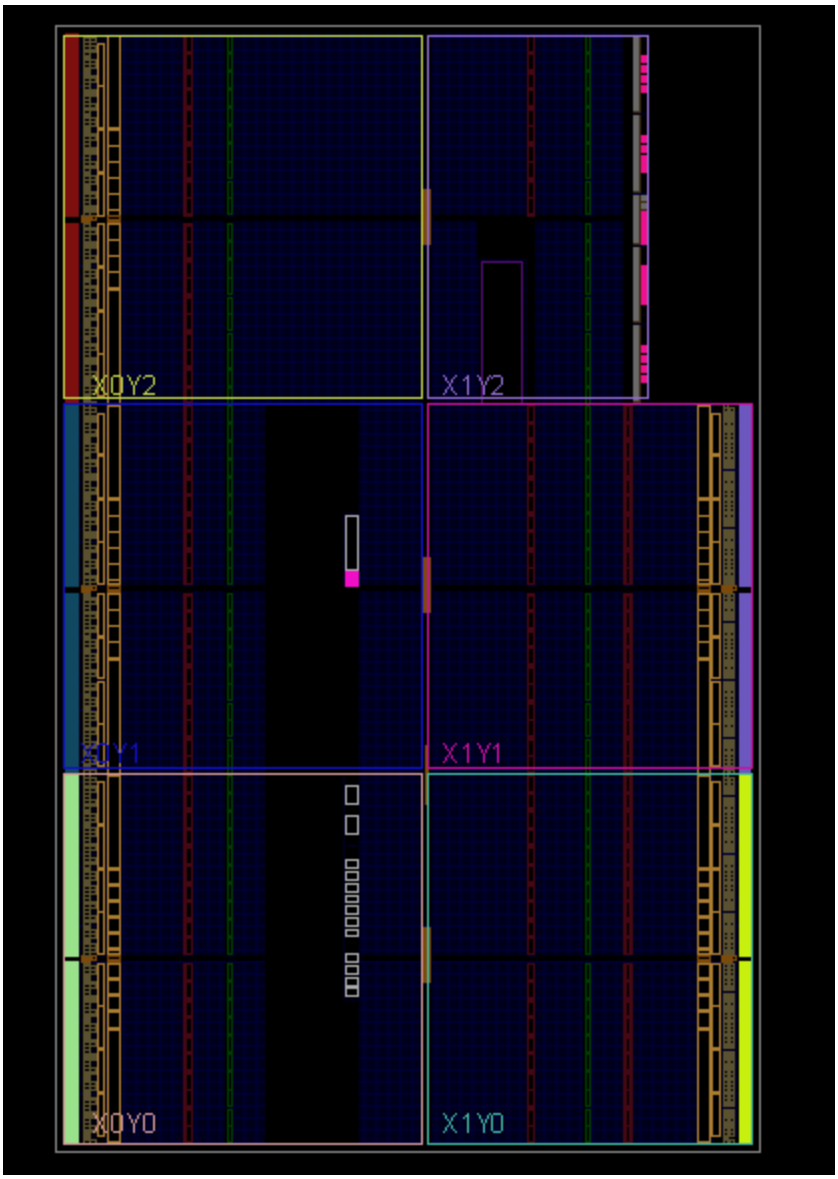
Q11

11.a.


cntdn_uut
deb_D
deb_L
deb_R
deb_C
deb_U
Debouncer
clk
input_unstable
output_stable
btnC
btnD
btnL
btnR
btnU
sw[1:0]
ctl1_
Ctl
complete
down
reset
set
trig
up
count_enabled
dec
inc
init_regs
ctr1_
Counter
sw[1:0]
time_reading[15:0]
seg1
Seg_7_Display
dir
x[15:0]
a_to_g[6:0]
an[3:0]
dp
seg[6:0]
Countdown
RTL_INV
I0
O

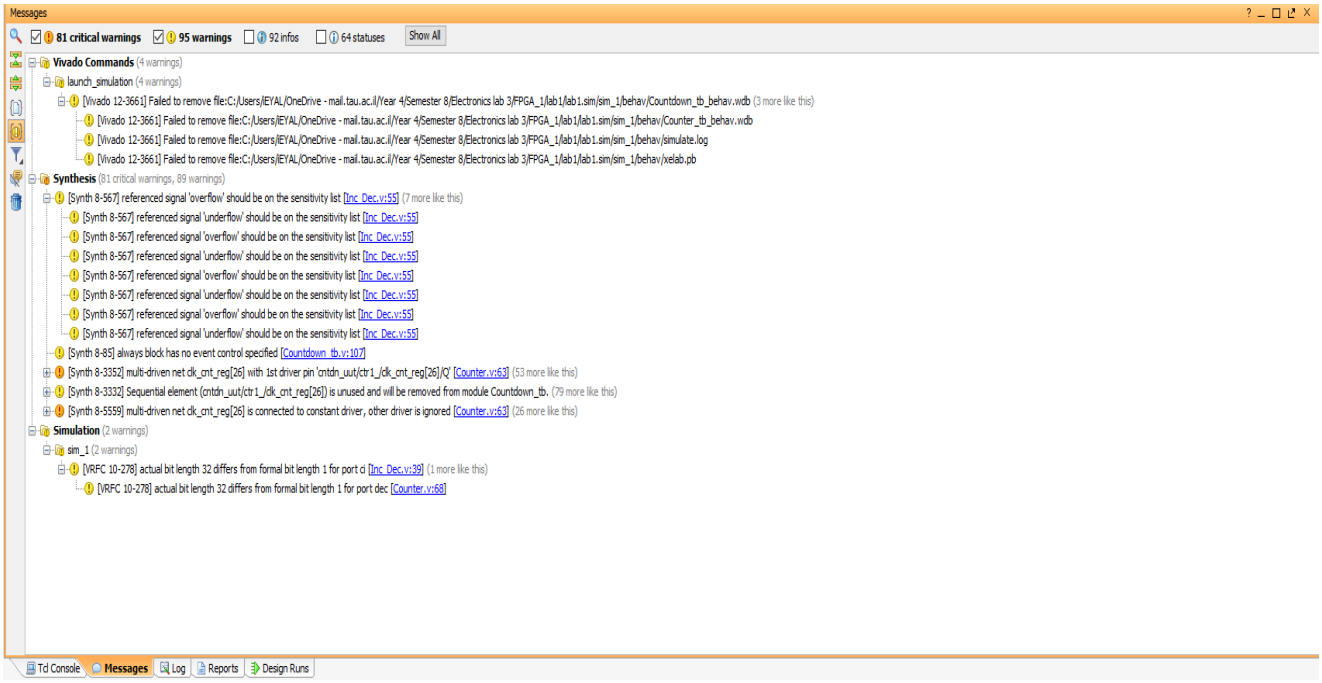
11.b.


cntdn_uut
btnC
btnD
btnL
btnR
btnU
clk
sw[1:0]
Countdown
RTL_INV
I0
O



The elaborated design shows the logical data & control paths in a graphic manner. It doesn't represent the physical positioning of the gates and wires on the board. On the other hand, the post synthesis design shows the actual wiring and layout of the circuit. Moreover, it optimizes the logic by omitting redundant registers from the design thus saving room on the chip.

11.c.


Messages
81 critical warnings
95 warnings
92 infos
64 statuses
Show All
Vivado Commands (4 warnings)
launch_simulation (4 warnings)
[Vivado 12-3661] Failed to remove file:C:/Users/IEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.sim/sim_1/behav/Countdown_tb_behav.wdb (3 more like this)
[Vivado 12-3661] Failed to remove file:C:/Users/IEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.sim/sim_1/behav/Counter_tb_behav.wdb
[Vivado 12-3661] Failed to remove file:C:/Users/IEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.sim/sim_1/behav/simulate.log
[Vivado 12-3661] Failed to remove file:C:/Users/IEYAL/OneDrive - mail.tau.ac.il/Year 4/Semester 8/Electronics lab 3/FPGA_1/lab1/lab1.sim/sim_1/behav/xelab.pb
Synthesis (81 critical warnings, 89 warnings)
[Synth 8-567] referenced signal 'overflow' should be on the sensitivity list [Inc_Dec.v:55] (7 more like this)
[Synth 8-567] referenced signal 'underflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'overflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'underflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'overflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'underflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'overflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-567] referenced signal 'underflow' should be on the sensitivity list [Inc_Dec.v:55]
[Synth 8-85] always block has no event control specified [Countdown_tb.v:107]
[Synth 8-3352] multi-driven net clk_cnt_reg[26] with 1st driver pin 'cntdn_uut/ctr1_/clk_cnt_reg[26]/Q' [Counter.v:63] (53 more like this)
[Synth 8-3332] Sequential element (cntdn_uut/ctr1_/clk_cnt_reg[26]) is unused and will be removed from module Countdown_tb. (79 more like this)
[Synth 8-5559] multi-driven net clk_cnt_reg[26] is connected to constant driver, other driver is ignored [Counter.v:63] (26 more like this)
Simulation (2 warnings)
sim_1 (2 warnings)
[VRFC 10-278] actual bit length 32 differs from formal bit length 1 for port d [Inc_Dec.v:39] (1 more like this)
[VRFC 10-278] actual bit length 32 differs from formal bit length 1 for port dec [Counter.v:68]
Tcl Console
Messages
Log
Reports
Design Runs