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2 REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|--|-------------------|
| Rev. 1.0 | Initial Issue | Jul.5.2018 |
| Rev. 1.1 | Revised <u>7 ORDERING INFORMATION</u> in page 6 | Apr.8.2022 |
| Rev. 1.2 | 1. Deleted <u>3 FEATURES</u> ■ Package : 8-pin 5mm x 6mm WSON & Deleted <u>5 PIN CONFIGURATION</u> WSON(Top View) & <u>WSON(See Through with Top View)</u> in page 3 2. Deleted <u>8-pin 5mm x 6mm WSON Package Outline Dimension</u> in page 5 3.Revised <u>7. ORDERING INFORMATION</u> in page 6 | May.23.2023 |



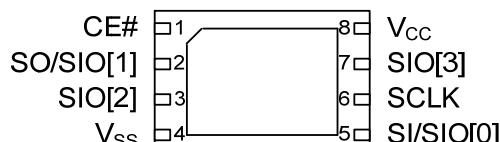
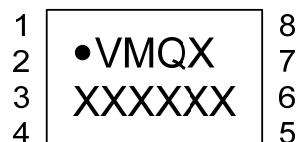
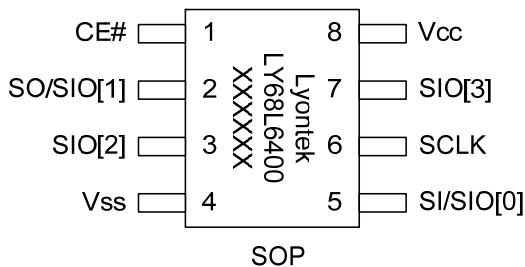
3 FEATURES

- 50Ω Output Drive Strength LVC MOS.
- Linear Burst (continuous) or 32 byte wrapped burst via toggle command.
- Linear Burst is supported up to 84MHz and can cross page boundary as long as t_{CEN} is met.
- Software reset.
- **Green package available**
- Package : 8-pin 150mil SOP
8-pin 2mm x 3mm DFN

4 SPECIFICATIONS

- Single Supply Voltage:
 - V_{CC}=2.7 to 3.6V
- Interface: SPI/QPI with SDR mode
- Performance: Clock rate up to
 - 133MHz (non-page boundary crossing)
 - 84MHz (page boundary crossing)
- Organization: 64Mb, 8M x 8bits
- Addressable bit range: A[22:0]
- Page size: 1024 bytes
- Refresh: Self-managed
- Operating temperature range
 - T_C = -40°C to +85°C
- Maximum Standby Current:
 - 200μA @ 85°C

5 PIN CONFIGURATION

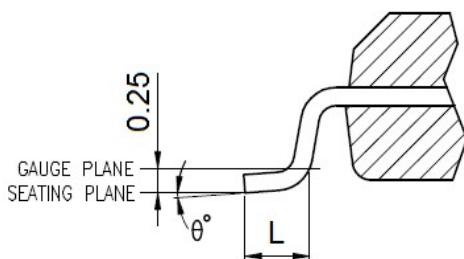
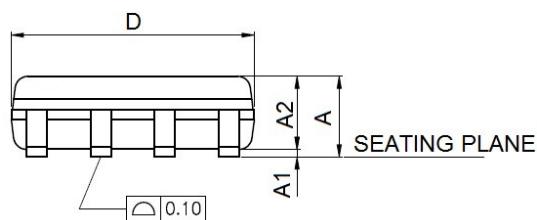
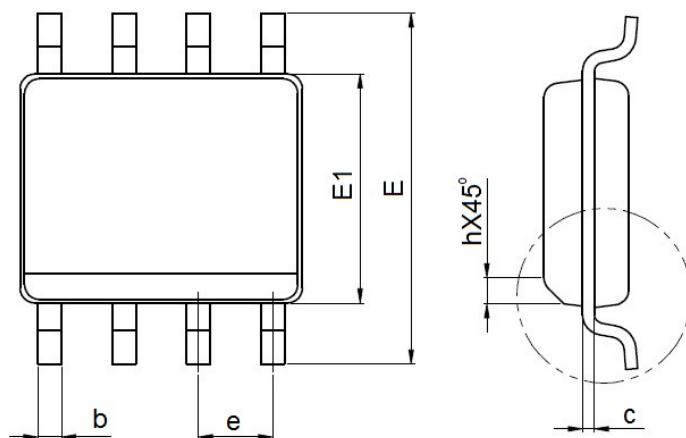


Note: DFN package with special top marking due to size limitation.
V : LY68L series, M : 64Mb, Q : S/QPI, X : DFN



6 PACKAGE OUTLINE DIMENSION

8-pin 150mil SOP Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | STANDARD | |
|----------------|----------|------|
| | MIN. | MAX. |
| A | — | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | — |
| b | 0.31 | 0.51 |
| c | 0.10 | 0.25 |
| D | 4.90 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.50 |
| θ° | 0 | 8 |

NOTES:

- 1.JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
MS-012 BA REV.F (THERMAL)
- 2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH,
PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS
AND GATE BURRS SHALL NOT EXCEED 0.15mm.
PER SIDE.
- 3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH,
OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS
SHALL NOT EXCEED 0.25mm PER SIDE.



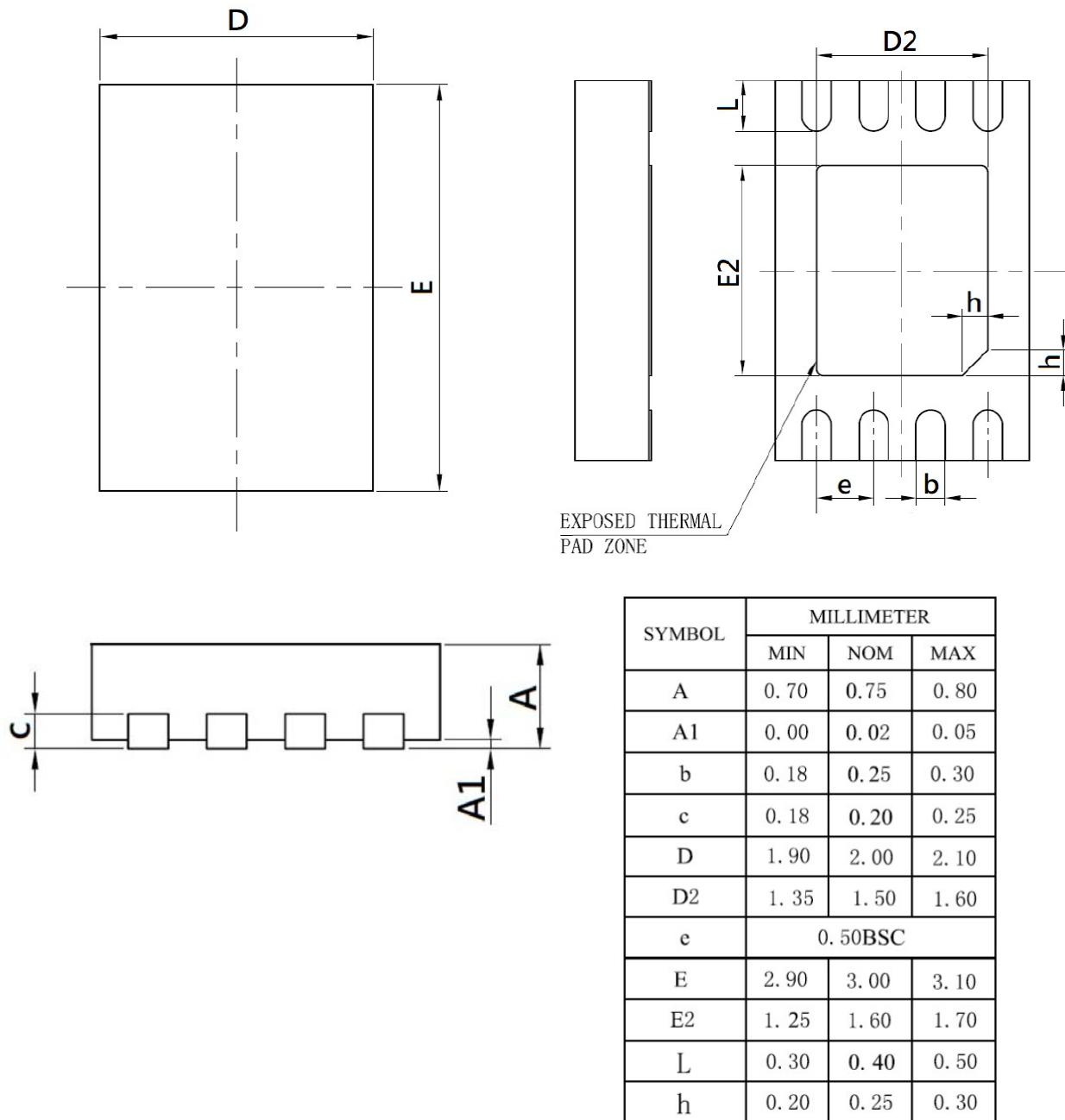
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LY68L6400

Rev. 1.2

64M Bits Serial Pseudo-SRAM with SPI and QPI

8-pin 2mm x 3mm DFN Package Outline Dimension





7 ORDERING INFORMATION

Table 1: Ordering Information

| Package Type | Maximum Clock Rate(MHz) | Temperature Range(°C) | Packing Type | Lyontek Item No. |
|--------------------------|-------------------------|-----------------------|------------------|------------------|
| 8-pin (150mil) SOP | 133 | -40°C~85°C | Tube(For Sample) | LY68L6400SLI |
| | | | Tape Reel | LY68L6400SLIT |
| 8-pin (2mm x 3mm) DFN | 144 | -40°C~85°C | Tape Reel | LY68L6400BAIT |

8 PIN DESCRIPTION

Table 2: Signals Table

| SYMBOL | TYPE | SPI Mode Function | QPI Mode Function | COMMENTS |
|-----------|--------|--|--------------------|----------|
| Vcc | Power | | Core supply 3V | |
| Vss | Ground | | Core supply ground | |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state. | | |
| CLK | Input | | Clock Signal | |
| SI/SIO[0] | I/O | Serial Input | I/O[0] | |
| SO/SIO[1] | I/O | Serial Output | I/O[1] | |
| SIO[2] | I/O | - | I/O[2] | |
| SIO[3] | I/O | - | I/O[3] | |



9 POWER-UP INITIALIZATION

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{CC} reaches a stable level at or above minimum V_{CC} , the device will require $150\mu s$ and user-issued RESET Operation (see section 14) to complete its self-initialization process. From the beginning of power ramp to the end of the $150\mu s$ period, CLK should remain LOW, CE# should remain HIGH (track V_{CC} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the $150\mu s$ period the device is ready for normal operation.

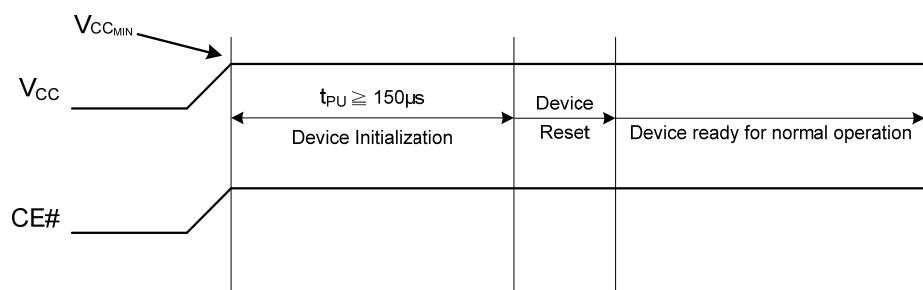


Figure 1 : Power-Up Initialization Timing



10 INTERFACE DESCRIPTION

10.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 64M device is addressed with A[22:0].

10.2 Page Size

Page size is 1K (CA[9:0]). Default burst setting is Linear Bursting that crosses page boundary in a continuous manner. Note however that burst operations which cross page boundary have a lower max input clock frequency of 84MHz. Optionally the device can also be set to wrap 32 (CA[4:0]) via the Wrap Boundary Toggle command and is not allowed to cross page boundary in this configuration.

10.3 Drive Strength

The device powers up in 50Ω.

10.4 Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

10.5 Truth Table

The device recognizes the following commands specified by the various input methods.

| COMMAND | CODE | SPI Mode (QE=0) | | | | | QPI Mode (QE=1) | | | | |
|------------------|------|-----------------|------|------------|-----|-------------------|-----------------|------|------------|-----|-------------------|
| | | CMD | Addr | Wait Cycle | DIO | MAX. Freq. | CMD | Addr | Wait Cycle | DIO | MAX. Freq. |
| Read | 'h03 | S | S | 0 | S | 33 | | | | | N/A |
| Fast Read | 'h0B | S | S | 8 | S | 133 | | | | | N/A |
| Fast Read Quad | 'hEB | S | Q | 6 | Q | 133 | Q | Q | 6 | Q | 133 ^{*1} |
| Write | 'h02 | S | S | 0 | S | 133 ^{*2} | Q | Q | 0 | Q | 133 ^{*1} |
| Quad Write | 'h38 | S | Q | 0 | Q | 133 | Same as 'h02 | | | | |
| Enter Quad Mode | 'h35 | S | - | - | - | 133 | N/A | | | | |
| Exit Quad Mode | 'hF5 | N/A | | | | | Q | - | - | - | 133 |
| Reset Enable | 'h66 | S | - | - | - | 133 | Q | - | - | - | 133 |
| Reset | 'h99 | S | - | - | - | 133 | Q | - | - | - | 133 |
| Set Burst Length | 'hC0 | S | - | - | - | 133 | Q | - | - | - | 133 |
| Read ID | 'h9F | S | S | 0 | S | 133 | N/A | | | | |

Remarks: S = Serial I/O, Q = Quad I/O

Note: 1. 133MHz max without crossing page boundary, and 84MHz max when burst commands cross page boundary.
2. Linear burst is prohibited.

10.6 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

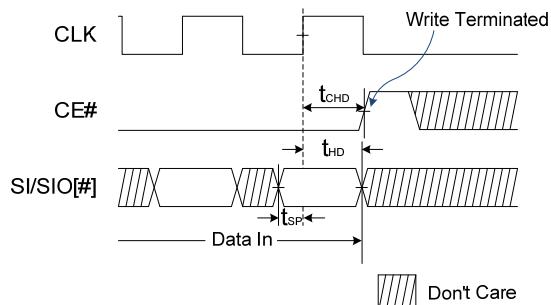


Figure 2 : Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time ($t_{CHD} > t_{ACLK} + t_{CLK}$) for a sufficient data window.

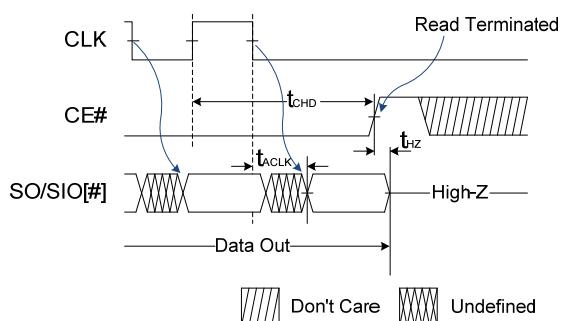


Figure 3 : Read Command Termination

11 WRAP BOUNDARY TOGGLE OPERATION

The Wrap Boundary Toggle Operation switches the device's wrapped boundary between Linear Burst which crosses the 1K page boundary (CA[9:0]) and wrap 32 (CA[4:0]) bytes. Default setting is Linear Burst.

Linear Burst allows the device to burst through page boundary. Page boundary crossing is invisible to the memory controller and limited to lower max CLK frequency of 84MHz. Table 3 shows an example of the sequence of bytes.

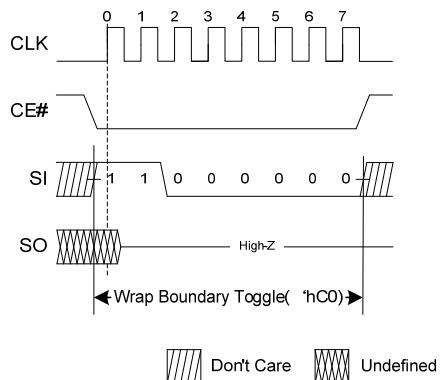


Figure 4 : SPI Wrap Boundary Toggle 'hC0'

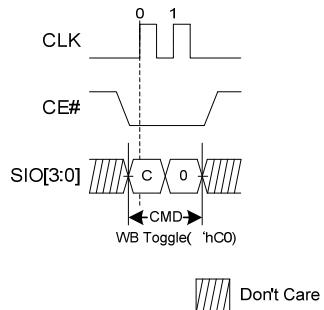


Figure 5 : QPI Wrap Boundary Toggle 'hC0'

Table 3: Burst Type / Length

| Burst Type / Length | Starting Address | Byte Sequence |
|---------------------|------------------|------------------------------------|
| Linear Burst | 4 | [4,5,6,...1023,1024,1025,1026,...] |
| Wrap 32 | 4 | [4,5,6,...31,0,1,2,...] |

12 SPI MODE OPERATIONS

The device powers up into SPI mode by default but can also be switched into QPI mode.

12.1 SPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

SPI Reads can be done in three ways:

1. 'h03: Serial CMD, Serial I/O, slow frequency, with linear or burst wrap of 32 byte configurability.
2. 'h0B: Serial CMD, Serial I/O, fast frequency, with burst wrap of 32/1K byte configurability.
3. 'hEB: Serial CMD, Quad I/O, fast frequency, with burst wrap of 32/1K byte configurability.

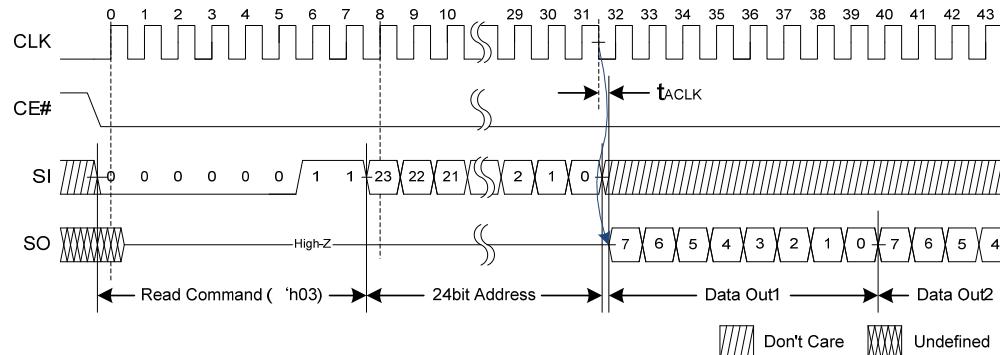


Figure 6 : SPI Read 'h03 (MAX. freq. 33MHz)

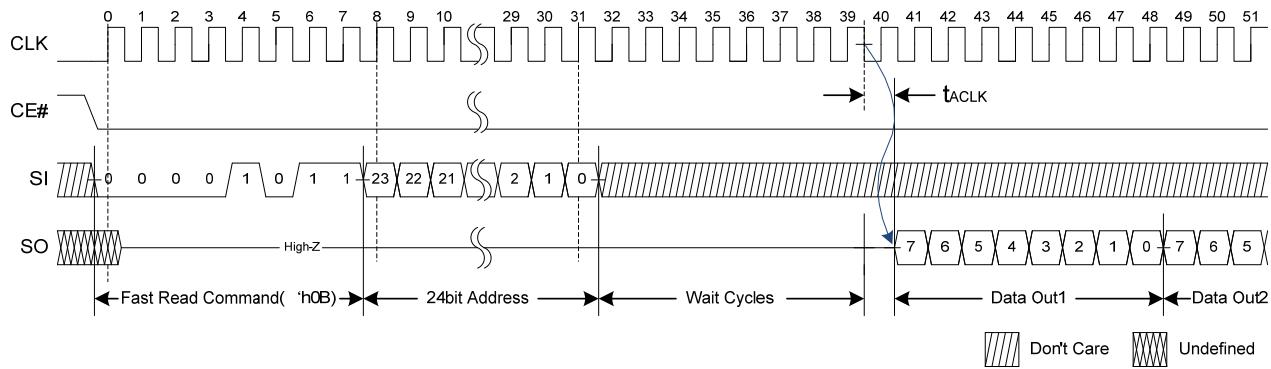


Figure 7 : SPI Fast Read 'h0B (MAX. freq. 133MHz)



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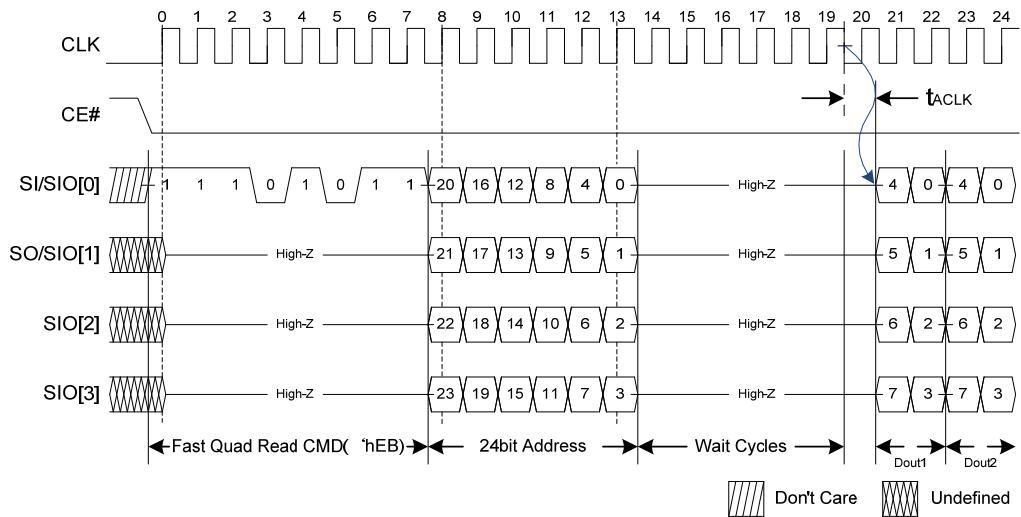


Figure 8 : SPI Fast Quad Read 'hEB (MAX. freq. 133MHz)



12.2 SPI Write Operations

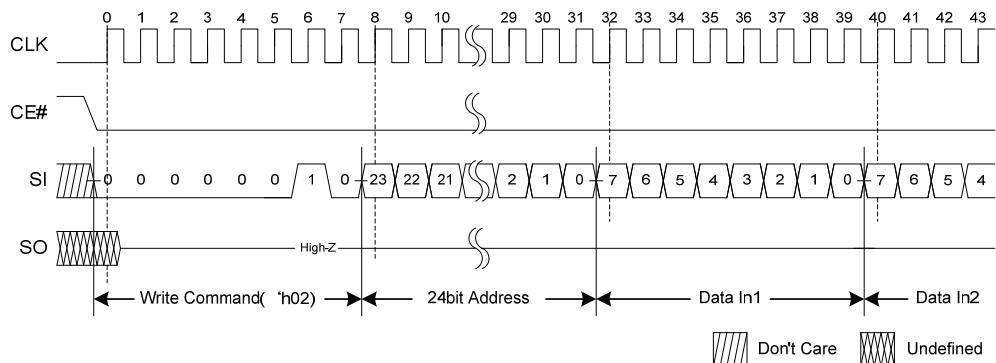


Figure 9 : SPI Write 'h02'

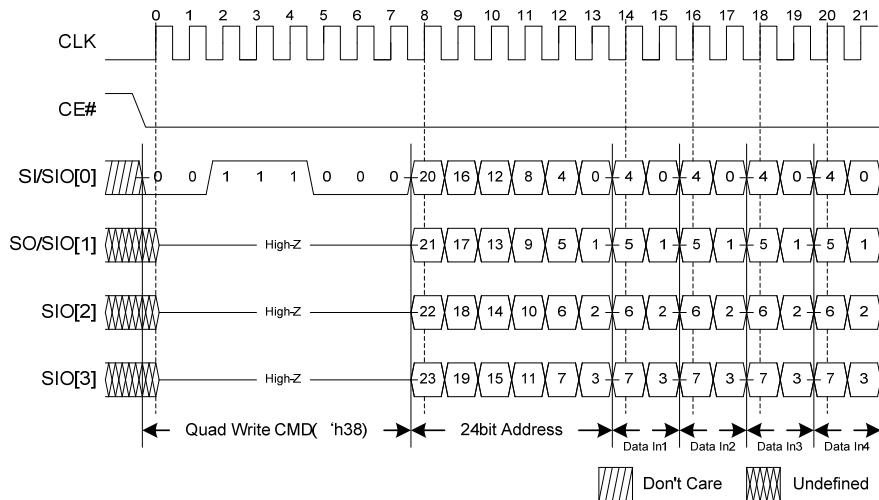
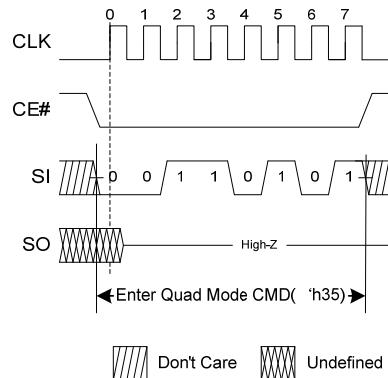


Figure 10 : SPI Quad Write 'h38'

12.3 SPI Quad Mode Enable Operation

This command switches the device into quad I/O mode.



**Figure 11 : Quad Mode Enable ‘h35
(available only in SPI mode)**

12.4 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

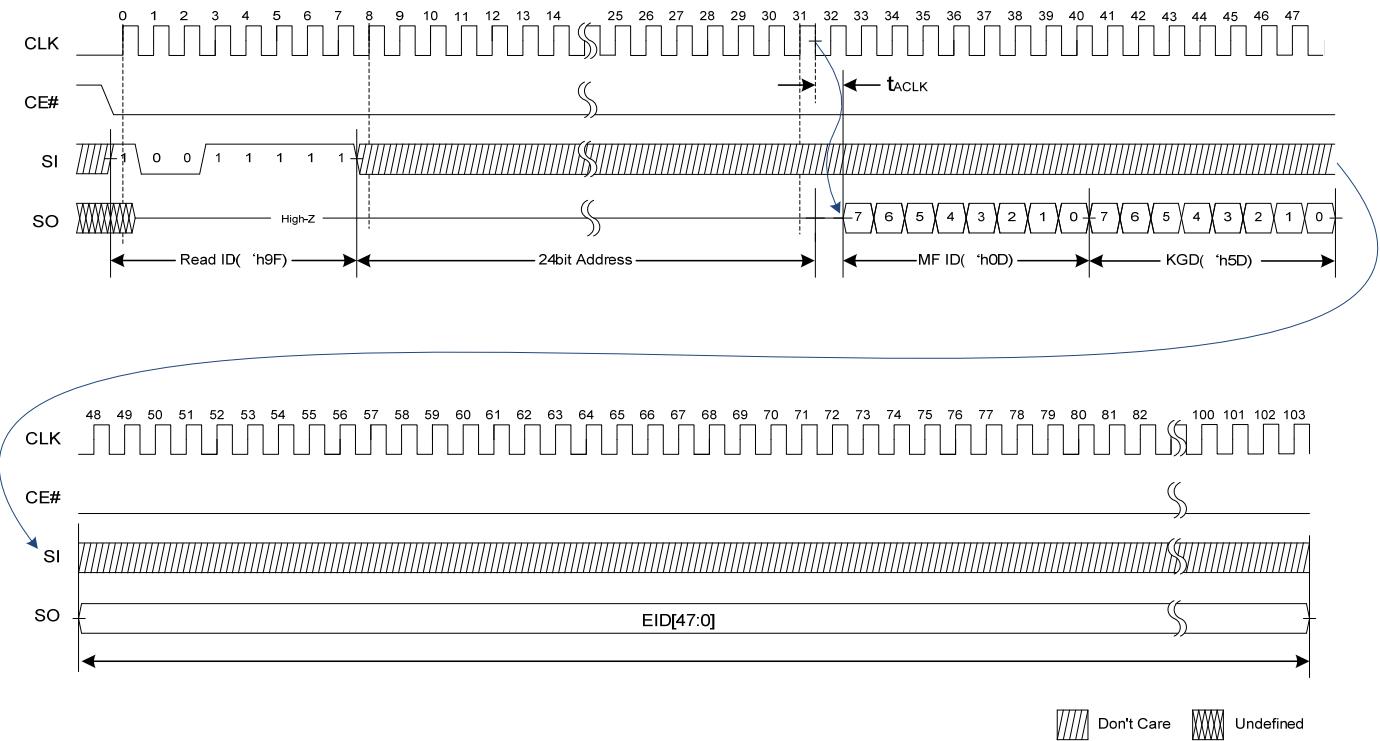


Figure 12 : SPI Read ID ‘h9F (available only in SPI mode)

Table 4: Known Good Die (KGD)

| KGD[7:0] | Known Good Die |
|-------------|----------------|
| 'b0101_0101 | FAIL |
| 'b0101_1101 | PASS |

*Note: Default is FAIL die, and only mark PASS after all tests passed.

13 QPI MODE OPERATIONS

13.1 QPI Read Operations

For all reads, data will be available t_{ACLK} after the falling edge of CLK.

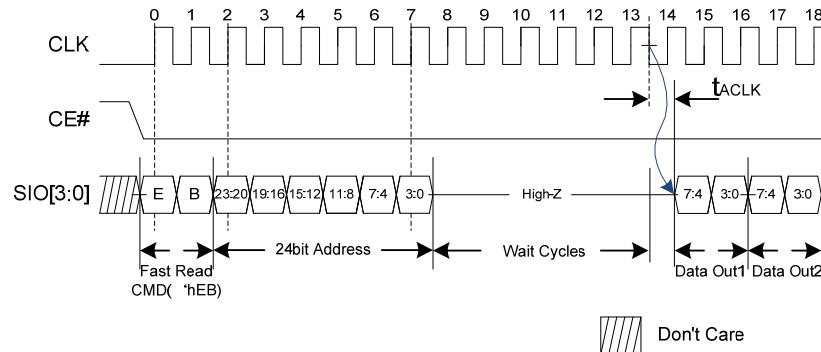


Figure 13 : QPI Fast Read 'hEB (MAX. freq. 133MHz)

13.2 QPI Write Operation(s)

QPI write command can be input as 'h02 or 'h38.

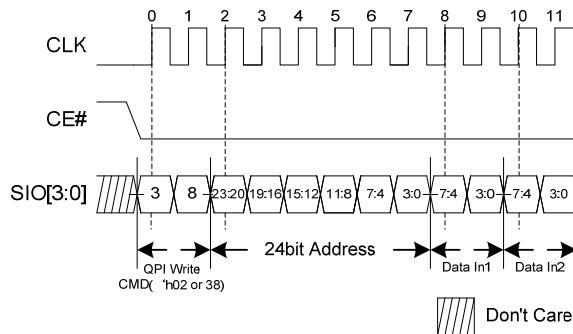
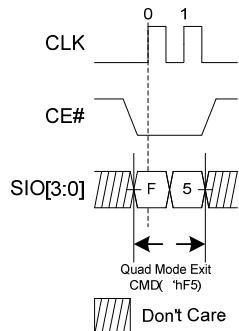


Figure 14 : QPI Write 'h02 or 'h38



13.3 QPI Quad Mode Exit Operation

This command will switch the device back into serial I/O mode.



**Figure 15 : Quad Mode Exit 'hF5
(only available in QPI mode)**

14 RESET OPERATION

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

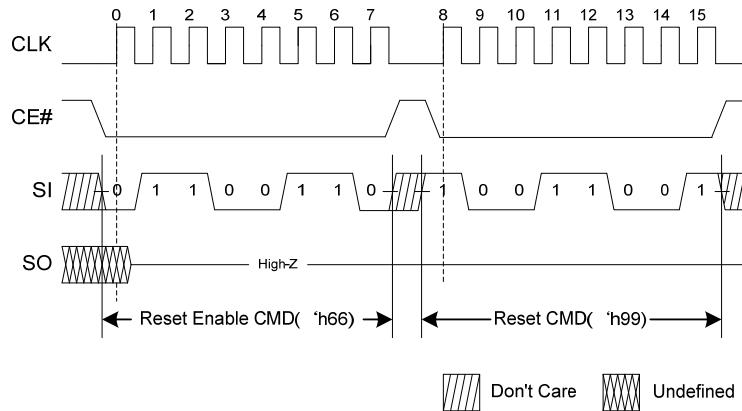


Figure 16 : SPI Reset

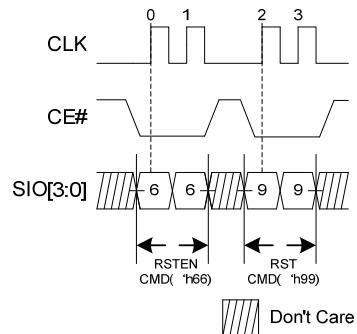


Figure 17 : QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

15 INPUT / OUTPUT TIMING

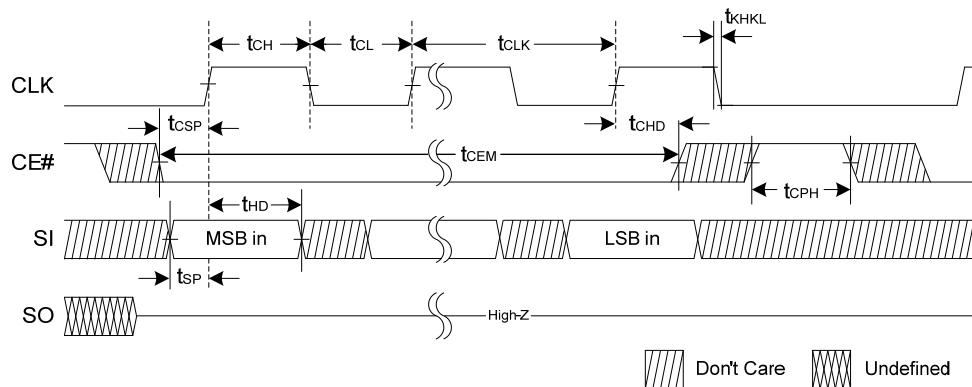


Figure 18 : Input Timing

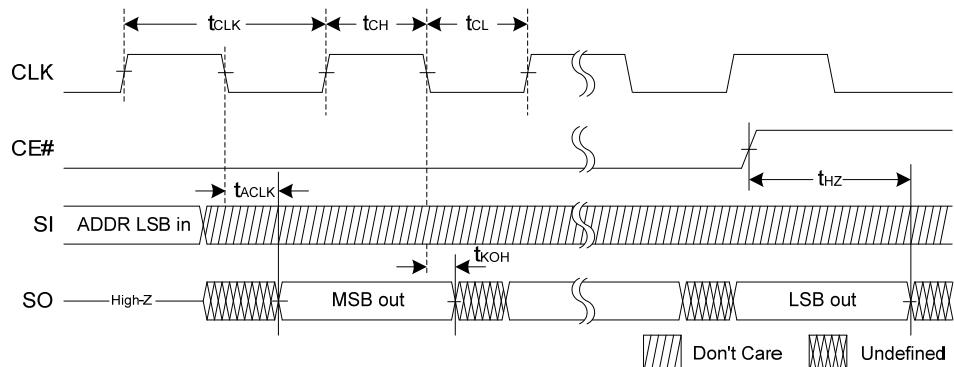


Figure 19 : Output Timing



16 ELECTRICAL SPECIFICATIONS

16.1 Absolute Maximum Ratings*

Table 5: Absolute Maximum Ratings*

| PARAMETER | SYMBOL | RATING | UNIT | NOTES |
|---|------------------|------------------------------|------|-------|
| Voltage to any pad except V _{CC} relative to V _{SS} | V _T | -0.3 to V _{CC} +0.3 | V | |
| Voltage on V _{CC} supply relative to V _{SS} | V _{CC} | -0.2 to +4.2 | V | |
| Storage Temperature | T _{STG} | -55 to +150 | °C | 1 |

Note: 1. Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

* Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

16.2 Pin Capacitance

Table 6: Package Pin Capacitance

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | NOTES |
|------------------------|------------------|------|------|------|----------------------|
| Input Pin Capacitance | C _{IN} | - | 6 | pF | V _{IN} =0V |
| Output Pin Capacitance | C _{OUT} | - | 8 | pF | V _{OUT} =0V |

Note: 1. Spec'd at 25°C.

16.3 Operating Conditions

Table 7: Operating Characteristics

| PARAMETER | MIN. | MAX. | UNIT |
|-----------------------|------|------|------|
| Operating Temperature | -40 | 85 | °C |



16.4 DC Electrical Characteristics

Table 8: DC Characteristics

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | NOTES |
|-----------------|---|----------------------|----------------------|------|-------|
| V _{CC} | Supply Voltage | 2.7 | 3.6 | V | |
| V _{IH} | Input high voltage | V _{CC} -0.4 | V _{CC} +0.2 | V | |
| V _{IL} | Input low voltage | -0.2 | 0.4 | V | |
| V _{OH} | Output high voltage (I _{OH} =-0.2mA) | 0.8 V _{CC} | - | V | |
| V _{OL} | Output low voltage (I _{OL} =+0.2mA) | - | 0.2 V _{CC} | V | |
| I _{LI} | Input leakage current | - | 1 | μA | |
| I _{LO} | Output leakage current | - | 1 | μA | |
| I _{CC} | Read/Write | - | 40 | mA | |
| I _{SB} | Standby current | - | 200 | μA | 1 |

Note: 1. Standby current is measured when CLK is in DC low state.

16.5 AC Electrical Characteristics

Table 9: READ/WRITE Timing

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | NOTES |
|-----------------------------------|--|------|------|------------------------|------------------------|
| t _{CLK} | CLK period - SPI Read('h03) | 30.3 | - | ns | 33MHz |
| | CLK period - all other operations | 7 | - | | 133MHz ^{*1,2} |
| t _{CH} / t _{CL} | Clock high/low width | 0.45 | 0.55 | t _{CLK} (min) | |
| t _{KHKL} | CLK rise or fall time | - | 1.5 | ns | |
| t _{CPH} | CE# HIGH between subsequent burst operations | 50 | - | ns | |
| t _{CEM} | CE# low pulse width | - | 8 | μs | |
| t _{CS} | CE# setup time to CLK rising edge | 2.5 | - | ns | |
| t _{CHD} | CE# hold time from CLK rising edge | 20 | - | ns | |
| t _{SP} | Setup time to active CLK edge | 2 | - | ns | |
| t _{HD} | Hold time from active CLK edge | 2 | - | ns | |
| t _{HZ} | Chip disable to DQ output high-Z | - | 6 | ns | |
| t _{ACLK} | CLK to output delay | 2 | 6 | ns | |
| t _{KOH} | Data hold time from clock falling edge | 1.5 | - | ns | |

Note: 1. Only Linear Burst allows page boundary crossing. Frequency limits are therefore
133MHz MAX. without crossing page boundary, and
84MHz MAX. when burst commands cross page boundary.

2. For operating frequencies > 84MHz, refer to JEDEC JESD84-B50 for data sampling training.



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