

## Software Upgrade for the CMS Layer1 Module

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## Section 1

### Motivation

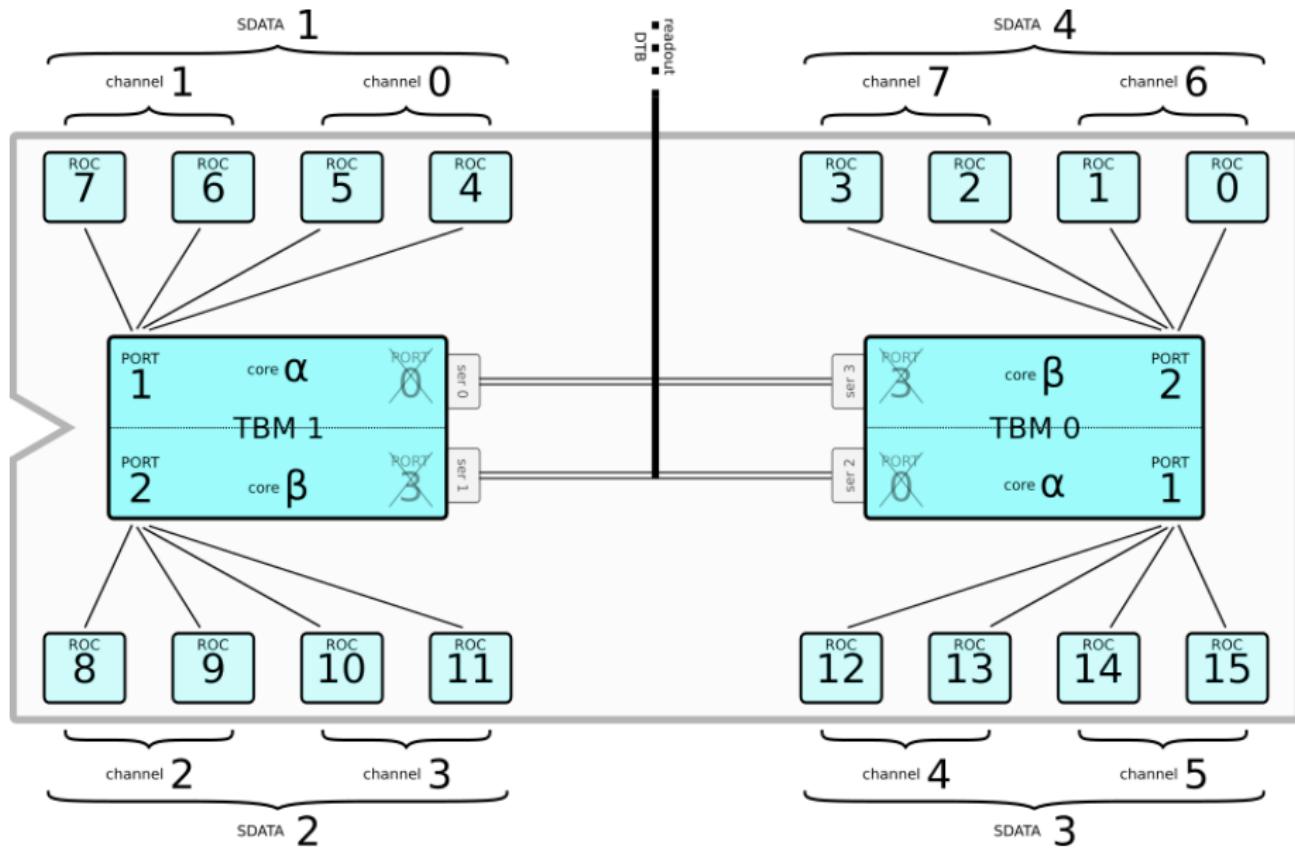
- tracker has to handle larger amount of data
  - ▶ 50 instead of 25 collisions per bunch crossing after the next upgrade
- adding innermost layer to the CMS tracker with a new module design (highest data volume)
  - ▶ equipped with new PROC600 as ROC → higher data processing speed
- current modules currently work with one TBM which has two SDATA lines
  - ▶ 8 ROCs per line
- improve readout speed by adding a second TBM

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## Section 2

### Layout

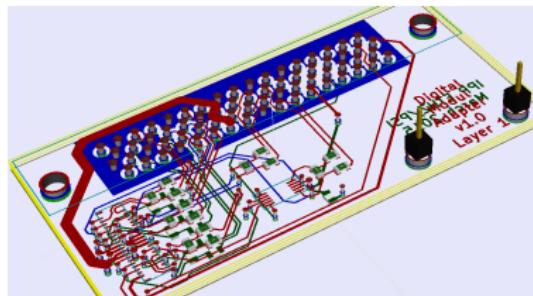
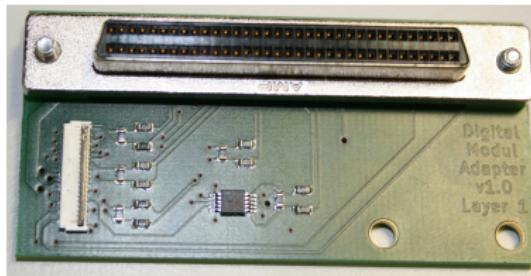
## Schematics



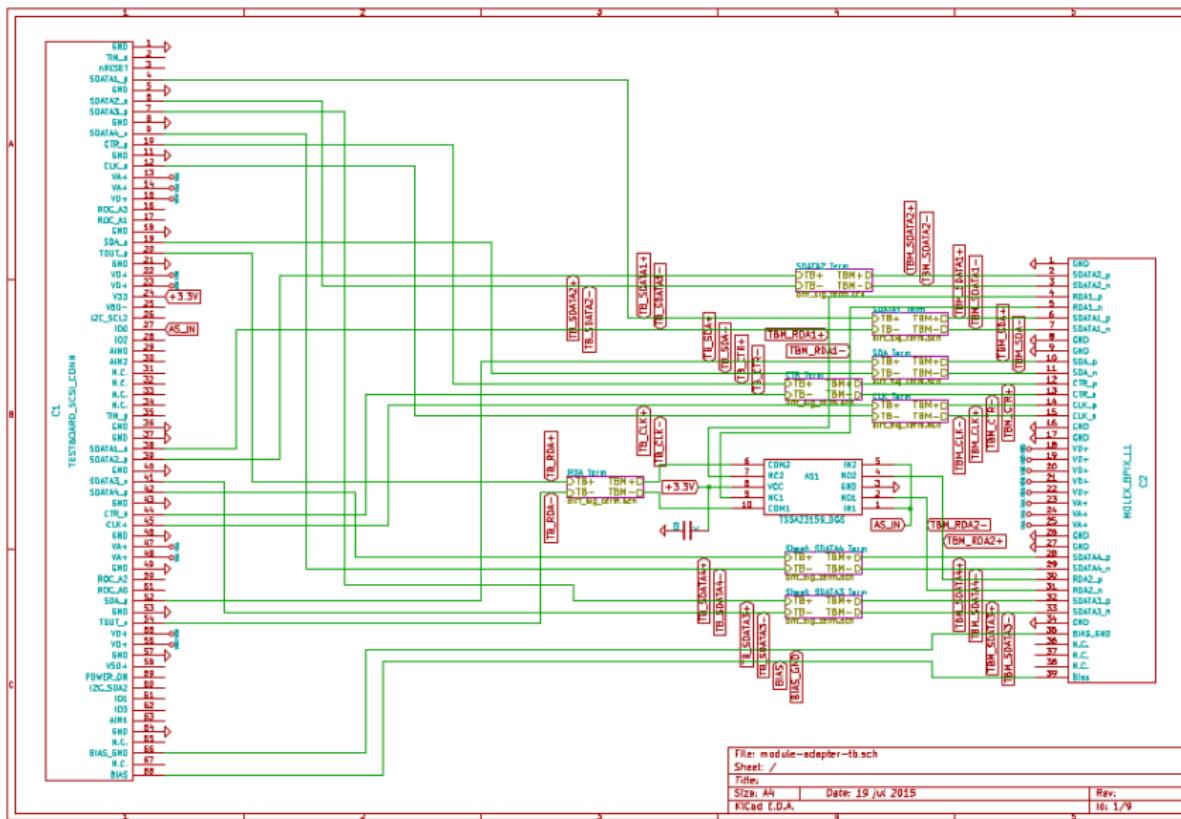


## Digital Module Adapter

- adapter from Molex of the module to the SCSI of the DTB
- old module has a Molex connector for a 33 pin cable
- additional TBM requires additional lines
  - ▶ two pairs of differential SDATA lines
  - ▶ one pair of RDA lines (for TBM feedback)
  - ▶ pin for shielding
  - ▶ one VD+ less
- Molex connector of the Layer1 module has 39 pins
- new adapter design by Martin Lickteig



## Digital Module Adapter



File: module-adapter-th.sch  
Sheet: /  
Title:  
Size: A4 Date: 19 JV 2015  
Kicad EDA Raw:  
16: 1/9

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## Section 3

### Modules for Testing

## Currently available:

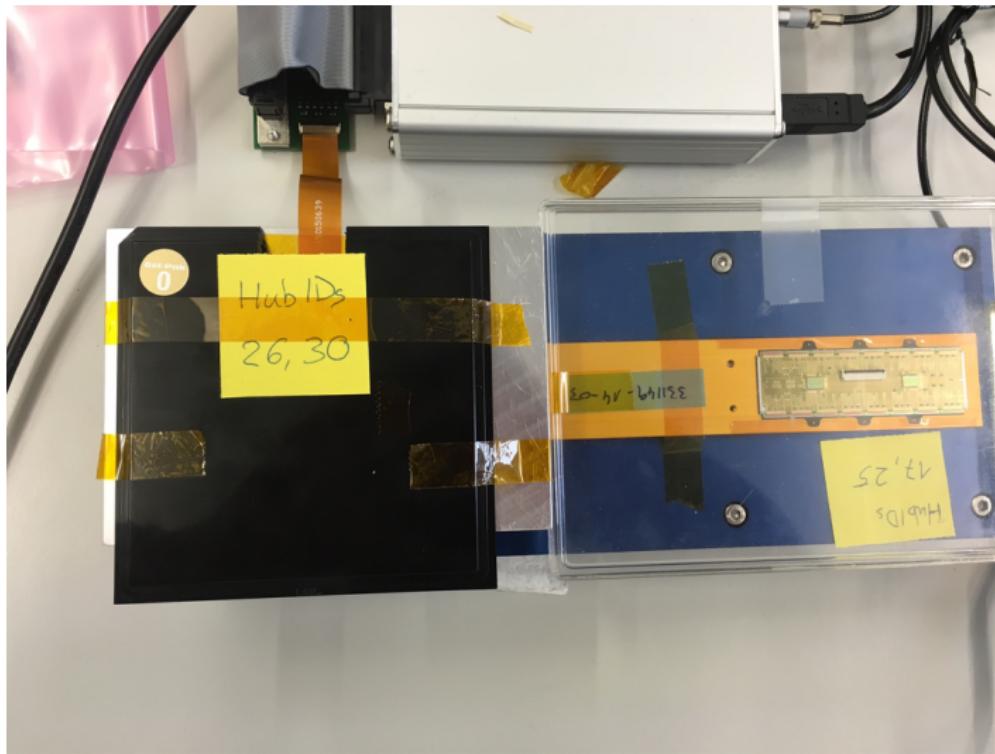
- PSI produced two layer1-like modules based on bare digv2.1respin modules:
  - ▶ one with TBM09 (current Token Bit Manager)
  - ▶ one with the new TBM10 → electrical shortcut
    - ★ sensors cannot be biased

## TMB10:

- TBM10 has additional delay of three clock cycles between trigger and token
  - ▶ required by PROC600

## Plan on further modules:

- fully working module with TBM10 and digv2.1respin (no shortcut)
- module with PROC600 as soon as new chip iteration is produced





## Section 4

### Changes of the DTB

## C++ code accessed by pXar on a virtual processor on the FPGA

### Issues:

- ROC I<sup>2</sup>C addresses remain the same
- HubIDs (hard wired address of the TBM) and PortAddresses change

### Software Additions:

- bool layer1: adding boolean as identifier for the layer1 module
- void roc\_I2cAddr\_Layer\_1(uint8\_t id): sets the correct HubAddress for layer1
- const unsigned char CTestboard::MODCONF L1[16]: stores the port addresses
- void mod\_Addr(uint8\_t hub0, uint8\_t hub1): accessible in pXar, sets the HubIDs

## Verilog FPGA design

### Issue:

- only 3 Deserializer400 implemented
  - ▶ due to former compiling issues

### Changes:

- reactivation of the 4th Deserializer400 to handle the 4 data streams



## Section 5

### Changes in PXAR

## Additional TBM

- `tbmConfig` in pXar almost built up correctly by module parameters in `configParameters.dat` file
  - ▶ `nModules`, `nRocs`, `nTBMs`
  - ▶ rename `tbmConfig` to `tbmCoreConfig`

**Issue:**

- cannot handle more than one HubID

**Solution:**

- changing `unsigned int fHubId` to `vector<uint8_t> fHubIds`
  - ▶ including adaption of: `readHubIds()`, `writeConfigParameterFile()`
- appending HubID with a comma to `hubId` option in config file
- overloading `initDUT()` method to be backwards compatible with old modules
  - ▶ if called with hubID vector of size 2: calls new DTB software function `mod_Addr`
- fixing method `writeTbmParameterFile()` which would write the settings to incorrect filenames 1+ TBMs