Michel Combes (PhD)

Senior Polymathic Engineer

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Work History

SHQL Technologies

chief engineer architect

(2019 - present) | Ecublens, Switzerland

presently launching SHQS, a weareable lab-on-chip project to feed medical research with data personalized, while still preserving security and privacy for the patient.

GC-Bank

distributed ledger architect

(2018 - present) | Ecublens, Switzerland

developed cryptocurrencies and ledger technologies; architect blockRings™ for Data Commons Systems; develop participatory token for collective; launched CERES platform as a transformative economy experiment; issued the first cryptomorphic currency LVC for a Festival in Miami; setup GC-bank portfolio and associated coin forge for minted currencies; developed non-proof of work blockchains; invented smart litigation and proof of witness for solution to double spending, and proof of membership for authentication, developed non-consensus based ledger as byzantine resistant system; developed system robust to Sybil attack for identity management.

2018

Intel Corp.

Lead Electrical Engineer R&D Architect

(2015 - 2018) | Lausanne, Switzerland

developed light weight smart glasses; deploy production validation and characterization flow on manufacture line; build and Reamp up volume for Vaunt smart glasses;

2015

Lemoptix S.A.

Head of Electrical Engineering

(2012 - 2015) | Lausanne, Switzerland

designed MEMs electronic control and drive algorythm. Developed picoprojector, wearable, Head up Displays; architect mems based picoprojector plateform, lead prototyping team; supervise Design and Manufacture of Headup displays, companion projectors and monochrome holographic glasses; lead the Engineeging Team responsible for design of company chipset.

2012

Intersil Inc.

Principal Engineer

(2010 - 2011) | Milpitas, USA

developed laser drivers, reference design, video processor; build reference designs for pico-projector, prepared CES demos (worked with major customers in the field Syndiant, Micron, LGE, MVIS, Bosh, bTendo); defined ARM based video processor architecture for MEMs scanner display systems, geometric correction, mixed signal servoing of laser beams, temperature and power management, white balance contolled loops; published datasheet and supporting documentations for products release; designed drivers for native / direct green lasers (Nishia, Soraa, OSRAM).

2008

Spatial Photonics Inc.

Sr. Electrical Engineering Manager

(2006 - 2008) | Sunnyvale, USA

developed pico-projectors and MEMs displays; developed FPGA demonstration boards for MEMs technology display; assembled bulk DC convertor for high efficiency LED illumination; developed algorithm for pixel rendering in a video system using Pulse Width Modulation (PWM); coded RTL for a dithered gamma correction module; directed LED projector System Architecture team.

2006

Reflectivity Corp.

Principal Electrical Engineer

(2003 - 2006) | Mountain View, USA

developed Image Quality Algorithm for HDTV; developed algorithm for pixel rendering in a video system using Pulse Width Modulation (PWM); implemented flash-based and FSM-based PWM sequencers on Spartan3 board; determined color filter optimization design rules using CIE-1976 space.

Orient Direct Inc.

ASIC Engineer

(2003 - 2003) | Santa Cruz, USA

developed embedded still camera; programmed de-mosaicing and image processing unit design; designed DDR arbiter between graphic CPU, memory and imager; developed video auto-white balance algorithm; oversaw prototype manufacturing for a wrist watch camera.

2002

APT Technologies Inc.

Mixed Signal Design Director

(2001 - 2002) | SantaCruz, USA

developed Serial ATA / High Speed IOs and switches; directed the Analog design Group of APT technologies; architected Out-of-Band Signaling for HDD / IDE interface; managed analog filters amplifiers, voltage references, signal detection and Gibabit SERDES module designs; prototyped Serial-ATA host bus adapter and routers enabling RAID and SCSI low cost solutions; deployed ASIC methodology and provided tools and EDA support to the company; supported Layout design, chip integration, verilog coding, modelsim and SPICE simulations, synplify, leonardo synthesis, place and route, design space exploration and optimization script using AI/CI technology; co-edited Serial ATA early specification and pushed standard.

2001

Infineon Technologies Corp.

System On Chip Integration Manager

(1999 - 2001) | SantaCruz, USA

developed Read/Write Channel, HDD Controller; lead SoC integration team to acheive a "one-chip" disk drive; Defined test plan and validation strategy for HDD Controller; managed IC design team to implement SATA PHY and Transport layers; coded, simulated, and evaluated MAC module for HDD controller.

1999

Texas Instruments Corp.

Digital Design Team Manager - MGTS

(1995 - 1999) | Dallas, USA / Nice, France

Mentored group design activity by establishing methodology and procedures that ensured a high-level quality product using state-of-the-art tools; designed HDD (700MHz) high performance architectures (Viterbi decoder) and fast arithmetic units; took full ownership of DSP+ARM mega-modules electrical design (tremendous success: 220M units); globally promoted an electrical "know-how" throughout his team and other organizations around the world: France, Italy, Japan, Houston, Chicago; defined the design strategy for new wireless product generations by providing specifications, end-user guidelines, tools, flows and trainings; participated in the cost reduction definition process and advanced libraries via technology steering committee.

1994

Bull S.A.

Integrated Circuits Development Engineer

(1990 - 1994) | Les Clayes-sous-Bois, France

Pioneered using Delay Locked Loop (DLL) for clock recovery and full digital PLLs; designed and architected various mixed-signal complex circuits: a 0.5u CMOS prototype for 1.2Gb/s serial link compatible IEEE 1355, a 0.8u packet-switching router 8Gbps, super scalar RISC micro processor, and a delta-sigma audioband analog to digital converter (TMS320AD50); designed key modules: asynchronous FIFOs, registers banks, Digital PLLs, and a 32b VLIW execution unit.

Education History

1994

Pierre & Marie Curie University

Ph.D. , Micro Electronics & Engineering

(1991 - 1994) | Paris, France

Phase and Delay Locked Loop

1991

Electronics Superior Institute of Paris

Master , Computer Engineering

(1989 - 1991) | Paris, France

Professional Skills

- Team Leadership / People Skill — 100%
- System Architect — 100%
- Deep Learning & Big Data — 60%
- Blockchain / Ledger Technologies — 100%
- Software Dev. — 40%
- Hardware Dev. — 80%
- SoC, ASIC, FPGA — 100%

Perl, Python, Verilog, ...