Management and analysis of physics datasets, Part. 1

Nith Laboratory

Antonio Bergnoli bergnoli@pd.infn.it - Filippo Marini filippo.marini@pd.infn.it

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Laboratory Introduction

Goals

- Build the UART transmitter unit
- Build the UART receiver unit

Uart Trasmitter

Transmitter waveform

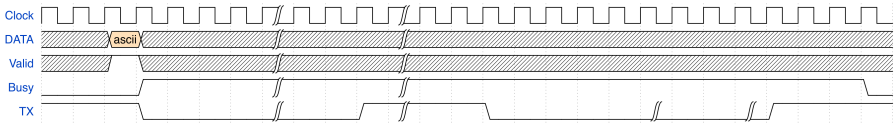


Figure 1: UART transmitter waveform

Baudrate Generator

- it is basically a counter
- it has only one output
- output is equal to '1' for exactly one clock cycle every *bit time (Tbit)*

BOARD clock frequency = 100 Mhz (10 ns period)

BAUDRATE = 115200 (bit/s)

DIVIDER= 100.000.000 / 115200 = 868.055

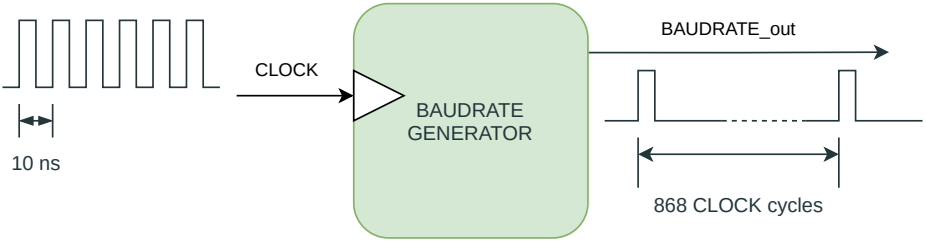


Figure 2: The Baudrate generator

The Uart Transmitter

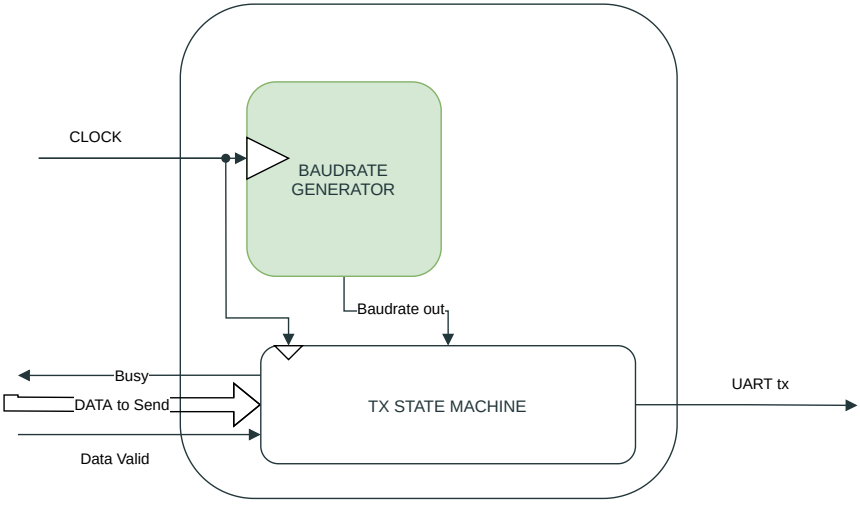


Figure 3: The Uart Transmitter

The Uart Transmitter State machine

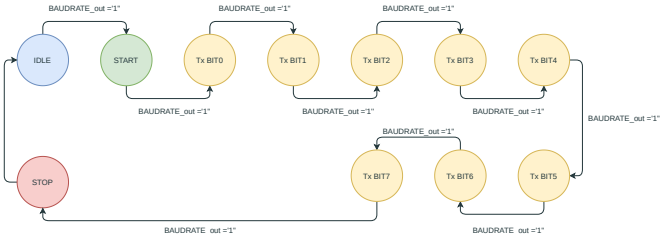


Figure 4: tx State machine idea

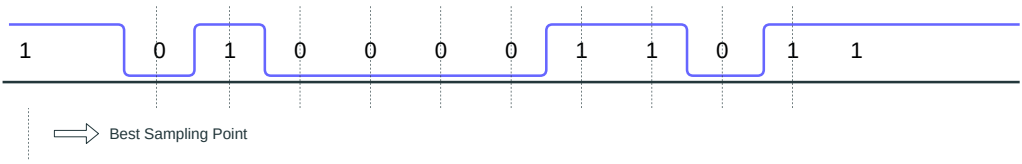
The BAUDRATE out signal make possible to switch from a state to another

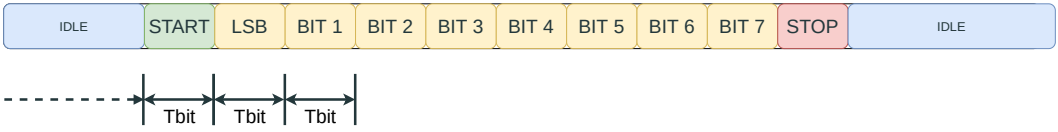
Uart Receiver

How to retrieve the incoming UART transmission?

The bits are recovered by sampling at the best sampling point: the middle of the baudrate period

Transmit Character 'a' (ASCII CODE hexadecimal: 61, binary: 01100001) at 115200 Bit/second, no parity bit



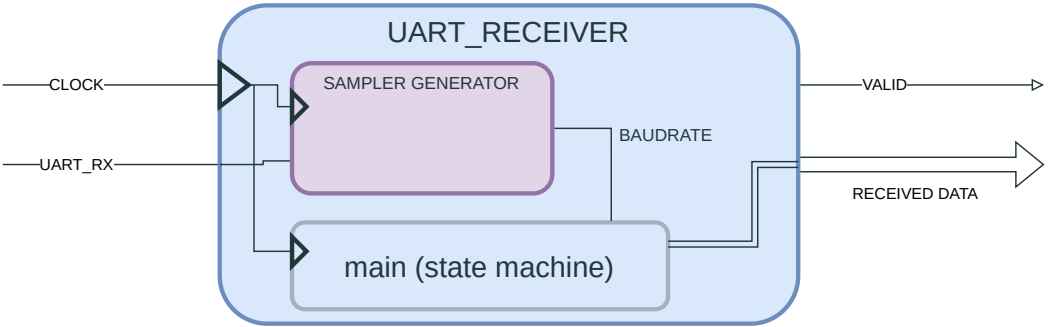


Tbit=1/115200 s = 8,68 us

Modules for the Uart receiver

The UART receiver consists of two main modules:

- The sampler generator
- the main state machine module



The Sampler Generator

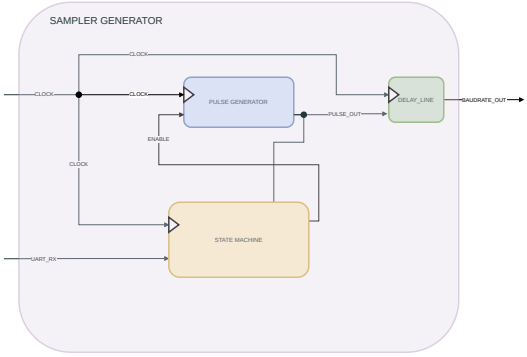
The Sampler Generator module is needed to provide the main UART receiver module with the data sampling pulses.

Like the trasmitter needed the Baudrate generator to transmit the UART bits, now the pulse generator dœs the same thing, but the pulses are now needed to sample the incoming bits.

The Sampler Generator

Just like the UART transmitter main module, the sampler generator is made up of 3 different submodules:

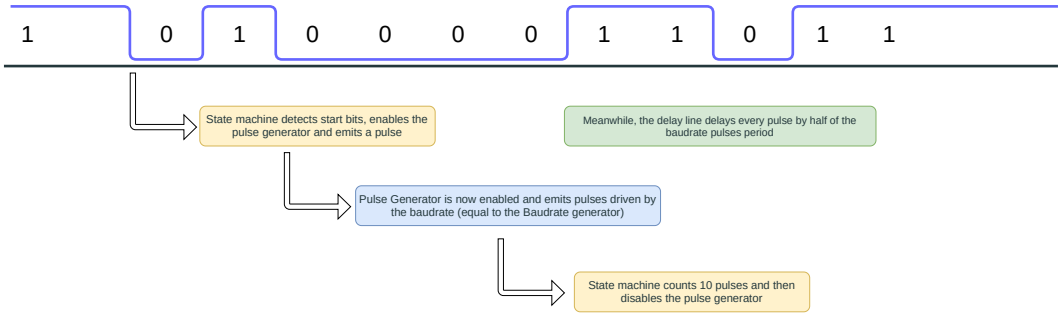
- The pulse generator
- The state machine
- the delay line



What does the Sampler Generator do?

The behaviour of the sampler generator is the following:

Transmit Character 'a' (ASCII CODE hexadecimal: 61, binary: 01100001) at 115200 Bit/second, no parity bit



Homework

- Design the Sampler Generator module and simulate it
- Design the UART Receiver module and simulate it