Management and analysis of physics datasets, Part. 1

Seventh Laboratory

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Laboratory Introduction

Goals

- Example design for the Arty7 FPGA Board
- Build the UART Transmit Unit

Example design for the Arty7

Using the LEDs

The Arty7 board presents several LEDs, buttons and switches. How to use them?

We can create a simple design implementing a counter

- 1 button resets the counter
- 1 button starts the counter
- 1 button stops the counter
- 4 LEDs act as a 4-bit counter

Implementing the counter

- The firmware consists of a 2-states state machine (**idle** and **start**).

```
type t_state is (st0_idle,
                 st1_start
                 );

signal s_state   : t_state;
```

```
p_fsm : process (clk_i, rst_i) is
begin  -- process p_fsm
  if rst_i = '1' then                   -- asynchronous reset (active high)
    s_state <= st0_idle;
  elsif rising_edge(clk_i) then         -- rising clock edge
    case s_state is
      --
      when st0_idle =>
        s_go <= '0';
        if start_i = '1' then
          s_state <= st1_start;
        end if;
      --
      when st1_start =>
        s_go <= '1';
        if stop_i = '1' then
          s_state <= st0_idle;
        end if;
      --
      when others =>
        null;
    --
    end case;
  end if;
end process p_fsm;
```

The counter process

- The counter is driven by the “s_go” signal (besides the reset signal)

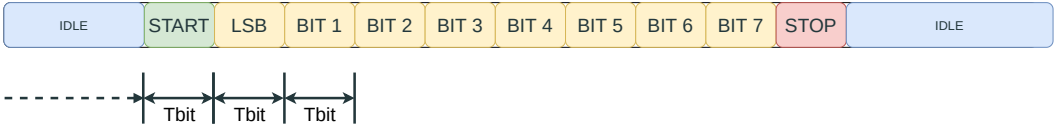
```
p_counter : process (clk_i, rst_i) is
begin  -- process p_counter
  if rst_i = '1' then                  -- asynchronous reset (active high)
    u_counter <= (others => '0');
  elsif rising_edge(clk_i) then        -- rising clock edge
    if s_go = '1' then
      u_counter <= u_counter + 1;
    end if;
  end if;
end process p_counter;

s_counter <= std_logic_vector(u_counter);
```

UART

The RS-232 Data frame: an example

- **Byte oriented frame**
- Mostly used to exchange *character stream* (ASCII code, see next slide) but also binary stream
- optional parity bit at the end of the trasmitted byte
- **start** and **stop** frame delimiter length = 1 bit (stop-bit could be 2 in some cases)

Transmit Character 'a' (ASCII CODE hexadecimal: 61, binary: 01100001) at 115200 Bit/second, no parity bit



Tbit=1/115200 s = 8,68 us

The Baudrate generator

- it is basically a counter
- it has only one output
- output is equal to '1' for exactly one clock cycle every *bit time (Tbit)*

Motivation

We need a periodic signal (another clock) at the rate of the transmission

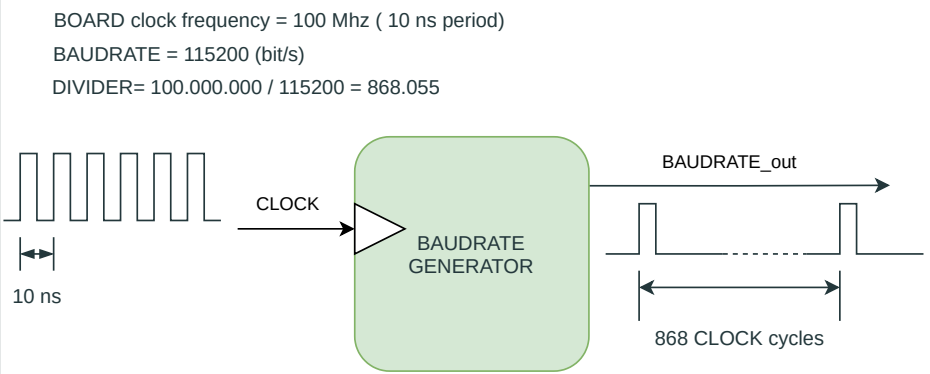


Figure 2: The Baudrate generator

Baudrate Generator Excercise

Write a Baudrate generator in VHDL, in the case of:

- Clock frequency= 100 Mhz
- Baudrate = 115200

Please ask if you're stuck!

The Uart Transmitter

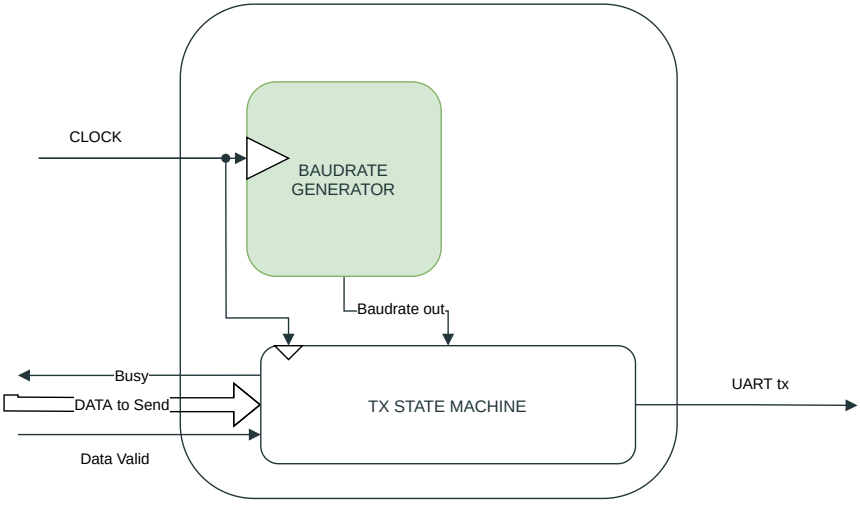


Figure 3: The Uart Transmitter

The Uart Transmitter State machine

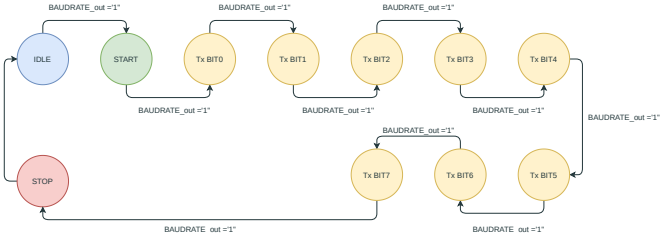


Figure 4: tx State machine idea

The BAUDRATE out signal make possible to switch from a state to another

Transmitter waveform

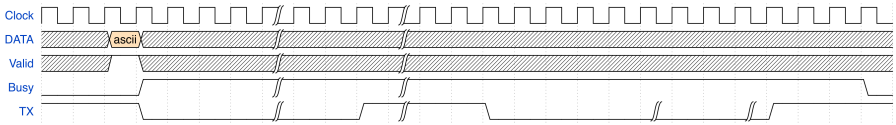


Figure 5: UART transmitter waveform

UART Transmitter Excercise

- Build a complete Uart transmitter working at data rate of 115200 baud

Please ask if you're stuck!