1. What are the **equations** to retrieve the sum (**Σ**) and the carry output ($\mathbf{C_{out}}$) of a full adder?

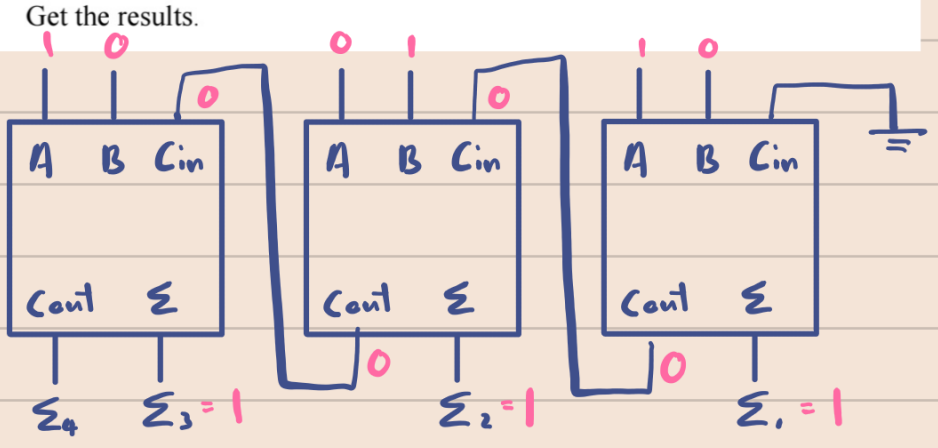
$\Sigma = (A \oplus B) \oplus C_{in}$

$C_{out} = AB + (A+B)C_{in}$

2. How **many full adders** are needed to complete these additions?
   a. 101 and 010 3
   b. 1100 and 0101 4
   c. 111 and 001 3
   d. 1010 and 1101 4
   e. 010 and 011 3
   f. 11001 and 10101 5

3. For Question ~~3~~ 2 (Show your workings): 101 + 010
   a. Draw the block diagram of parallel adders for Question 3
   b. Get *every instance* of sum (**Σ**) and carry output ($\mathbf{C_{out}}$) for each full adder.
   c. Get the results.

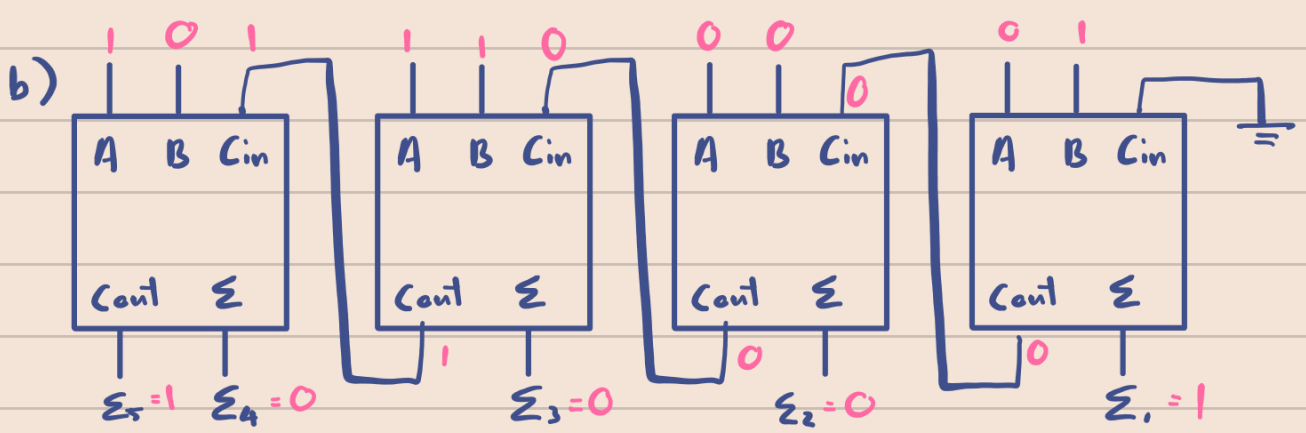
a)



101
+010
111

Σ = 111

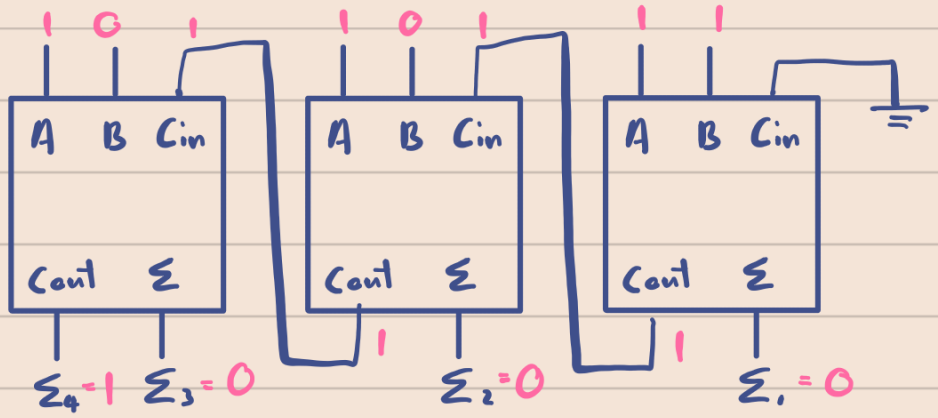
b)



1100
+0101
10001

Σ = 10001

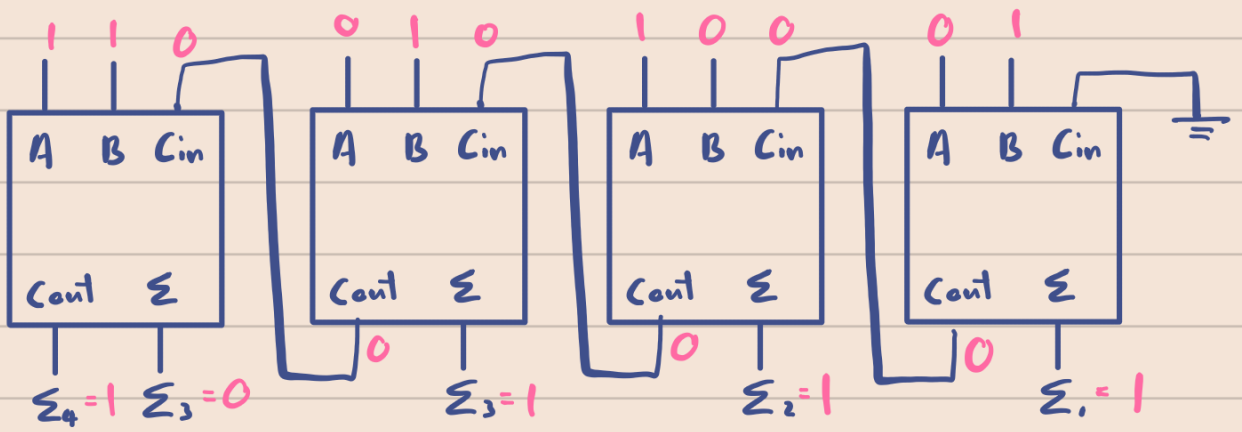
c)



$$\begin{array}{r} {}^{1}{}^{1}{}^{1}\,1 \\ +\,0\,0\,1 \\ \hline 1\,0\,0\,0 \end{array}$$

Σ = 1000

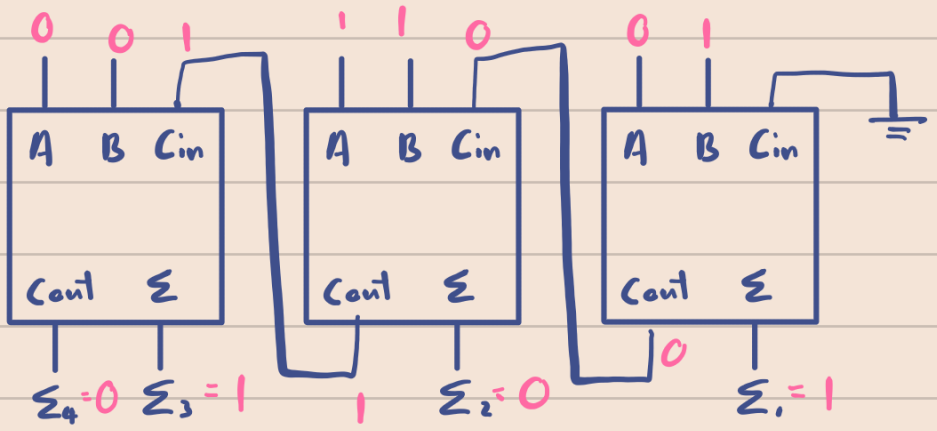
d)



$$\begin{array}{r} 1\,0\,1\,0 \\ +\,1\,1\,0\,1 \\ \hline 1\,0\,1\,1\,1 \end{array}$$

Σ = 10111

e)

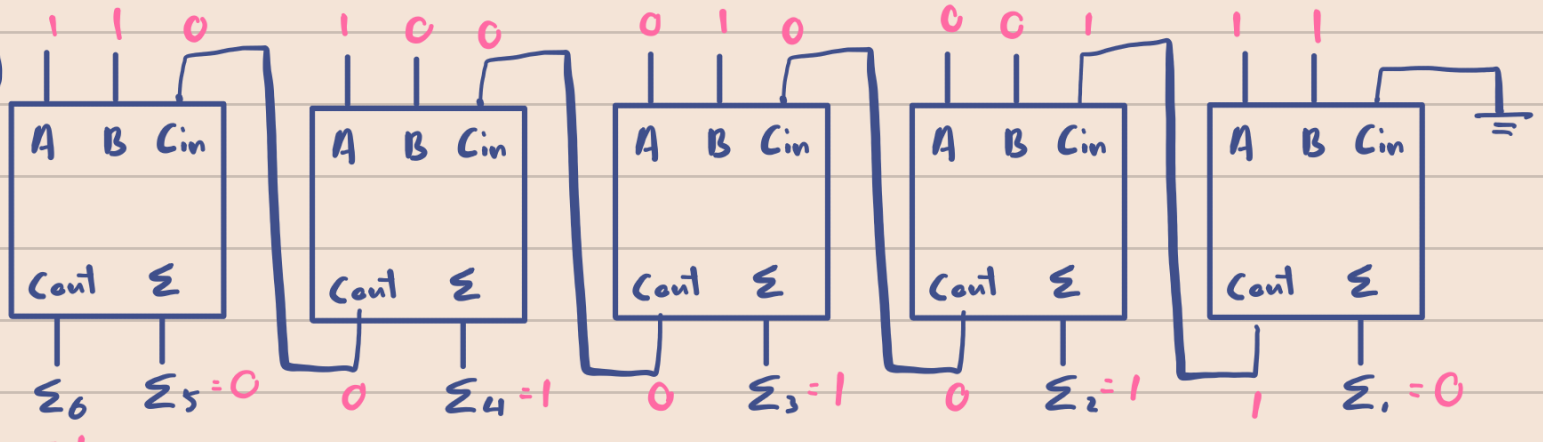


$$\begin{array}{r} {}^{1}\,0\,1\,0 \\ +\,0\,1\,1 \\ \hline 1\,0\,1 \end{array}$$

Σ = 101

$$\begin{array}{r} {}^{1}{}^{1}\,1\,0\,0\,{}^{1}1 \\ +\,1\,0\,1\,0\,1 \\ \hline 1\,0\,1\,1\,1\,0 \end{array}$$

f)



Σ = 101110

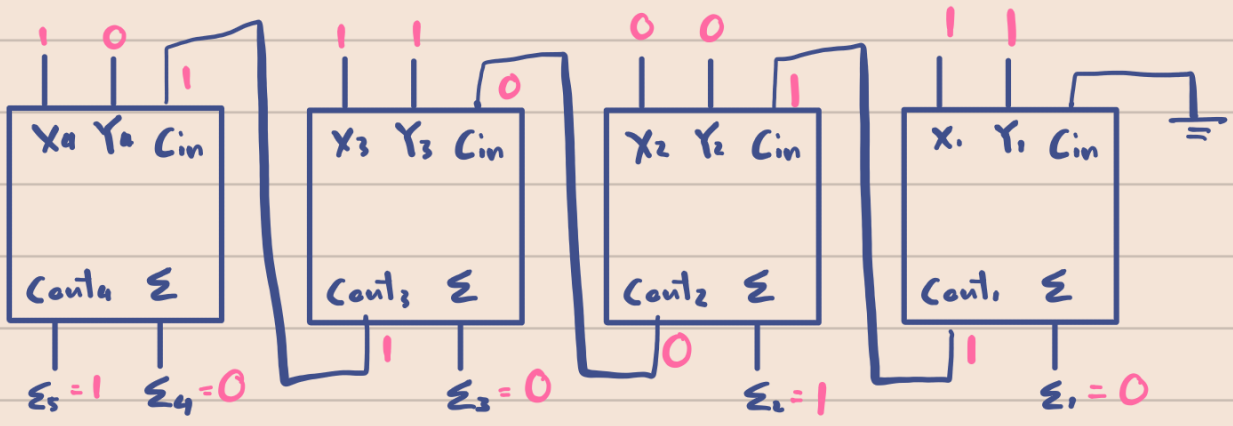
4. Use the parallel adder truth table (Table 1) to find the sum and output carry for the addition of the following two 4 bit number if the input carry (C_{n-1}) is 0. Show the diagram.

$X_4X_3X_2X_1 = 1101$ $Y_4Y_3Y_2Y_1 = 0101$

Table 1

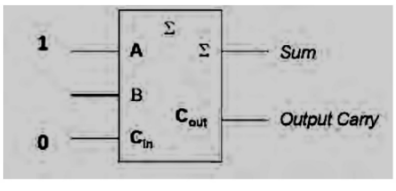
X_n	Y_n	C_{n-1}	C_n	$\sum_n$
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

1101
+0101
10010



Σ = 10010

5. Determine the outputs of **Sum** and **Output Carry** for the inputs given for Full Adder as shown below.



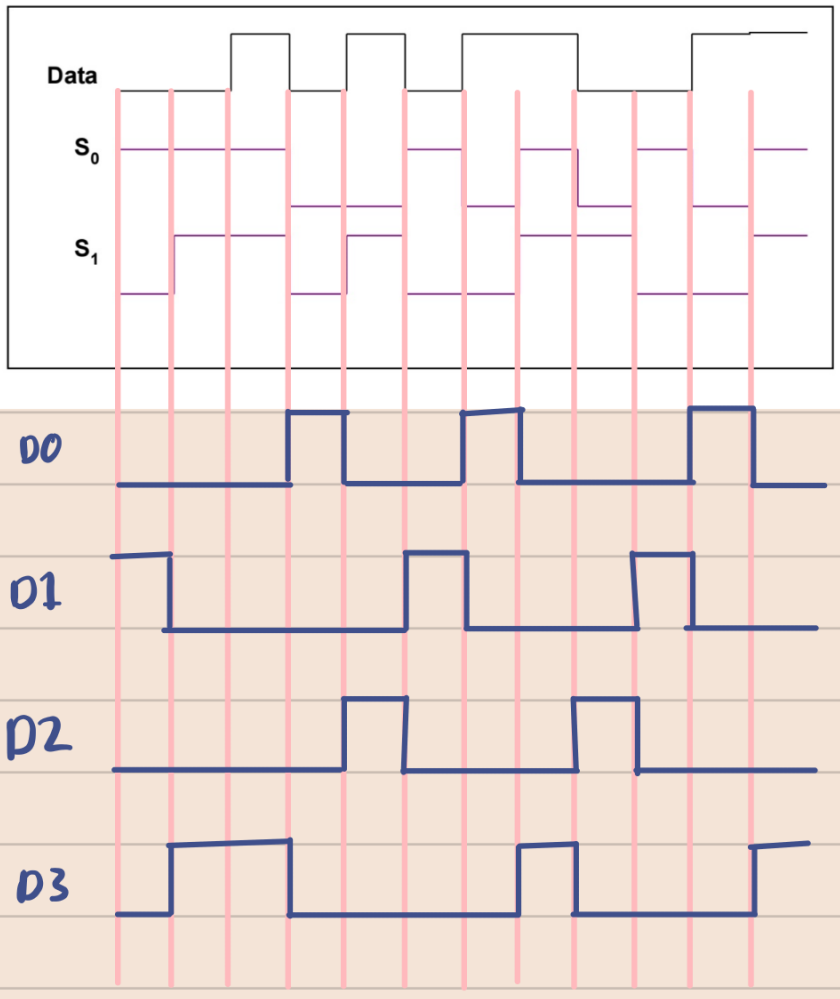
If B = 0	If B = 1
Σ = 1	Σ = 0
Cout = 0	Cout = 1

7. Convert the following:
   a. 98 in BCD to binary
   b. 01110101 in BCD to binary

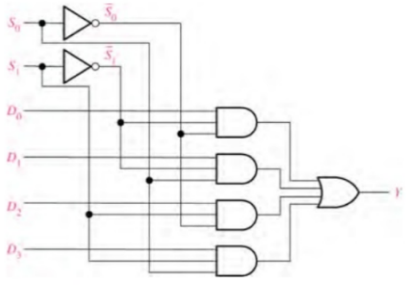
a) 98 = 1001 1000 = 01100010

b) 0111 0101 = 75 = 01001011

8. A DEMUX has 4 outputs D0, D1, D2 and D3. Given the information below, draw the appropriate waveforms for the outputs.



9. a) What type of multiplexer shown in a figure below.
   b) Develop the truth table for multiplexer in figure below.



a) 1×4 multiplexer

10. What is the difference between **decoder** and **multiplexer**.

Decoder - detect the presence of a specified combination of bits on its input

Multiplexer - allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.

12. Using a full-adder, determine the logic state (1 or 0) at each gate output for the following inputs:
    (a) $A = 1, B = 1, C_{in} = 1$
    (b) $A = 0, B = 1, C_{in} = 1$
    (c) $A = 0, B = 1, C_{in} = 0$

a) $\Sigma = 1$, $C_{out} = 1$

$\Sigma = 0$, $C_{out} = 1$

$\Sigma = 1$, $C_{out} = 0$

13. What the full-adder inputs that will produce each of the following outputs:
    (a) $\Sigma = 0, C_{out} = 0$
    (b) $\Sigma = 1, C_{out} = 0$
    (c) $\Sigma = 1, C_{out} = 1$
    (d) $\Sigma = 0, C_{out} = 1$

a) $A = 0$, $B = 0$, $C_{in} = 0$

b) $A = 1$, $B = 0$, $C_{in} = 0$

c) $A = 1$, $B = 1$, $C_{in} = 1$

d) $A = 1$, $B = 1$, $C_{in} = 0$

14. Determine the outputs of a full-adder for each of the following inputs:
    (a) $A = 1, B = 0, C_{in} = 0$
    (b) $A = 0, B = 0, C_{in} = 0$
    (c) $A = 0, B = 1, C_{in} = 1$
    (d) $A = 1, B = 1, C_{in} = 1$

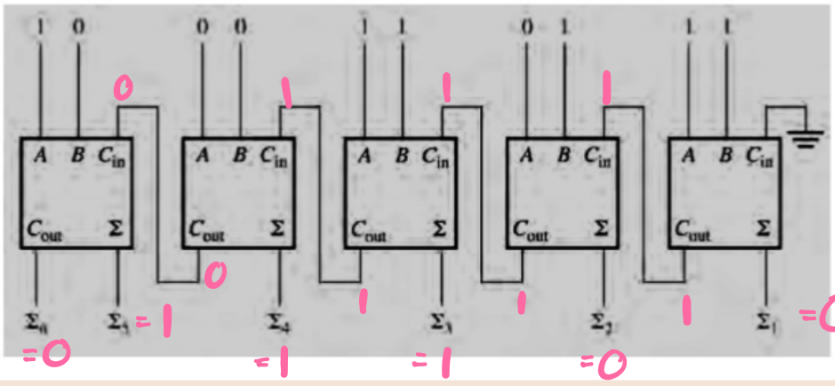
a) $\Sigma = 1$, $C_{out} = 0$

b) $\Sigma = 0$, $C_{out} = 0$

c) $\Sigma = 0$, $C_{out} = 1$

d) $\Sigma = 1$, $C_{out} = 1$

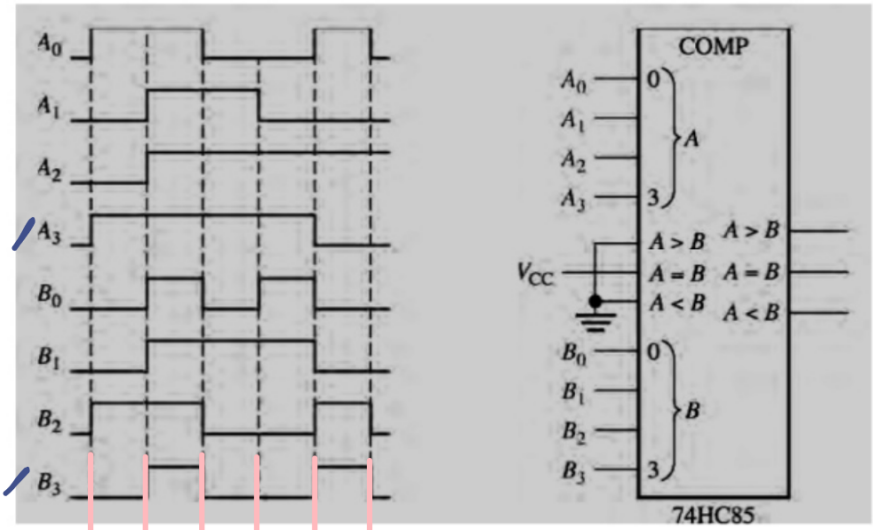
15. For the parallel-adder, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.

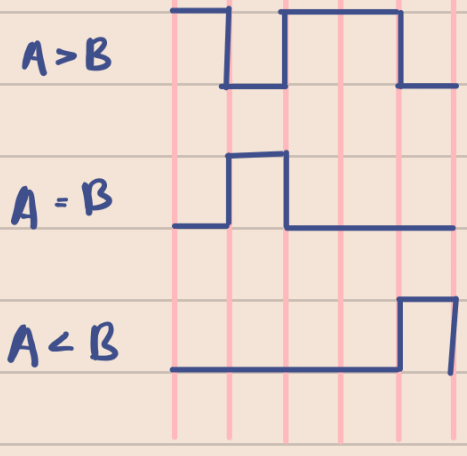


$$\begin{array}{r} 10101 \\ +\ 00111 \\ \hline 11100 \end{array}$$

$\Sigma = 11100$

16. For the 4-bit comparator, plot each output waveform for the inputs shown. The outputs are active-HIGH.





17. Show the decoding logic for each of the following codes if an active-HIGH (1) output is required:

(a) 1101 $A\bar{B}CD$
(b) 1000 $A\bar{B}\bar{C}\bar{D}$
(c) 11011 $AB\bar{C}DE$
(d) 11100 $ABC\bar{D}\bar{E}$
(e) 101010 $A\bar{B}C\bar{D}E\bar{F}$
(f) 111110 $ABCDE\bar{F}$
(g) 000101 $\bar{A}\bar{B}\bar{C}D\bar{E}F$
(h) 1110110 $ABC\bar{D}EF\bar{G}$

18. For the decimal-to-BCD encoder logic, assume that the 9 input and the 3 input are both HIGH. What is the output code? Is it a valid BCD code?

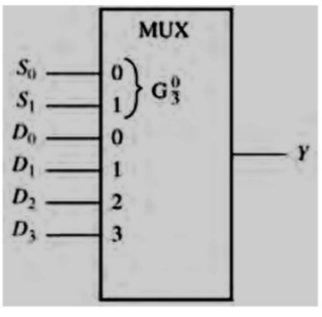
1001 0011

1001 0011. valid because they are between 0-9.

19. Convert the following decimal numbers to BCD and then to binary.

(a) $2 = 0010 = 0010_2$
(b) $8 = 1000 = 1000_2$
(c) $13 = 0001\ 0011 = 1101_2$
(d) $26 = 0010\ 0110 = 11010_2$
(e) $33 = 0011\ 0011 = 100011_2$

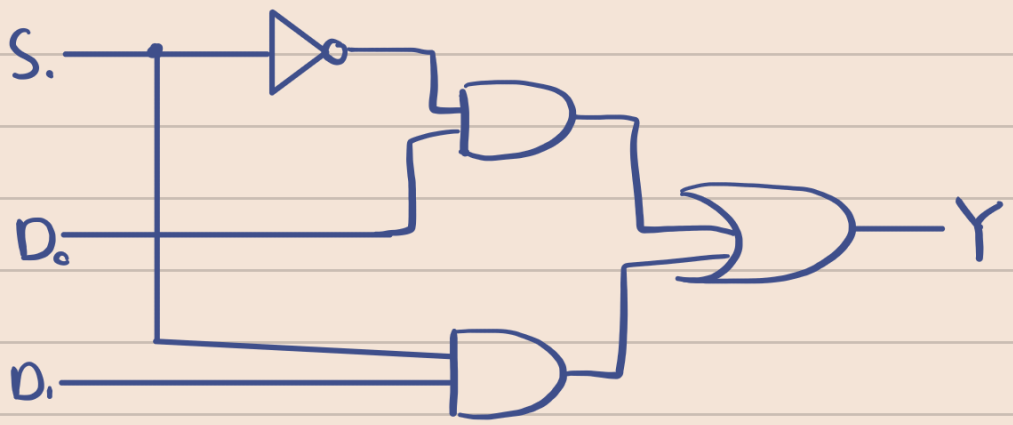
20. For the multiplexer given, determine the output for the following input states: $D_0 = 0$, $D_1 = 1$, $D_2 = 1$, $D_3 = 0$, $S_0 = 1$, $S_1 = 0$.



Y = 1

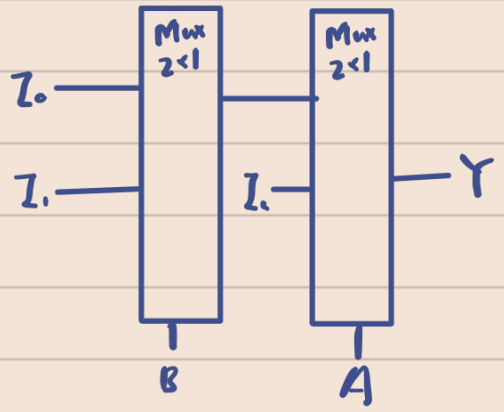
21. Draw a logic circuit for 2-to-1 multiplexer (MUX) using gates.

S_0	Y
0	D_0
1	D_1

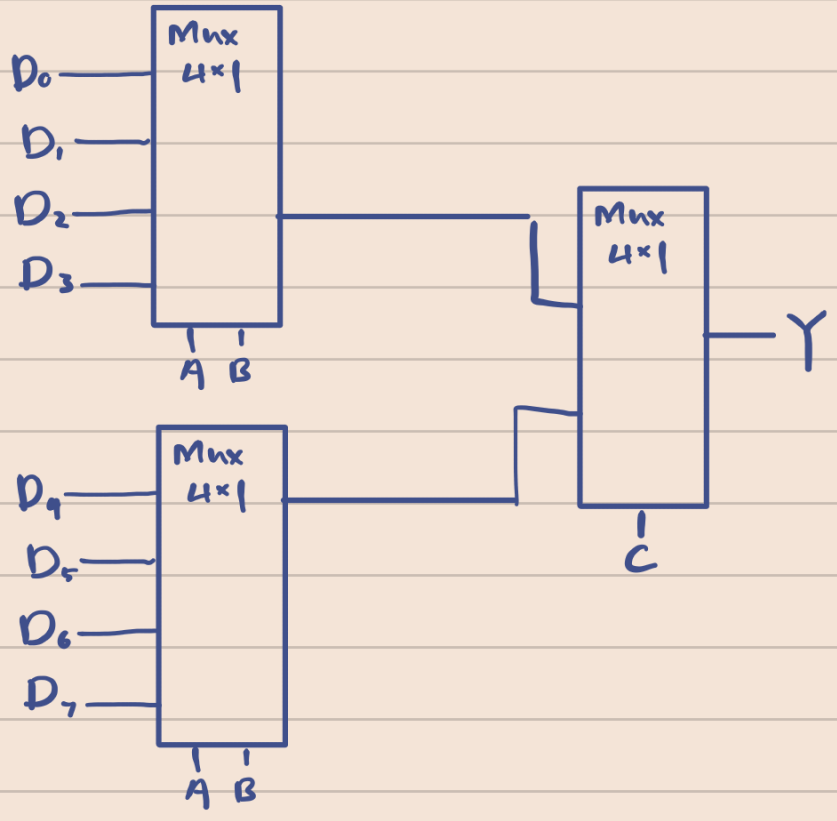


22. (a) Show how two 2-to-1 MUX (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows:
If $AB = 00$, select I_0
If $AB = 00$, select I_1
If $AB = 1$ – (B is a don't care), select I_2

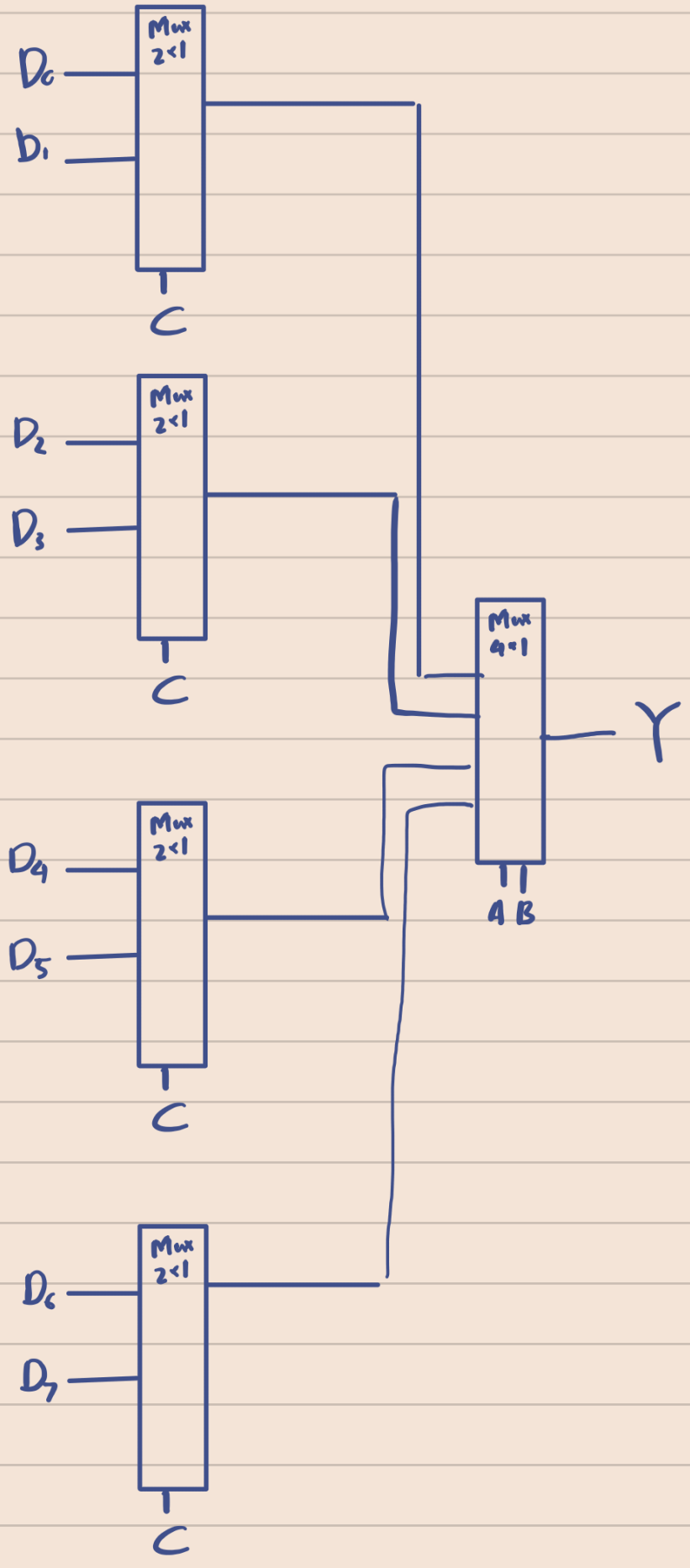
A	B	I_0	I_1	I_2
0	0	1	x	x
0	1	x	1	x
1	0	x	x	1
1	1	x	x	1



(b) Show how two 4-to-1 and one 2-to-1 MUX could be connected to form an 8-to-1 MUX with three control inputs.



(c) Show how four 2-to-1 and one 4-to-1 MUX could be connected to form an 8-to-1 MUX with three control inputs.



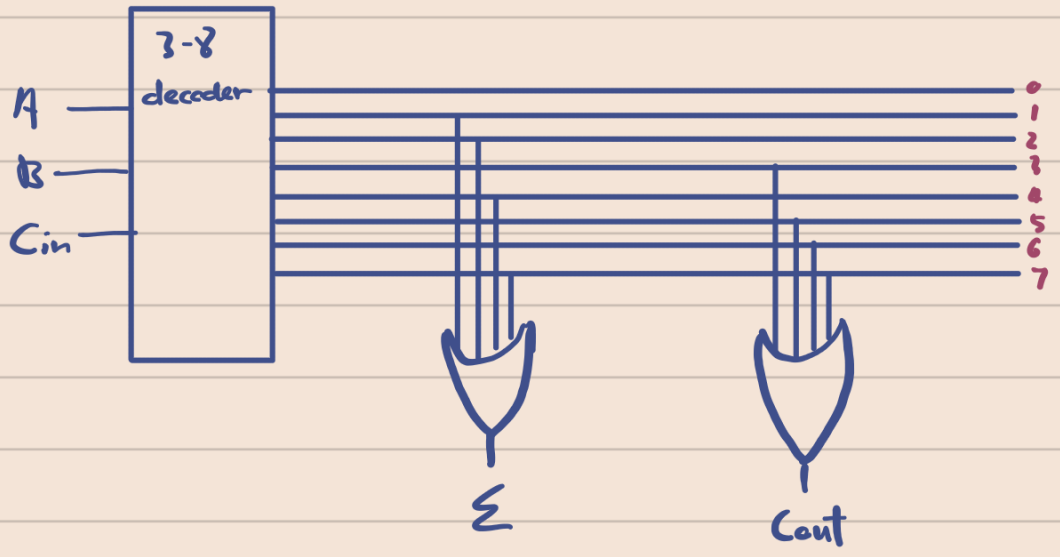
24. Realize a full adder using 3-to-8 line decoder and

(a) two OR gates
(b) two NOR gates

0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Σ Cout

a)



b)