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A comparative study based on optical and electrical performance of micro- and nano-textured surfaces for silicon solar cells

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ABSTRACT

In this contribution, we report on the optical and electrical properties of textured silicon surfaces usually incorporated in solar cell fabrication. In order to study the influence of different texturisation processes, nano-texturing was accomplished by soft UV-NIL process while the micro-textured surfaces were prepared using TMAH solution. The nano-textured surfaces were found to be superior in terms of optical performance but the passivation of these structures was solely limited by the fabrication process itself. Any defect or damage caused during the pattern transfer (plasma etch) process acts as a recombination centre which significantly reduces carrier lifetime. By systematically removing the plasma induced damage from the surface, it was possible to improve the effective lifetime from 24.4 μs to 1092 μs. We report that, despite of the enlarged surface area compared to micro-textured surface, our nano-texture surface possess excellent optical properties and higher lifetime.

1. Introduction

"State-of-the-art" solar cells based on crystalline silicon bulk material feature randomly textured front surface coated with thin SiNx anti-reflection coating (ARC) for an efficient reduction of reflection. However, for better exploitation of solar spectrum there has been a considerable interest to include light trapping structures in the solar cell design which gave rise to highly innovative ways of forming nano-textured surfaces using femtosecond laser pulses [1], black silicon formation [2] or by nano-imprinted layers [3,4] due to their excellent broadband anti-reflection properties. The cost effective UV-Nanoimprint Lithography (UV-NIL) process have been extensively used for the formation of anti-reflective nano-textured surfaces, whose detailed fabrication sequence is summarised in [3]. Yet, the crucial electronic properties of these types of nano-scaled structures are a major drawback which will only be overcome by an effective passivation of the enlarged surface area. Therefore, integration of such anti-reflective textures in commercial solar cells fabrication so far, has been delayed.

In the literature, typically polished or micro-textured surfaces passivated using plasma enhanced chemical vapour deposited silicon nitride (PECVD SiN_x) or thermally grown silicon dioxide (SiO_2) layers have been studied. We investigated the passivation of nano-scaled structures and compared them with micro-textured and polished surfaces. Herein, we report on the passivation properties of thermally grown SiO_2 layer, which is well known to exhibit excellent surface passivation on both n- and p-doped Si surfaces.

2. Experimental method

In order to study the influence of different texturisation processes on optical and electrical properties, nano-texturing was accomplished by a UV-NIL process (see Fig. 1). A HBr-based reactive ion etching (RIE) process was applied to obtain the tailored silicon nano-conical array suitable for anti-reflection textures (see Fig. 2a). The height of the fabricated silicon nano conical-array was determined to about 1.18 μm, resulting in a pattern aspect ratio of about 2.0. The process induced effects were compared to micro-textured surfaces prepared using mixture of alkaline etching solution Tetramethylammonium hydroxide (TMAH) and Iso-propyl alcohol (IPA) (see Fig. 2b) forming random pyramids on both wafer sides in the range of 3–10 μm. The surface morphology produced after the texture process was analysed by SEM and the optical properties were studied using spectral reflectivity measurements at a normal incidence. A LAMBDA™ 950 spectrophotometer with an integrating sphere of 150 mm is used to measure overall transmittance and specular reflectance over a range of 200–1200 nm. Additionally, the passivation quality of the textured silicon surfaces with thermally oxidised thin SiO_2 layer was evaluated by measuring minority carrier lifetimes using contactless photo conductance measurement technique [5]. As a reference un-patterned and polished wafers of the same material were used.

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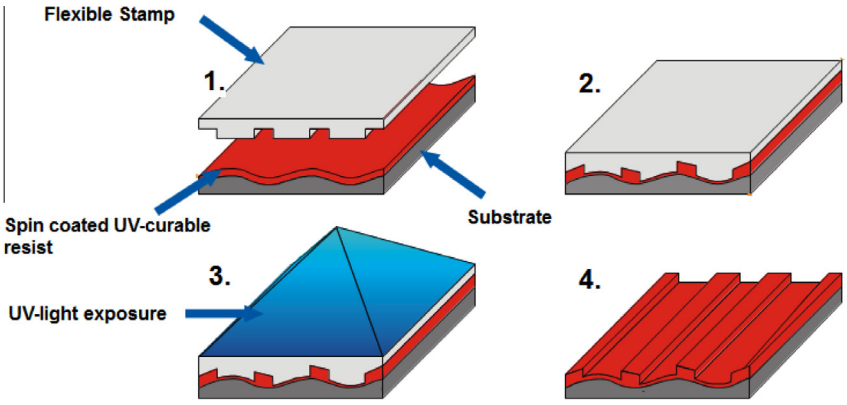
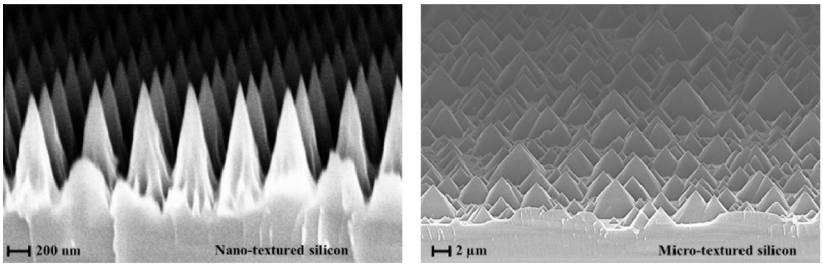


Fig. 1. Soft UV-NiL imprint sequence. (1) Spin coating of UV-curable resist on substrate. (2) Adaptation of stamp to waviness of substrate. (3) UV-exposure and curing of resist. (4) Detachment of the stamp.



(a) Nano-textured surface fabricated using soft UV-NIL process. Magnification X 30k.

(b) Micro-textured surface formation in mixture of TMAH and IPA solution. Magnification X 2.5k

Fig. 2. Surface topography of the nano- and micro-textured surface. Periodic nano-structures feature 118 µm height with the period of about 490 nm while the randomly micro-textured surface has height and width ranging between 3 and 10 µm.

The substrates used in this study are 4″, 520 µm-thick, p-type, ⟨100⟩ oriented, both side polished FZ silicon wafers having resistivity about 10,000 Ωcm. This high-quality intrinsic material with doping level of $1.328 \times 10^{12}\,cm^{-3}$ ensures that the measured effective lifetime (τ_{eff}) is not limited by bulk defects. All samples have been cleaned by a standard 3-step clean and rinse, consisting of self-heating piranha solution (10 min, H_2SO_4:H_2O_2 1:1) followed by RCA1 clean (10 min, H_2O:H_2O_2:NH_4OH 7:2:1) and diluted HF treatment (2 min, HF:H_2O 1:20) to remove native oxide at the surface right before the passivation. Lifetime samples (except nano-textured samples) were identically structured, cleaned and passivated on both sides. Unlike, the alkaline texture process which leaves the micro-pyramids on both wafer surface; it is very difficult to get the identical nano-textured surface on both wafer sides using our process and hence the nano-textured lifetime samples has been given an asymmetric structure Nevertheless, a very high quality passivation was brought on both wafer sides, so that the lifetime in this sample will be solely dominated by the textured surface itself. All samples were passivated together at 1050 °C by a thin thermally grown SiO_2 layer (30 nm) and treated by a post deposition annealing for 30 min in mixture of forming gas (N_2 + 10% H_2) at 400 °C.

3. Results and discussion

3.1. Optical characterisation

To quantify the benefits arising from the textured surfaces, the wavelength dependent reflection $R(\lambda)$ is weighted with the solar spectrum from 300 nm to 1200 nm. The weighted reflectance (R_W) can be calculated via [4]

$$R_w = \frac{\int_{\lambda 1}^{\lambda 2} S(\lambda) R(\lambda) \frac{\lambda}{hc} d\lambda}{\int_{\lambda 1}^{\lambda 2} S(\lambda) \frac{\lambda}{hc} d\lambda}$$

where $S(\lambda)$ is the AM1.5 g spectrum. The integration boundaries mark roughly for the silicon solar cells usable part of the solar spectrum.

The soft UV-NIL replication process followed by a pattern transfer into silicon using RIE forms nano-scaled needle like structures that turn silicon surface completely into an effective medium with a gradually increasing refractive index. This leads to the low reflectivity (R_W = 2.26 %) and black appearance of our samples. The overview of hemispherical total reflection measured on studied surfaces is illustrated in Fig. 3.

The micro-textured surface leads to R_W of 14.61% and the unpatterned silicon substrate without ARC is about 34.79% both quite above the reflectance measured from the nano-structured wafer in the entire wavelength range between 300–1200 nm (refer Fig. 3). The increase in reflectance above 1000 nm spectral region corresponds to the light reflected from the rear surface, and transmitted back through the front textured surface due to drastic reduction in absorption coefficient of silicon at longer wavelengths. It has to be noted, however, that the optical performance of the nano-textured surface adapted in this work is still much better than the one from micro-textured samples coated with standard SiN_x ARC ($R_W \sim 3.98\%$) typically used in solar cell fabrication. The nano-structure is indeed an effective gradual ARC thanks to its sub-wavelength dimensions. For this reason it can reach and overcome the micro-structure coated with a monolayer ARC.

3.2. Electrical characterisation

Despite widespread applicability, silicon surfaces exposed to plasma processes suffers from surface damage. The nature and severity of this damage is a complex function of many plasma

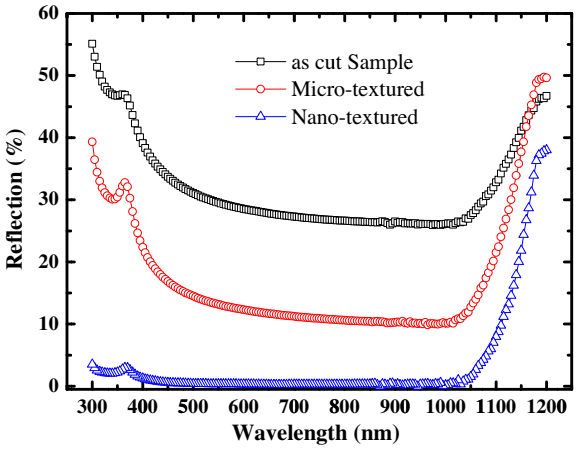


Fig. 3. Overview of hemispherical total reflectance measured on micro-, nano-textured and reference wafers. Nano-texture surface possesses excellent anti-reflective properties over a wide wavelength range.

parameters including the chemistry of plasma gases, RF power, temperature, and pressure [6]. According to Schaefer et.al. [7], the Si surfaces exposed to plasma etching consist of a top thin (5 nm) layer entirely covered of plasma residuals. The layer underneath extending to 10–20 nm consists of heavily damaged Si lattice. The damage caused by RIE processes effectively degrades electrical performance of semiconductor [8] and photovoltaic (PV) devices [9]. Therefore, it was of utmost importance to remove the plasma induced damage from the nano-textured surface.

3.2.1. Damage removal etching

In PV devices, on the one hand, it is necessary to have the surface textured to reduce optical losses but on the other hand textured surfaces usually contains a large numbers of dangling bonds which must be passivated for obtaining high solar cell efficiencies. Therefore, it is essential to inhibit the introduction of any kind of damage during texture formation, which can lower the minority carrier lifetime. In the past, various surface treatments including RTA annealing [10], thermal oxidation and wet-chemical etching [8], and anodic oxidation [7] aimed at the recovery of damage-free Si surfaces have been investigated. Due to controlled etch rates in silicon, acidic mixture of $HF–HNO_3–H_2O$ solution have been used for damage removal etching (DRE) performed in our work.

In the absence of excessive surface damage, such passivation layer reduces surface recombination to the extent that the resulting τ_{eff} (4183 μs) is often dominated by the bulk lifetime (τ_{bulk}) of a sample. This is reflected by the lifetime measurements on the FZ polished samples (see Table. 1). It is found that significant surface damage has been introduced after the pattern transfer step using RIE process and the measured τ_{eff} (24.4 μs in absence of DRE) have been reduced accordingly. After the RIE process, samples were treated by dipping in DRE solution for a period between 40 and 240 s at room temperature to remove the damaged layer. We will refer it DRE sequence 1 as the DRE step was introduced after all cleaning steps on the plasma etched surface have been performed. The τ_{eff} of the sample after 120 s DRE measures 120.8 μs, compared with 24.4 μs for the RIE etched sample without DRE step. It is important to note that, even after 120 s DRE step the R_W was still low enough (4.28%) indicating no harmful effect on nano-textured surface. The negative influence both on R_W and τ_{eff} could be only observed after 120 s DRE which might have caused due to over etching of the patterned surface leading to surface defects, the sites which act as an active recombination centers.

We performed another variation in DRE process which is stated as DRE sequence 2. In this case, we applied DRE step right after the plasma treatment and all other cleaning steps were performed later.

Table 1
Influence of DRE on the weighted reflection (R_W) and effective carrier lifetime (τ_{eff}) of nano-textured surface. All τ_{eff} values were measured on samples covered with 30 nm thick SiO_2 layer at an excess carrier density of 1×10^{15} cm^{-3}.

Surface type	DRE (s)	DRE sequence	τ_{eff} (μs)	R_w (%)
Polished	–	–	4183	34.79
	–	–	24.4	2.26
	40	1	43.8	2.35
	60	1	102.2	2.64
Nano-textured	120	1	120.8	4.28
	240	1	78.2	8.91
	60	2	1092	2.49
	120	2	461	12.25

Interestingly, an order of magnitude higher $\tau_{eff} \sim 1092$ μs could be achieved just by using optimal DRE time of 60 s. Further removal of silicon resulted in reduced lifetime; yet, higher than the ones achieved during DRE sequence 1 processes. Moreover, 120 s DRE performed using sequence 2 resulted in significantly higher R_W values compared to the samples etched for same time using DRE sequence 1. This behavior could be attributed to the fact that DRE sequence 1 is applied on the hydrophobic surface (HF treatment being last cleaning step), resisting the etchants to dislodge the defects from the surface. While, sequence 2 assists in removal of residues and defects more effectively due to follow up cleaning procedures. Thus the results indicate that an optimal DRE sequence and process time does not increases the reflectance significantly rather improves τ_{eff} due to the removal of the surface defects on the wafer.

3.2.2. Comparison of lifetime measurements

The recombination at randomly textured surface is generally larger than the recombination at an equivalent planar ⟨100⟩ surface [11]. This is attributed to the fact that, higher surface recombination arises from an increase in surface area and an exposure of planes having ⟨111⟩ crystal orientations with high defect densities [12]. Samples investigated under AFM reveals that, our nano-textured wafers have about four times higher surface area compared with the planar silicon wafers and about two times higher than the micro-pyramid textured silicon wafers, which brings out even more surface defect states and dangling bonds responsible for lifetime reduction as shown in Table 1. But, the optimised nano-structured surface formed after DRE measures much higher lifetime and lower surface recombination velocities (SRV) compared to the micro-textured counterpart. The effective surface recombination velocity (S_{eff}) was determined by assuming infinite bulk lifetime and is given by [13],

$$S_{eff} \leqslant \frac{W}{2\tau_{eff}}$$

with τ_{eff} and S_{eff} the maximum SRV on either side of the wafer and W the sample thickness.

The planar and micro-textured samples are symmetrical samples and for this reason the surface recombination velocity on both surfaces will be acceptably similar, for this case Sproul [14] has proposed a dimensionless solution for the surface recombination component ($\tau_{surface}$) of the effective lifetime (τ_{eff}). Instead, for the nano-textured the structure is not symmetric. However it fulfills the requirements of another structure for which Sproul proposed another formulation.

When both surfaces are symmetric $S = S_1 = S_2$,

$$\tau_s = \frac{w}{2S} + \frac{1}{D}\left(\frac{w}{\pi}\right)^2$$

and when one surface is perfectly passivated, so $S_2 = 0$,

$$\tau_s = \frac{w}{S_1} + \frac{4}{D}\left(\frac{w}{\pi}\right)^2$$

Table 2
Summary of τ_{eff} measured on different surfaces. For comparison area factor, $\tau_{surface}$ and S_{eff} of each surface is given.

Surface type	Area factor	τ_{eff} (μs)	$\tau_{surface}$ (μs)	S_{eff} (cm/s)
Planar	1	4183	4414	5.96
Micro-textured	1.73 [12]	393	395	68.20
Nano-textured	4	1092	1107	49.25

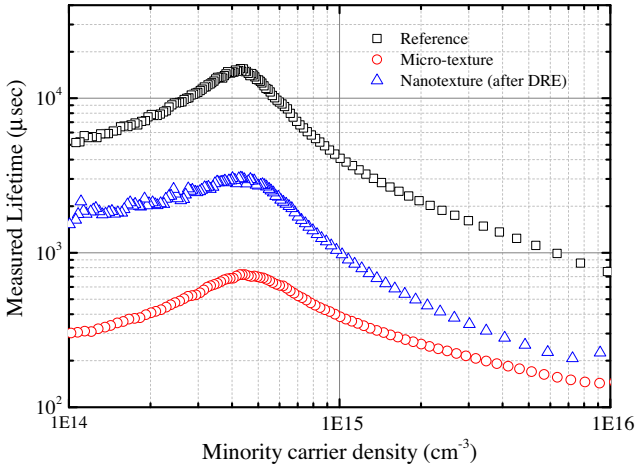


Fig. 4. Injection level dependent lifetime measured on different surfaces passivated with 30 nm SiO_2 layers. The samples were annealed in forming gas at 400 °C for 30 min. Polished (un-textured) surface outperforms textured group in terms of higher lifetime values, indicating very low amount of recombination rate.

τ_s is function of the surface recombination velocities S_1 and S_2, the cell width w and the minority carrier diffusivity D.

Lifetime and surface recombination velocities at an excess carrier density of 1×10^{15} cm^{-3} of all studied surfaces are summerised in Table 2.

As discussed in previous section, DRE plays a key role in the surface preparation to increase lifetimes; possibly also by locally reducing nano-roughness on these structures which has positive influence on the quality of passivation. Besides that, non-textured areas are also present in the nano-textured samples due to periodic nature of the imprinted process which could also contribute to the higher lifetime for these samples. The injection level dependent lifetime curves (see Fig. 3) shows almost half and a full order of magnitude gain for planar surface over nano- and micro-textured surface respectively.

All lifetime curves in Fig. 4 show the expected decrease in effective lifetime at the higher injection levels due to Auger recombination. The decrease in effective lifetime in low injection level for micro-textured surface is more significant than the nano-textured surface which can be attributed to increased SRH recombination in the bulk or at the surface. Other than the textured morphology, there can be additional causes of low electrical performances and investigation of this is out of the scope of this work. From our investigation, we have observed that the surface enlargement due to texture process reduces the lifetime up to a large extent but the sample preparation plays a major role in recovery of lifetime. Our optically superior nano-textured surface outperformed the studied micro-textured surface in terms of passivation quality, proving its suitability for solar cells.

4. Conclusion

For the first time, we present a comparison of different surface morphologies passivated with thin thermal oxide layer based on their optical and electrical properties. The substantial surface damage caused by pattern transfer through the plasma etching process can be removed by appropriate DRE process allowing the introduction of superior suppression of reflection without any detrimental effect in the lifetime of carriers. We conclude that despite the surface enlargement by a factor of 2 compared to the micro-textured surface, our optimised nano-textured surface allows in obtaining superior AR properties while keeping the better quality of surface passivation, highly important for solar cell application.

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