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Next-generation multi-crystalline silicon solar cells: Diamond-wire sawing, nano-texture and high efficiency

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ABSTRACT

The absence of an effective texturing technique for diamond-wire sawn multi-crystalline silicon (DWS *mc*-Si) solar cells has hindered commercial upgrading from traditional multi-wire slurry sawn silicon (MWSS *mc*-Si) solar cells. In this paper, a nano-texture technique has been developed to achieve 18.31% efficient DWS *mc*-Si solar cells on a pilot production line. Their unique pyramidal nanostructure, which has the most close-packed {111} surface of Si diamond crystal, not only benefits both light-trapping and electric properties but also can effectively remove the saw-marks and amorphous layer of the cells. Therefore, the short-circuit current I_{sc} of a nano-textured DWS *mc*-Si solar cell is ~324 mA higher than that of a micron-textured one, while its open-circuit voltage V_{oc} does not show an evident decrease with the increase of its surface area. The technique has paved the way for the mass production of DWS *mc*-Si solar cells by satisfying the exact requirements of the PV industry for high efficiency and low cost.

1. Introduction

In the past few decades, multi-wire slurry sawing (MWSS) has been a mainstream technique for slicing large ingots of single/multi-crystalline silicon (*sc*-Si/*mc*-Si) into thin wafers in the PV industry [1,2]. However, as its production increased to several hundred thousand tons each year, MWSS shortages eventually emerged, including low productivity, high breakage of steel-wire, and high material consumption and industrial waste (i.e., non water-soluble cutting fluid, slurry and disposable wires). Therefore, several research groups have demonstrated that diamond wire sawing (DWS) has several superiorities over MWSS, i.e., 2.5-fold slicing speed, half the thickness of the saw-damage layer, and water-soluble coolant without any slurry [3,4]. More importantly, DWS showed great potential for cutting thin wafers down to 60 μm [5]. Therefore, DWS is expected to become a next-generation slicing technique for fabricating wafer-based Si solar cells. In fact, DWS *sc*-Si solar cells that are fabricated in production lines have shown comparable photovoltaic properties to MWSS ones [6].

Unfortunately, DWS *mc*-Si solar cells are still unpopular and unacceptable in the PV industry mainly due to the lack of an effective texture technique. In general, the normal texture process for MWSS *mc*-Si wafers, which is based on the isotropic acidic etching of a HNO_3/HF system, can reduce the reflection of a wafer down to ~23%. In our preliminary works, the reflection loss of a DWS *mc*-Si wafer after the same texture process is still as high as ~28%, resulting in a 0.4% lower power conversion efficiency (η) than that of an MWSS wafer. Unlike the randomly and homogeneously fractured surface in MWSS wafers, the existence of directional saw marks and an incompletely covered amorphous Si layer in DWS wafers will result in an undesirable texture, as will be discussed later. Because *mc*-Si solar cells have occupied more than 80% of the photovoltaic (PV) market, it is an urgent requirement for PV researchers and the industry to develop an effective texture technique for efficient DWS *mc*-Si solar cells.

Recent progress in nanostructure textured black silicon has attracted intensive attention due to its great potential for applications in silicon-based solar cells [7–11]. There are several advantages of black silicon solar cells: excellent light trapping in a wide spectrum ranging from 300 to 2000 nm [7]; the possibility of removing the need for expensive plasma-enhanced-chemical-vapor-deposition (PECVD) processing; and wider acceptance angle of light [12]. There are three main types of techniques for fabricating black silicon: laser texturing [9,10], reactive ion etching (RIE) [13–16], and metal-catalyzed chemical etching (MCCE) [17,18]. For mass production, the RIE and MCCE techniques have high expectations, but obviously MCCE is much more suitable for the current industry product line where the texturing process is also based on chemical solutions due to their low-cost and stability. It is worth mentioning that the efficiency of the

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nanostructured MWSS *mc*-Si solar cells have reached over 18% in our group through the use of an MCCE technique [19].

In this work, we demonstrate that DWS *mc*-Si solar cells can achieve an efficiency as high as 18.31% after being nano-textured and having their saw marks eased.

2. Experiments

A standard process for producing *mc*-Si solar cells consists of four main steps, i.e., obtaining a micron-textured surface by using acid etching in an HNO_3/HF mixture solution, forming a *p*–*n* junction emitter by diffusing phosphorus into silicon, depositing the SiN_x antireflection/passivation layer by PECVD, and metalizing the top/bottom electrodes by screen printing and firing. In this work, one group of MWSS *mc*-Si wafers and two groups of DWS *mc*-Si wafers from same batch (20 pieces each, $156 \times 156 \times 0.18\ mm^3$, *p*-type, specific resistance $\rho = 1–3\ \Omega$ cm, GCL company, China) had normal acid etching applied first to obtain the micron-texture (labeled as MT-MWSS *mc*-Si and MT-DWS *mc*-Si). Then, one group of MT-DWS *mc*-Si wafers underwent a nano-texture process (as detailed elsewhere [19]) to incorporate a nano-pyramid structure onto the surface (labeled as NT-DWS *mc*-Si). In this process, the wafer was first loaded with Ag nano-particles on the surface by using an electroless plating method, was then placed in a mixture solution of H_2O_2 and HF to form an array of nano-pores, and was finally post-etched in an alkali solution, such as NaOH, to convert the nano-pore texture into a unique nano-pyramid texture. Finally, three groups of wafers (MT-MWSS *mc*-Si, MT-DWS *mc*-Si and NT-DWS *mc*-Si) were fabricated into solar cells in a pilot product line with the same parameters.

The microstructure, reflection, external quantum efficiency (EQE), doping concentration, surface sheet resistance, lifetime of minority carrier and IV curves of the resulted DWS *mc*-Si wafers or solar cells were measured by SEM (Hitachi, S4800, Japan), TEM (FEI Tecnai G2F20S-Twin,USA), Reflectometer (Radiation Technology D8, China), PV Measurements (QEX7, USA), ECV Pro (Nanometrics, UK), 4 Probe sheet resistance tester (Napson RT-70V, Japan), IV measurement system (Berger PSL-SCD, Germany), and WT2000 (Semilab WT2000, Hungary), respectively.

3. Results and discussion

3.1. The comparison of as-cut DWS and MWSS mc-Si wafers

The surface microstructure of as-cut silicon wafers has a strong influence on the etching behavior. Fig. 1 shows photos and SEM images of DWS and MWSS *mc*-Si wafers. Different from the homogeneously distributed rough, dentate, and fractured surface of gray MWSS *mc*-Si wafers, shiny silver DWS *mc*-Si wafers feature smooth areas, individual fractures, parallel grooves and many cracks (Fig. S1, Supporting information) [4]. In principle, the cutting mechanisms of MWSS and DWS wafers are quite different: the former was sliced by rotating free-SiC particles driven by a high-speed moving wire [2], and the latter was sawn by fixed-diamond particles adhered to a high-speed moving wire [3]. Obviously, the clearly visible parallel grooves with lateral cracks on the surface of DWS wafers were the trace lines of the kerfs of diamond blades, the smooth areas may be the bottom parts of the grooves after their laterals were scratched by later incoming diamond blades, and the disperse fractures were mainly formed by

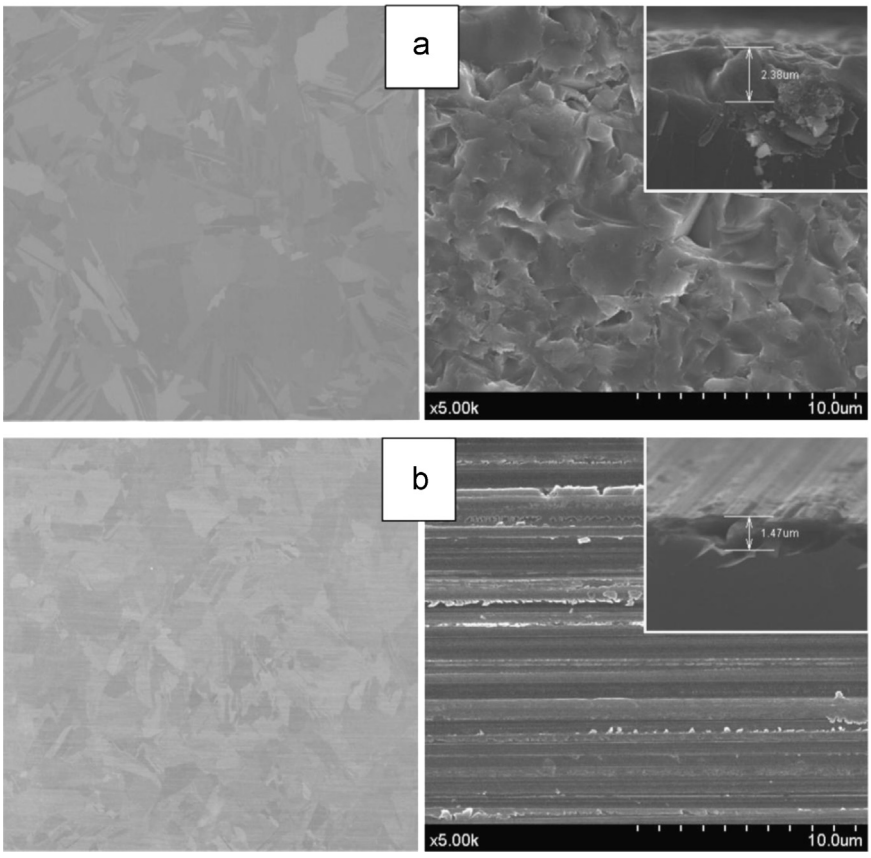

Fig. 1. Surface photos (left) and SEM images (right) of (a) MWSS and (b) DWS *mc*-Si as-cut wafers. Insets: the cross-section images of the wafers.

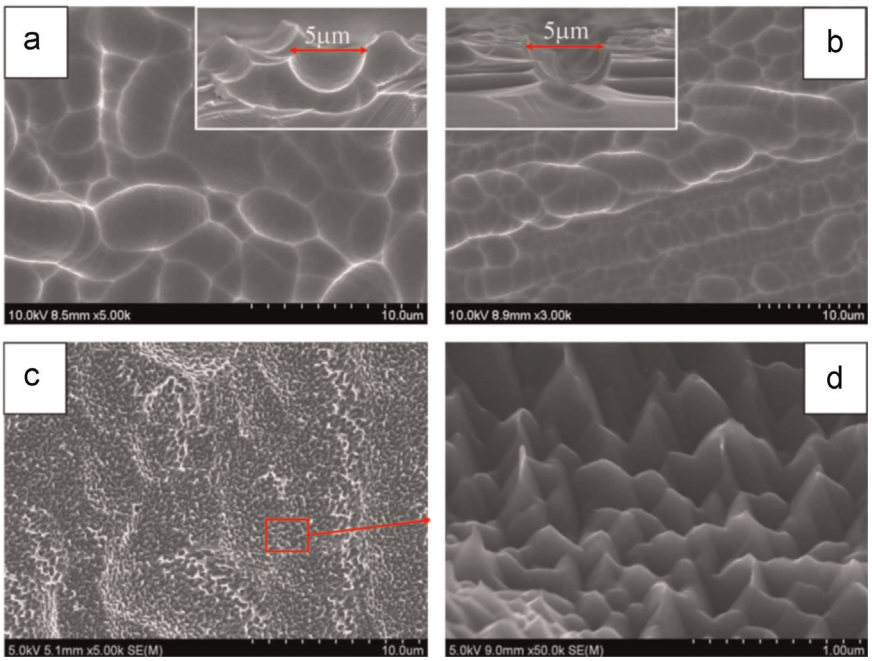

Fig. 2. SEM images of the surface of (a) a micron-textured MWSS *mc*-Si wafer, (b) a micron-textured DWS *mc*-Si wafer, and (c) and (d) a nano-textured DWS *mc*-Si wafer in two magnifications. Insets in (a) and (b): the cross-section of an oval pit in a DWS wafer is much shallower than that of an MWSS wafer.

the random striking of the diamond particles. It was suggested that the smooth areas among the grooves of as-cut DWS *mc*-Si wafers not only cause them to have a higher initial reflection than that of MWSS *mc*-Si wafers (~36% vs. ~28%, see Fig. 3) but may also be a main reason for the shallow oval pits formed after acid etching [4]. The damage layer of an MWSS *mc*-Si wafer is deeper than that of a DWS one, and it has a crucial influence on the microstructure during the etching process [20].

3.2. Microstructure and reflection evolution of DWS mc-Si wafers during the texture process

Both MWSS and DWS *mc*-Si wafers underwent the same acid etching to remove the damage layer and form the micron-sized texture, and the mass losses after etching are roughly 5% and 4%. Fig. 2(a) and (b) compares the surface and cross-sectional morphologies of two wafers. Obviously, the oval pits in the MWSS wafer are deeper than those of the DWS wafer because a thin amorphous silicon layer only found in the DWS wafer will prevent effective etching of the surface [21]. Interestingly, those strings of either large or tiny oval pits inherited the orientation of the grooves. We believe that those large oval pits were originally developed from cracks at the lateral groove, but the small ones were from the smooth areas on the surface. Moreover, few deep pits were found as a result of the etching of the fractures.

One group of MT-DWS *mc*-Si wafers was first loaded with silver particles (Fig. S2**,** Supporting information) and were then etched in a HF/H_2O_2 solution to obtain a nano-texture. As shown in Fig. 2 (c) and (d), a uniform nanostructure was successfully incorporated into the former micro-texture. More exciting, the profile as well as the orientation of the micron pits is not very evident. Our previous work showed that easing off the saw marks could significantly benefit the cell performance [22]. The height and diameter of the nanostructure are in the range of 100–200 nm.

Fig. 3 shows the reflectivity R vs. the wavelength (350–1050 nm) curves of wafers with different microstructures. The average reflectivity $\bar{R}$of the as-cut DWS *mc*-Si wafer (36.73%) is ~9% higher than that of the MWSS wafer (27.94%), while the $\bar{R}$of acid-etched DWS *mc*-Si wafer (28.50%) is ~5% higher than that of

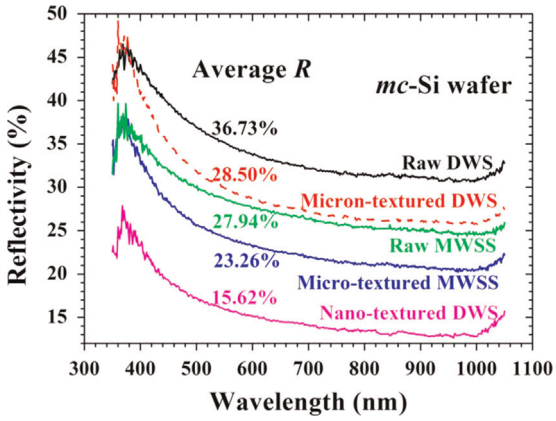

Fig. 3. Reflectivity of MWSS and DWS *mc*-Si wafers of different microstructures.

the MWSS one (23.26%). In our preliminary work, the efficiency of the micron-textured DWS *mc*-Si solar cell is ~0.4% lower than that of the MWSS one. The above results indicated that the current texture process used in the industry product line for MWSS *mc*-Si wafers is incapable of completing an effective texture for DWS *mc*-Si wafers, which is a primary obstacle for the PV industry in adopting DWS *mc*-Si wafers as a replacement of traditional MWSS *mc*-Si wafers.

Actually, the reflection of a nanostructured DWS *mc*-Si wafer can be reduced and made very low (i.e., ~5%, Fig. S3, Supporting information). However, its efficiency is roughly 13–16.5%, which is lower than the 17.5% efficiency of normal *mc*-Si solar cells due to strong recombination, which is proportional to the high surface area of the nanostructure [23]. Therefore, a post-etching step was applied to the nanostructured DWS *mc*-Si wafer to reduce the surface area. In the present work, an average R of ~15.6% was optimized for nano-textured DWS *mc*-Si wafers by considering a balance between the optical and electrical properties of the final cell.

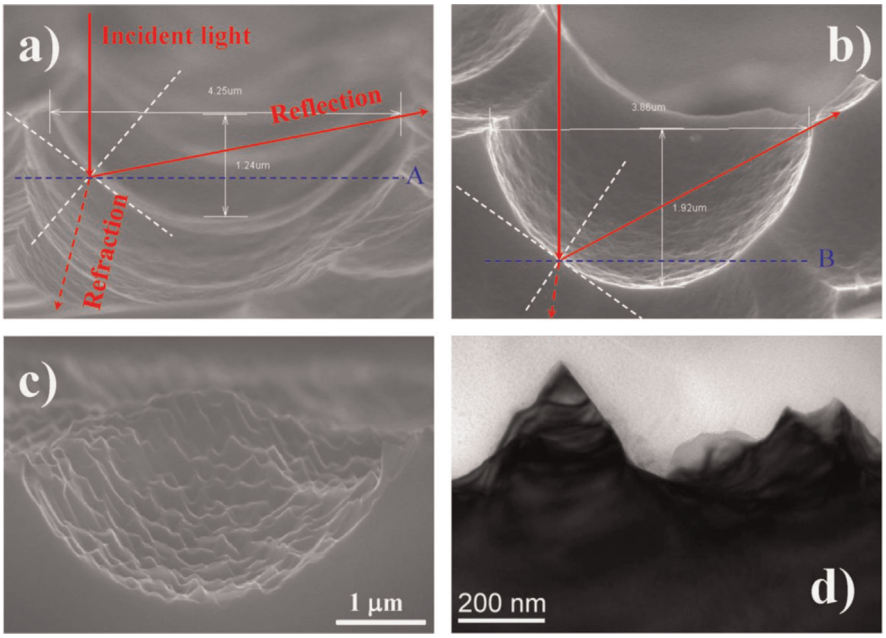

Fig. 4. Cross-sectional SEM images of (a) a micron-textured DWS *mc*-Si, (b) a micron-textured MWSS *mc*-Si, and (c) a nano-textured *mc*-Si. Lines A and B represent the plane that determines whether the incident light will be reflected into the air or re-refracted into the silicon (d) a cross-sectional TEM image of a nano-textured *mc*-Si wafer, showing that the nano-pyramid has an average height of ~150 nm.

3.3. *Light trapping simulation of the DWS mc-Si wafer with nano-texture*

Based on the above results, there is no doubt that the light trapping ability in DWS *mc*-Si wafers is strongly dependent on the surface texture conditions. Fig. 4 gives more insight into the investigations concerning the mechanisms behind this. After acid etching, micron-sized oval pits are formed in the surfaces of both MWSS and DWS wafers, but their sizes are quite different. Fig. 4 (a) and (b) shows two typical oval pits in DWS and MWSS wafer surfaces; the DWS pit has a large opening (~4.25 μm) and shallow depth (~1.24 μm) in contrast to the ~3.86 μm opening and 1.92 μm depth of the MWSS pit. Such a micron-texture is larger than the wavelengths of incident visible light, and thus, the reflection and refraction behaviors at the wafer surface can be explained as being classic optical. Here, we define a critical plane (i.e., plane A for the DWS pit and plane B for the MWSS pit), which can be determined by the pit's curvature radius, as shown in the images. One can imagine that the light irradiated at the pit surface above the critical plane will be partially refracted into the silicon substrate, be partially reflected, and then reach the other side of the pit surface and thus have a second chance to be refracted into the substrate; in the case where light reaches the pit surface below the critical plane, it will be directly reflected into the air instead of re-entering the silicon substrate. Obviously, a DWS pit with a larger curvature radius and shallower depth will reflect more light into the air than that of the MWSS pit, which is the main reason for their difference in reflection (28.5% vs. 23.26%). However, even 23.26% reflection is still very high for a solar cell; thus, in industry, the SiN_x layer (80–90 nm) is coated to further reduce the wafer reflection to an acceptable level, such as ~8%.

As shown in Fig. 4(c), the nano-textured DWS *mc*-Si wafer had a double-scale surface texture, indicating a remarkable light-trapping ability [24], which partly comes from the contribution of micron-sized oval pits (~8% reduction in R from 36.73% to 28.5%) and is partly attributed to its nanostructure (~13% reduction in R from 28.5% to 15.6%). The light-trapping mechanism of the nanostructure is usually attributed to the gradient-index, from $n_{air}=1$ (refractivity of air) to $n_{si}=3.5$ (refractivity of silicon) [25]. It should be noted that the pseudo pyramid nanostructure is formed after alkali etching. Pyramids with an average height of ~150 nm are shown in Fig. 4(d). Such a pyramid texture ensures that the wafer surface is covered by the most close-packed {111} crystal surface, thus benefitting not only its light-trapping but also its electron-transporting abilities [21].

To theoretically study its light trapping properties, a nano-textured DSW *mc*-Si wafer can be treated as a multilayer of pyramid-air binary, as illustrated in Fig. 5(a). Similar to the model of optically graded surfaces [26], such a multilayer also can be thought of as a medium with a gradient refractive index and impedance, which can smoothly connect the air and the Si substrate. The effective index is calculated based on quasi-static effective medium theory (EMT) [27,28], which gives $n_{eff}=\sqrt{\left(n_{Si}^2+1+f_{Si}\left(n_{Si}^2-1\right)\right)/\left(n_{Si}^2+1-f_{Si}\left(n_{Si}^2-1\right)\right)}$, with n_{Si} and f_{Si} being the refractive index and filling ratio at different positions, respectively. We note that such an EMT is valid when the lattice constant of the nanostructure is much smaller than the operating wavelength. Here, the operating wavelength is chosen as 800 nm to guarantee the approximate validity of the EMT. In Fig. 5(b), we plot the effective refractive index n_{eff} as a function of the position in the direction of height for a nanostructure having a height of 150 nm and a lattice constant of 212 nm ($\sqrt{2}\times 150$ nm). It shows that n_{eff} continuously changes from 1 to 3.5, indicating that the sudden change of the impedance at the interface of air and Si has been smoothed. As a consequence, the reflection can be largely reduced.

We construct a model (Fig. S4, Supporting information) to simulate the reflectance with respect to the height of the nanostructures, as shown in the left of Fig. 5(c). An incident wave is propagating along the z direction and impinges on the Si wafer with pyramid-textured surface, and the transmitted waves are absorbed by a perfect matched layer (PML). The right of Fig. 5 (c) presents the x-component electric field E_x distribution. The incident electric field polarized in the x direction is normalized to unity, and the maximal value of the E_x in the air region slightly exceeds unity due to the reflection. The simulated results in Fig. 5 (d) indicate that the reflectance rapidly decreases with the

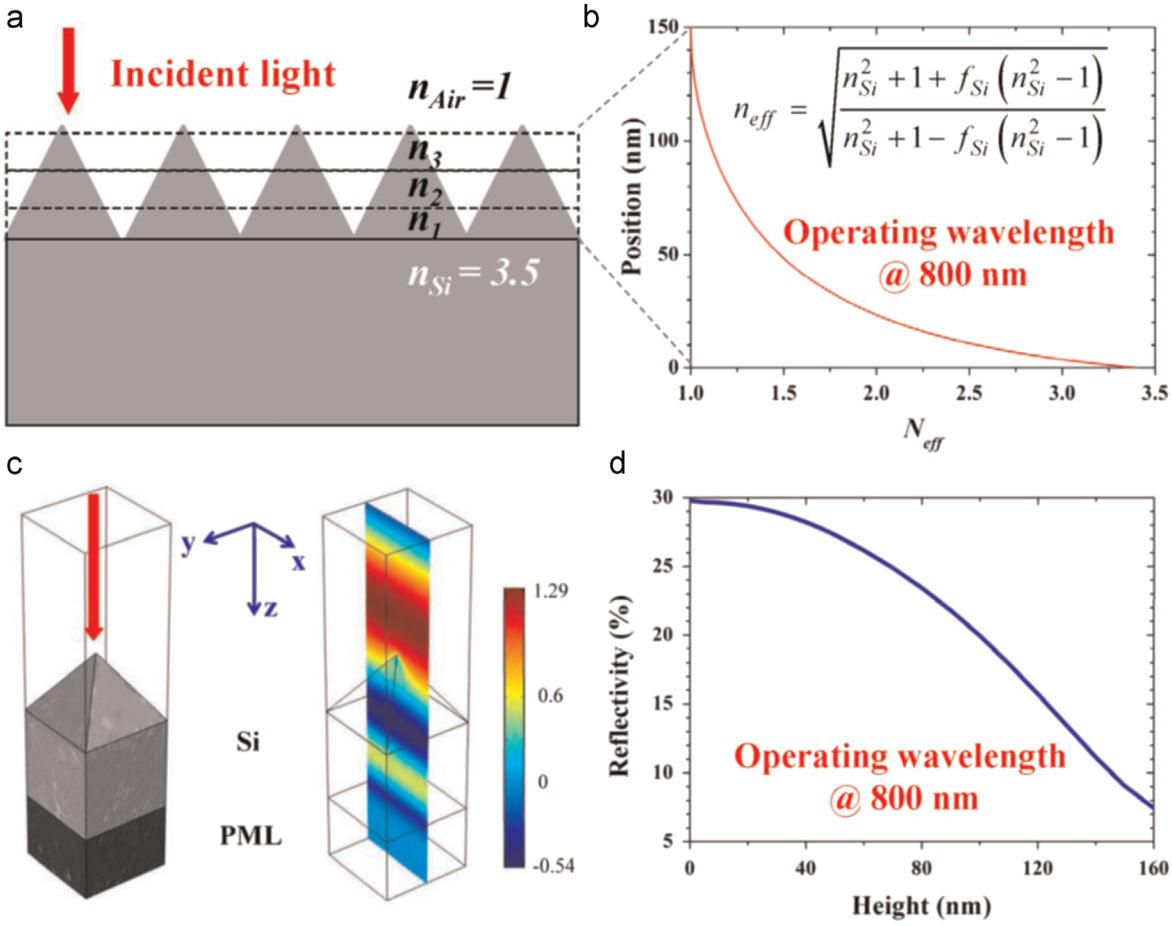

Fig. 5. (a) Illustration of a Si wafer with a nano-pyramid texture, which can be treated as multi-layers of different refractive indexes. (b) The effective refractive index as the function of the position in the height direction for the pyramid nanostructure with a height of 150 nm. (c) The simulation structure for reflection (left) and a snapshot of the resulting *x*-component of the electric field (right). (d) The simulation reflectance vs. the height of the pyramid nanostructure.

increase of the height, and it suggests that pyramid nanostructures with higher height can generate a smoother transition of the refractive index and impedance, resulting in lower reflection. However, in the practice of this work, the height of the nanostructure was kept at approximately 150 nm for the DWS *mc*-Si wafer considering both the electronic and optical properties.

3.4. Characteristics of DWS mc-Si solar cells

Micron-textured MWSS and DWS and nano-textured DWS *mc*-Si wafers were fabricated into solar cells on the production line through the same processes, i.e., phosphorous diffusion, phosphorsilicate glass removal, SiN_x coating by PECVD and screen printing of electrodes followed by a short sintering. Due to the existence of the nanostructure, the thickness of SiN_x in the NT-DWS *mc*-Si wafer is not uniform like that of the MT-DWS wafer (Fig. S5, Supporting information). Note that, a new screen printing pattern of 4 bus lines and 91 grid lines is used to improve the performance of cells with large current (Fig. S6, Supporting information).

With the introduction of nanostructure to the cells, one problem is that the doping concentration on the surface may be higher than normal (i.e., $>10^{18}$ cm^{-3}), and thus, dominant Auger recombination will cause a low lifetime and high surface recombination velocities in the emitter [10]. Therefore, we measured the phosphorus concentration dependence on depth in three samples, as shown in Fig. 6. The p-dopant zone is ~500 nm deep, and the concentration profiles of the three wafers are different due to the differences of the surface microstuctures. From the surface to a

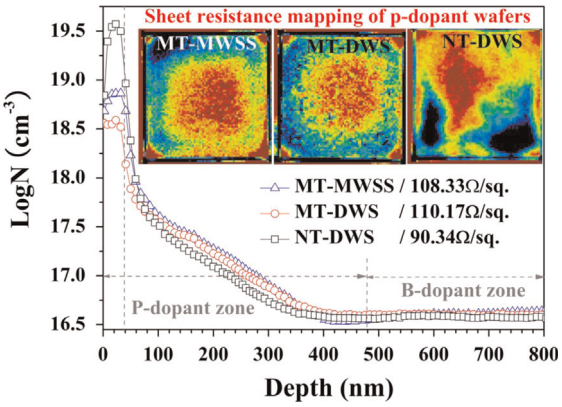

Fig. 6. Phosphorus doping distribution of MWSS and DWS samples. Inset: sheet resistance mapping of p-dopant wafers and the sheet resistances of three samples are labeled.

depth of ~40 nm, both micron-textured MWSS and DWS curves have concentrations below 10^{19} cm^{-3}, whereas the nano-textured DWS *mc*-Si wafers have much higher concentrations ($>10^{19}$ cm^{-3}). In general, high energy light (i.e., wavelength less than 400 nm) that has a large absorption coefficient will be absorbed in a short distance (i.e., less than 100 nm) of the surface [29]. In the case of NT-DWS with a nanostructure depth of ~150–200 nm, the generated carriers are easily recombined in this zone. Fortunately, the concentration profiles from 40 to 500 nm for the three wafers are nearly overlapped. Nevertheless, with the

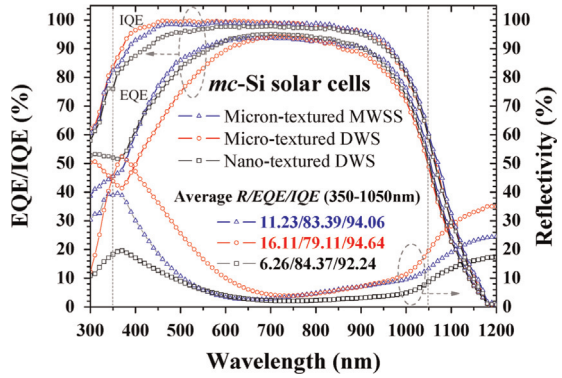

Fig. 7. Reflectivity, EQE and IQE curves of MWSS and DWS *mc*-Si solar cells. The dashed lines are guides for the eye for 350 and 1050 nm. The nano-textured DWS solar cell has lower reflection than the Micron-textured ones.

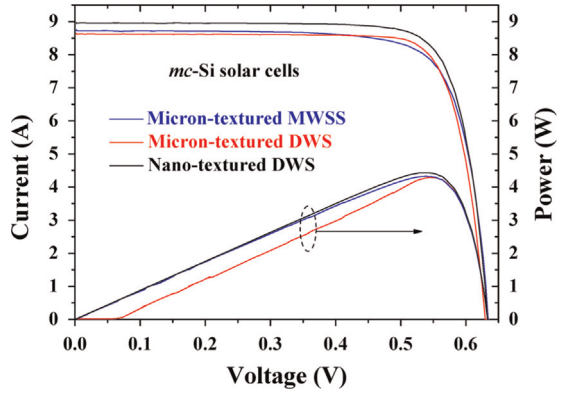

Fig. 8. *I–V* characteristics of *mc*-Si solar cells. The measurement area is $15.6 \times 15.6\ cm^2$, and the corresponding current density of the nano-textured DWS *mc*-Si is 36.74 mA/cm^2 under AM 1.5G illumination.

Table 1
Main characteristics of *mc*-Si solar cells of different textures

mc-Si cell	V_{oc} (V)	I_{sc} (A)	*FF* (%)	η (%)
MT-MWSS	0.634	8.753	78.46	17.89
MT-DWS	0.633	8.651	78.34	17.63
NT-DWS	0.634	8.975	78.31	18.31

optimization of the nanostructure, the doping concentration and surface sheet resistance of the NT-DWS cell were tuned to a reasonable level.

Fig. 7 presents the reflectivity, external quantum efficiency (EQE) and internal quantum efficiency (IQE) of three cells. Note that the average *R* marked in the figure is a total reflection of the cells, including the effects of SiN_x coating and a front silver electrode, and a high *R* will usually result in a low EQE, which is the case for MT-DWS. However, the three IQE curves are almost overlapped in the range from 600 to 1200 nm and then diverge in short wavelengths. The MT-DWS cell has the highest IQE and even its reflection is the highest among the three cells. We believe that the surface condition has a strong influence on the IQE value, which will mainly reflect the situation of surface recombination of electron–hole pairs. Therefore, it is not difficult to understand why a highly reflective MT-DWS cell has a larger overall EQE than a MT-MWSS cell; this may be due to its shallow surface texture. Compared with that of the MT-DWS cell, the IQE of the NT-DWS cell is reduced in the short wavelength region, and it can be attributed to its increased surface area, where the short wavelength light is absorbed mostly. Nevertheless, the EQE of NT-DWS cell is the highest among the three cells, implying that its gain of light trapping with nanostructure is larger than its loss of the surface recombination.

Fig. 8 shows the *I–V* characteristics of our best micron- and nano-textured *mc*-Si DWS solar cells, and the main parameters of the cells are listed in Table 1. The efficiency of the nano-textured DWS *mc*-Si solar cell (18.31%) is 0.64% higher than that of the micron-textured DWS one (17.67%), which could be due to its enhanced light absorption, i.e., the short-circuit current (I_{sc}) has an increase of ~324 mA. More importantly, the open-circuit voltage (V_{oc}) is the same for both DWS cells, confirming that the problem of extra recombination introduced by the nanostructure can be neglected.

The PV industry is always in pursuit of new techniques for the mass production of *mc*-Si solar cells, requiring not only high efficiency but also low cost. DWS *mc*-Si cells are expected to reduce the cutting cost from the side of wafers, and its high efficiency has also been confirmed by using our nano-texture technique. We believe that the technique presented in this paper will satisfy the above requirements, and it has a great potential to become a standard process for producing highly efficient *mc*-Si solar cells in the future.

4. Conclusion

In summary, 18.31%-efficient DWS *mc*-Si solar cells with a unique nano-pyramid texture have been fabricated through the use of traditional acid etching and an additional nano-texture process on an industrial production line. The results confirmed that our novel technique can provide an effective texture for DWS *mc*-Si solar cells. Mainly due to its enhanced light-trapping ability, the I_{sc} of a nano-textured DWS *mc*-Si solar cell is ~324 mA higher than that of a micron-textured one. Meanwhile, its V_{oc} retains a high value, which is very important for the properties of modules made from nano-textured cells. The technique has paved the way for the mass production of DWS *mc*-Si solar cells by satisfying the requirements of the PV industry for high efficiency and low cost.

Acknowledgments

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Appendix A. Supplementary material

Supplementary data associated with this article can be found in the online version at http://dx.doi.org/10.1016/j.solmat.2015.05.030.

References

[1] H.J. Möller, C. Funke, M. Rinio, S. Scholz, Basic mechanisms and models of multi-wire sawing, Adv. Eng. Mater. 6 (2004) 501–513.
[2] H.J. Möller, C. Funke, M. Rinio, S. Scholz, Multicrystalline silicon for solar cells, Thin Solid Films 487 (2005) 179–187.
[3] N. Watanabe, Y. Kondo, D. Ide, T. Matsuki, H. Takato, I. Sakata, Characterization of polycrystalline silicon wafers for solar cells sliced with novel fixed-abrasive wire, Prog. Photovolt.: Res. Appl. 18 (2010) 485–490.
[4] B. Meinel, T. Koschwitz, J. Acker, Textural development of SiC and diamond wire sawed sc-silicon wafer, Energy Procedia 27 (2012) 330–336.

[5] X.G. Yu, P. Wang, X.Q. Li, D.R. Yang, Thin czochralski silicon solar cells based on diamond wire sawing technology, Sol. Energy Mater. Sol. Cells 98 (2012) 337–342.
[6] K.X. Chen, Y.Y. Liu, X.S. Wang, L.J. Zhang, X.D. Su, Novel texturing process for diamond-wire-sawn single-crystalline silicon cell, Sol. Energy Mater. Sol. Cells 133 (2015) 148–155.
[7] C. Wu, C.H. Crouch, L. Zhao, J.E. Carey, R. Younkin, J.A. Levinson, E. Mazur, R. M. Farrell, P. Gothoskar, A. Karger, Near-unity below-band-gap absorption by microstructured silicon, Appl. Phys. Lett. 78 (2001) 1850–1852.
[8] J. Oh, H.C. Yuan, H.M. Branz, An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures, Nat. Nanotechnol. 7 (2012) 743–748.
[9] T.H. Her, R.J. Finlay, C. Wu, S. Deliwala, E. Mazur, Microstructuring of silicon with femtosecond laser pulses, Appl. Phys. Lett. 73 (1998) 1673–1675.
[10] C.H. Crouch, J.E. Carey, J.M. Warrender, M.J. Aziz, E. Mazur, Comparison of structure and properties of femtosecond and nanosecond laser-structured silicon, Appl. Phys. Lett. 84 (2004) 1850–1852.
[11] M. Halbwax, T. Sarnet, Ph. Delaporte, M. Sentis, H. Etienne, F. Torregrosa, V. Vervisch, I. Perichaud, S. Martinuzzi, Micro and nano-structuration of silicon by femtosecond laser: application to silicon photovoltaic cells fabrication, Thin Solid Films 516 (2008) 6791–6795.
[12] H.C. Yuan, V.E. Yost, M.R. Page, P. Stradins, D.L. Meier, H.M. Branz, Efficient black silicon solar cell with a density-graded nanoporous surface: optical properties, performance limitations and design rules, Appl. Phys. Lett. 95 (2009) 123501.
[13] J. Yoo, G. Yu, J. Yi, Large-area multicrystalline silicon solar cell fabrication using reactive ion etching (RIE), Sol. Energy Mater. Sol. Cells 95 (2011) 2–6.
[14] J. Kim, D. Inns, K. Fogel, D.K. Sadana, Surface texturing of single-crystalline silicon solar cells using low density SiO_2 films as an anisotropic etch mask, Sol. Energy Mater. Sol. Cells 94 (2010) 2091–2093.
[15] H. Kohata, Y. Saito, Maskless texturization of phosphorus-diffused layers for crystalline Si solar cells by plasmaless dry etching with chlorinetrifluoride gas, Sol. Energy Mater. Sol. Cells 94 (2010) 2124–2128.
[16] P. Choulat, G. Agostinelli, D. Dehertoghe, G. Beaucarne, Improved performances of *mc*-Si solar cells on thin multi-crystalline silicon substrate, in: Presented in 22nd European Photovoltaic Solar Energy Conference and Exhibition, Milan, Italy, 2007.
[17] S. Koynov, M.S. Brandt, M. Stutzmann, Black multi-crystalline silicon solar cells, Phys. Status Solidi (RRL) 1 (2007) R53–R55.
[18] S. Koynov, M.S. Brandt, M. Stutzmann, Black nonreflecting silicon surfaces for solar cells, Appl. Phys. Lett. 88 (2006) 203107.
[19] X.Y. Ye, S. Zou, K.X. Chen, J. Li, J. Huang, F. Cao, X.S. Wang, L.J. Zhang, X.F. Wang, M.R. Shen, X.D. Su, 18.45%-efficient multi-crystalline silicon solar cell with nano-scale pseudo-pyramid texture, Adv. Funct. Mater. 24 (2014) 6708–6716.
[20] J. Acker, T. Koschwitz, B. Meinel, R. Heinemann, C. Blocks, HF/HNO3 etching of the saw damage, Energy Procedia 38 (2013) 223–233.
[21] A. Bidiville, K. Wasmer, R. Kraft, C. Ballif, Diamond wire-sawn silicon wafer: from the lab to the cell production, in: Presented in 24th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany, 2009.
[22] K.X. Chen, Y.Y. Liu, X.S. Wang, L.J. Zhang, X.D. Su, Novel texturing process for diamond-wire-sawn single-crystalline silicon solar cell, Sol. Energy Mater. Sol. Cells 133 (2015) 148–155.
[23] C. Chartier, S. Bastide, C. Levy-Clement, Metal-assisted chemical etching of silicon in HF–H_2O_2, Electrochim. Acta 53 (2008) 5509–5516.
[24] F. Toor, H.M. Branz, M.R. Page, K.M. Jones, H.C. Yuan, Multi-scale surface texture to improve blue response of nanoporous black silicon solar cells, Appl. Phys. Lett. 99 (2011) 103501.
[25] H. Lv, H. Shen, Y. Jiang, C. Gao, H. Zhao, J. Yuan, Porous-pyramids structured silicon surface with low reflectance over a broad band by electrochemical etching, Appl. Surf. Sci. 258 (2012) 5451–5454.
[26] R.B. Stephens, G.D. Cody, Optical reflectance and transmission of a textured surface, Thin Solid Films 45 (1977) 19–29.
[27] J.C. Maxwell-Garnett, Colors in metal glasses and metal films, Philos. Trans. R. Soc. Lond., Ser. A 203 (1904) 385–420.
[28] Y. Wu, J. Li, Z.Q. Zhang, C.T. Chan, Effective medium theory for magnetodielectric composites: beyond the long-wavelength limit, Phys. Rev. B 74 (2006) 085111.
[29] M.A. Green, Solar Cells: Operating Principles, Technology and System Applications, University of New South Wales, Australia, 1998.