Michelle Y. Ho

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EDUCATION

Stanford University - MS in Electrical Engineering
University of Arizona - BS with Honors in Electrical Engineering

TECHNICAL SKILLS:

Languages: Python, Bash, SQL, C++, Java
Frameworks/Tools: Pytest, Ansible, Jenkins, Flask, Git, Gitlab CI, TeamCity
Operating System: Linux (CentOS, Fedora, Ubuntu, RHEL), Windows

WORK EXPERIENCE:

Intel - Software Engineer - Infrastructure, Automation, Build & Release **Santa Clara, 2018 - Present**

- Architected and implemented the Open FPGA Stack (OFS) configuration tool for FPGA IP subsystem designs. Reduced users design time from 1 day to less than 30 minutes by reliably producing complex configurations of PCIe, Ethernet, memory and clock systems for FPGA design.
- Designed, implemented and maintained the build system for OFS hardware source code. Debugged and resolved any build breaks to ensure artifacts are successfully created and available for daily regression testing. Integrated notification and dashboard tools for monitoring build history.
- Implemented organization's test framework, used on a daily basis to validate the integration of FPGA code with software stack. Built to be modular, extensible, and configurable across environments. Integrated open source frameworks, such as Pytest and Ansible. Worked with end users to define feature additions.
- Single-handedly improved test regression pass rate from 40% to 99%. Performed daily test failure analysis, test logic rewrite, and discussion with subject matter experts to resolve bugs and improve code quality.
- Managed and delivered internal and external releases for all OFS, FPGA Programmable Accelerator Cards, and Open Programmable Acceleration Engine products.
- Prototyped a Flask application that tracks key release information and test regression results.

Intel - Automation Tool Developer for FPGA Validation **Santa Clara, 2017 - 2018**

- Worked on Scalable Performance Server Development Group's Cicada Chip, a custom state-of-the-art server processor chip.
- Designed and implemented an algorithm in Python to intelligently tailor test suite to the desired FPGA configuration.
- Constructed a program that parses through PCIe transaction logs for the purpose of analyzing system hangs and other unexpected behaviors. This empowered client teams to reduce debug time from 1 week to 1 day.

Cisco – ASIC Validation Engineer **Santa Clara, 2011 – 2017**

- Validated 3 Enterprise Switching ASIC chips for Cisco flagship access networking solutions.
- Developed code to automate programming of registers on the chip. Helped accelerate test and debug efforts.
- Exhaustively verified and performed coverage analysis on multiple blocks on the chip to ensure functionality.

LEADERSHIP/VOLUNTEER:

Women Who Code - Silicon Valley Chapter - Director **SF Bay Area, 2018-Present**

- Led chapter to the 2nd most active WWCode chapter in the world. (https://www.womenwhocode.com/sv/about)
- Organized the majority of technical workshops and talks to audiences of 100+. Some events included: Data Structures & Algorithms for Interviews, Intro to Data Science / Machine Learning, Intro to Git, career talks, etc.
- Successfully pitched to multiple tech companies for multi-year collaboration and sponsorship.
- Served as a mentor to other women, with a focus on helping women switch careers to software development.

Intel AI for Social Good **Santa Clara - 2019**

- Collaborated with lead data scientist on Intel's project with the National Center for Missing and Exploited Children (NCMEC). Developed a Flask application that transforms a Cybertip line data report into a geolocation identification for the specific law enforcement agency to be contacted for help.