Michelle Y. Ho

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EDUCATION

Stanford University — MS in Electrical Engineering
University of Arizona — BS with Honors in Electrical Engineering

TECHNICAL SKILLS:

Languages: Python, Bash, SQL, C++, Java
Frameworks & Tools: Pytest, Ansible, Django, Flask, Git, GitHub Actions, GitLab CI, TeamCity
Operating Systems: Linux (CentOS, Fedora, Ubuntu, RHEL), Windows

WORK EXPERIENCE:

Intel - Software Engineer - Infrastructure, Automation, Build & Release **Santa Clara, 2018 - 2024**

- Architected and implemented in Python a code generator for the Open FPGA Stack (OFS), covering complex PCIe, Ethernet, memory, and clock IP subsystems configurations. Accelerated design workflows by reducing setup time by over 95%, from 1 day to under 30 minutes.
- Rewrote complex Bash build scripts into modular, well-documented Python code and implemented CI/CD pipelines using GitLab CI and GitHub Actions, resulting in 100% of the team being able to maintain the build instead of 20%.
- Single-handedly improved regression test pass rate from 40% to 99% by rewriting test logic to implement more precise validations of code output against test inputs. Partnered with subject matter experts to identify root causes, resolve bugs, and enhance code quality.
- Developed a modular, extensible test framework used daily to validate FPGA-software integration. Integrated Pytest and Ansible to support flexible, cross-environment testing and collaborated with end users to define and prioritize feature enhancements.
- Owned triage and resolution of nightly CI build failures, consistently delivering fixes within 2–3 hours, ensuring successful daily artifact generation, and unblocking globally distributed teams to continue development.
- Automated and delivered 15+ successful releases of Open FPGA Stack products. Streamlined coordination across development, customer engagement, and product security teams, improving delivery timelines by 50%.
- Prototyped a Flask-based tool to track critical release data and regression test results, improving visibility into release status and test outcomes.

Intel - Automation Tool Developer for FPGA Validation **Santa Clara, 2017 - 2018**

- Worked on Scalable Performance Server Development Group's Cicada Chip, a custom state-of-the-art server processor chip.
- Developed a Python parser for PCIe transaction logs to triage system hangs and anomalies, reducing client debug time by 7x, from one week to one day.

Cisco – ASIC Validation Engineer **Santa Clara, 2011 – 2017**

- Automated register programming to accelerate test and debug processes for three enterprise switching ASICs.
- Performed verification and coverage analysis across multiple chip blocks to ensure functional correctness.

LEADERSHIP/VOLUNTEER:

Women Who Code - Silicon Valley Chapter - Director **SF Bay Area, 2018-Present**

- Led chapter to become the 2nd most active Women Who Code chapter globally.
- Organized and facilitated technical workshops and talks for 100+ attendees on topics including Data Structures & Algorithms, Data Science, Machine Learning, Git, and career development.
- Mentored women transitioning to software development careers, providing career guidance and technical support.

Intel AI for Social Good **Santa Clara - 2019**

- Collaborated with lead data scientist on Intel's project with the National Center for Missing and Exploited Children (NCMEC). Developed a Flask application that converts CyberTipline reports into geolocation data, enabling rapid identification of the appropriate law enforcement agency for timely intervention.