Computer Architectures **02LSEOV 02LSEOQ [MA-ZZ]**	Delivery date: Monday 5/11
Laboratory **3**	Expected delivery of lab_03.zip must include: - `program_2_a.s`, `program_2_b.s` and `program_2_c.s` - this file compiled and if possible in pdf format.

Please, configure the winMIPS64 simulator with the *Base Configuration* provided in the following:

- Code address bus: 12
- Data address bus: 12
- Pipelined FP arithmetic unit (latency): 4 stages
- Pipelined multiplier unit (latency): 8 stages
- divider unit (latency): not pipelined unit, 12 clock cycles
- Forwarding is enable
- Branch prediction is disabled
- Branch delay slot is disabled
- *Integer ALU: 1 clock cycle*
- *Data memory: 1 clock cycle*
- *Branch delay slot: 1 clock cycle*.

1) Considering the assembly program you create in the previous lab called **`program_2.s`**, described in the following:

```
for (i = 1; i <= 100; i++){
        v3[i] = v1[i]*v2[i];
        v4[i] = v3[i]/v2[i];
        v5[i] = v4[i]+v2[i];
}
```

   a. Detect manually the different data, structural and control hazards that provoke a pipeline stall
   b. Optimize the program by re-scheduling the program instructions in order to eliminate the most hazards provoking stalls. Compute manually the number of clock cycles the new program (**`program_2_a.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

   c. Starting from the previous program, enable the *branch delay slot* and re-schedule some instructions in order to improve the previous program execution time. Compute manually the number of clock cycles the new program (**`program_2_b.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

   d. Unroll 4 times the program (**`program_2_b.s`**), if necessary re-schedule some instructions and renaming the used registers. Compute manually the number of clock cycles the new program (**`program_2_c.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

Complete the following table with the obtained results:

Program / c.c. computation	program_2.s	program_2_a.s	program_2_b.s	program_2_c.s
By hand	3206	3106	3107	2957
By simulation	3206	3106	3107	2957

2) Compare the results obtained in the point 1, and provide some explanation in the case the results are different.

Eventual explanation:

Note: in program_2_b.s and program_2_c.s I had to add a NOP instruction to avoid the execution of the HALT operation during the branch delay slot while looping.