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M 3003

EM MICROELECTRONIC-MARIN SA

Real Time Clock Circuit

1. Summary

The M 3003 is a monolithic low power CMOS device intended to be used as a Real Time Clock for processor system applications. The internal circuit is clocked with a 32,768 Hz quartz crystal oscillator. Time information is stored in a 15 by 8 bit RAM. An 8 bit status word in the RAM stores the mode of operation programmed by the user. The 4 bit address and data words are multiplexed via TTL compatible I/O pins. Write-in and read-out are performed as in a conventional RAM but additional interrupt facilities are also provided. The time information is in BCD format.

2. Features

- Easy to use like a RAM with fast access time
- Timings and levels compatible with most microprocessors
- Independent watch, alarm and timer functions
- Preset alarm time up to 1 month
- Timer up to 24 hours
- Busy, interrupt and timing output signals provided
- 4 bit BCD format; display system compatible
- Busy output can be used as an 1Hz strobe for display control
- Low standby battery current
- Very few external components needed, except crystal and battery, to keep time during power supply failure
- Watch counts from seconds to 99 years, indicates day of the week, week number, and leap year
- Automatic leap year correction
- Interrupt status available on the bus and on the $\overline{IRQ}$ pin
- $\overline{IRQ}$ also available during battery operation for "sleep and awake" conditions
- Synchronisation input to tune the device by an external time reference
- Test features added

3. Block Diagram

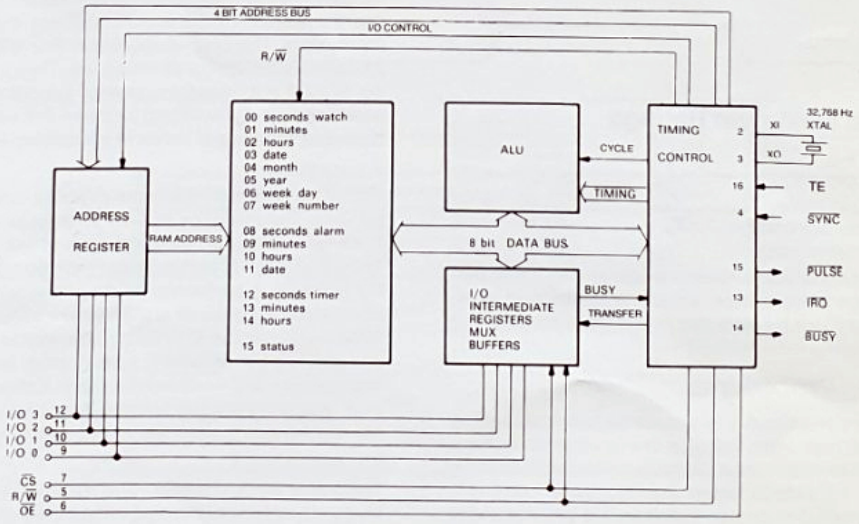

Fig. 1

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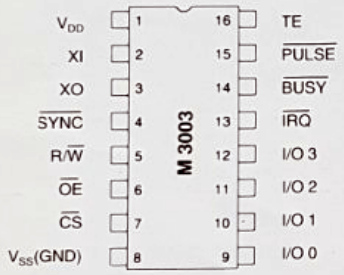
4. Pin Description

Pin	Name	Function
1	V_{DD}	Positive supply terminal
2	XI	32,768 Hz quartz connection
3	XO	32,768 Hz quartz connection
4	SYNC	Watch seconds synchronisation input
5	R/W	Read/write select input
6	OE	Output enable input
7	CS	Chip select input
8	V_{SS}	Ground terminal (GND)
9	I/O 0	Data bus input/output lines, Address bus input lines
10	I/O 1	
11	I/O 2	
12	I/O 3	
13	IRQ	Interrupt request output
14	BUSY	Internal update cycle signal output
15	PULSE	Programmable timing pulse output
16	TE	Transfer enable input



5. Absolute Maximum Ratings

Voltage V_{DD} to V_{SS}	V_{MAX}	−0.3 to +8.0V
Voltage of any pin to V_{SS}	V_{MAX}	−0.3V
Voltage of any pin to V_{DD}	V_{MAX}	+0.5V
Operating temperature range	T_A	−40 to +85°C
Storage temperature range	T_{STO}	−65 to +150°C

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. Handling Procedures

This device contains circuitry to protect the terminals against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit. For proper operation it is recommended that all terminal voltages are constrained to the range $V_{SS} < V_{TERMINAL} < V_{DD}$, unless specially permitted. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

Typical Data Transfer Sequence

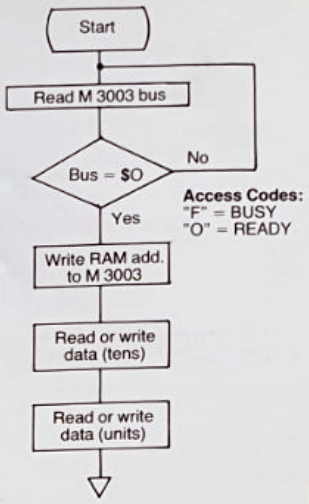


Fig. 2

7. Functional Description

7.1. Power supply and data retention

The M 3003 may be powered with a supply voltage between 2 and 5.5V, backed up with a battery as indicated in Fig. 7 for power-down data retention. Because of the low power consumption of the device, lithium cells or standard rechargeable cells give years of effective life. When the transfer enable input TE goes to a low state, all inputs are disabled, and the I/O lines and the outputs $\overline{BUSY}$ and $\overline{PULSE}$ are set to a high impedance state. The open-drain output $\overline{IRQ}$ will still go to GND if an internal interrupt condition occurs. Thus it is possible to use the M 3003 in a "sleep and awake" condition to switch on the power system. Care should be taken that no parasitic current flows due to improper states of interfacing signal lines.

7.2. RAM

The 16 x 8 RAM is used to store all watch, alarm, timer and status data. The allocation of RAM addresses is shown in Table 1. All time data is stored in the form of two 4-bit BCD words. The transfer of this data between the internal 8-bit bus and the I/O terminals is performed by the bidirectional I/O buffer and multiplexer. If the alarm and timer functions are not used, the RAM section allocated to the addresses 8 to E may be used as an additional non-volatile system storage. In this case the data may assume any hexadecimal value. It should be noted however, that if the unused function is inadvertently activated by altering the status word, the stored data may be modified.

7.3. Status word

The status word, stored at RAM address F, controls the timekeeping functions performed in the ALU section of the M 3003. The functions of the individual bits of the status word are shown in Table 2. The status word must be written after every break of the backup supply.

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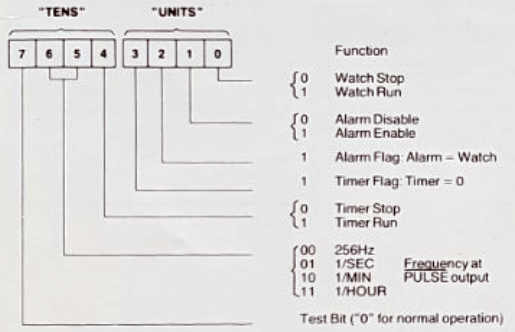
I/O Address Locations Table 1

Address	Data	Group	Max. Value*	Operations
0	Seconds	WATCH	59	Time data
1	Minutes		59	incremented
2	Hours		23	under control of
3	Date		28, 29, 30, 31	status Bit 0
4	Month		12	
5	Year		99	
6	Week day		07	
7	Week no.		53	
8	Seconds	ALARM	59	Alarm data,
9	Minutes		59	providing an IRQ
A	Hours		23	under control of
B	Date		28, 29, 30, 31	status bit 1
C	Seconds	TIMER	59	Timer data
D	Minutes		59	incremented under
E	Hours		23	control of status bit 4
F	Status	STATUS		Control

* Only applicable to WATCH, ALARM and TIMER data.

Status Word Bit Allocations Table 2



7.4. Data transfer

The interface between the M 3003 and the host microprocessor consists of four bidirectional multiplexed data/address lines (I/O 0-3), three control lines ($\overline{CS}$, $\overline{OE}$, R/$\overline{W}$), and an interrupt request line ($\overline{IRQ}$). When power is first applied to the M 3003, the state of the multiplexer is undefined. The multiplexer may be reset by activating $\overline{CS}$ twice for longer than 280ns before any data transfer. This procedure may also be used every time when synchronisation is lost, due to a power failure or a data transfer aborted by the M 3003. Data present on the I/O lines is read from or written into the M 3003 depending on the status of the R/$\overline{W}$ and $\overline{OE}$ input signal. The $\overline{OE}$ input activates the output buffers of the M 3003 during the read-out sequence. If the host processor has no appropriate output signal, $\overline{OE}$ should be connected to $\overline{CS}$.

Fig. 2 shows the flow diagram for a typical data transfer sequence, with the general transfer signals shown in Fig. 4. The appropriate timings for read-out are presented in Fig. 5a; for write-in refer to Fig. 5b.

If consecutive transfers are executed (e.g. seconds, minutes, hours, date), no internal update will occur during this procedure, if the time between two transfers is less than 2ms. Thus, if such procedures are repeated to look for an event or to refresh a display, the delay between two procedures should be greater than 6ms, in order to enable an internal update cycle. However, maximum transfer time restrictions as described under 7.5 must be considered.

7.5. Internal update cycle

Every second, an internal time update occurs and lasts between 0.73ms and 6ms. During this update cycle, the multiplexer is reset, the $\overline{BUSY}$ output is low, and the data on the I/O lines will be "F". The RAM is allocated to the ALU. If an external data transfer is already initiated (see 7.4.), the internal update cycle is delayed for a maximum of one second. Then, the external transfer will be aborted.

7.6. Alarm

An alarm date and time may be preset in RAM addresses 8 to B. During every update cycle, the ALU compares the contents of the watch addresses 0 to 3 with the preset alarm time. When the watch data equals the alarm data and the alarm is enabled (status word bit 1), then the $\overline{IRQ}$ output goes low and the alarm flag (status word bit 2) is set. This status will remain until the alarm flag is acknowledged.

7.7. Timer

By activating the status word bit 4 (timer run), the preset time data in RAM addresses C to E increments every second with the update cycle. When passing from 23:59:59 to 00:00:00, the timer flag (status word bit 3) is set and the $\overline{IRQ}$ output goes low until the flag is acknowledged.

Typical Program Sequence in Response to $\overline{IRQ}$

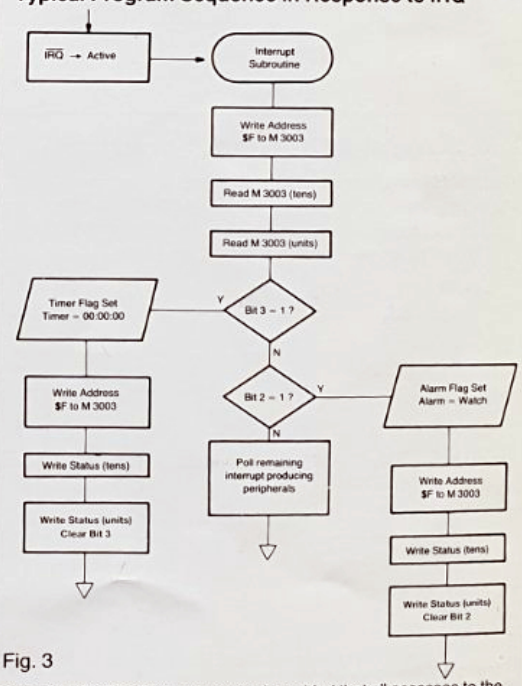


Fig. 3

Note: "BUSY TEST" is not required provided that all accesses to the M 3003 are completed within 1 second of receipt of IRQ.

7.8. $\overline{IRQ}$ output

A low state on the interrupt request output $\overline{IRQ}$ indicates that either the preprogrammed alarm data matches the clock data, or that the timer data has incremented from 23:59:59 to

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00:00:00, provided that the appropriate function is active. Once activated, $\overline{IRQ}$ will remain low until it is acknowledged by resetting the appropriate interrupt flag of the status word. A typical program sequence in response to an IRQ signal is shown in Fig. 3.

7.9. $\overline{PULSE}$ output

The $\overline{PULSE}$ output may be programmed with bits 5 and 6 of the status word to produce a negative pulse of 64μs width every second, minute or hour, while the watch is running. The 256Hz square wave option is available independently of the watch function. The timing of the output pulse waveforms is shown in Fig. 6.

7.10 $\overline{SYNC}$ input

If the $\overline{SYNC}$ input is set low for longer than 200μs, the watch will synchronize to the falling edge of this $\overline{SYNC}$ signal with a precision of $\pm$2ms. The seconds register is cleared and, if the content is $\geq$30, the minutes register will be incremented.

7.11. Frequency tuning

The frequency of the oscillator can be tuned with the variable capacitor between XI and V_{DD}. A control signal in the form of a 256Hz square wave is available on the $\overline{PULSE}$ output (see 7.10.).

We recommend the use of ETA quartz crystals, and that the XI / XO pins are shielded with a ring connected to V_{DD}.

7.12. Test

From the various test features added to the M 3002, some may also be activated by the user. A first test mode can be entered by setting bits 7 and 5 high with bit 6 immaterial, leaving input $\overline{SYNC}$ high. All watch and timer data will increment in parallel at the rate of 1Hz depending on the status of bits 1 and 4 of the status word. To enter the second test mode, bit 7 of the status word must be set high, bits 5 and 6 set low, and then the $\overline{SYNC}$ input tied low. This will bypass the first 5 divider stages and connect pin XI directly to the 1kHz node of the divider chain, which must be then driven by a signal generator. At 32'678 Hz, the time counting will be speeded up by a factor of 32. Higher speeds can be achieved by speeding up the pulse generator. Modifying the status register as for the first test mode will combine both tests. To leave the test mode, set status bit 7 low. Every activation of $\overline{CS}$ will immediately exit the test mode, but the status word has to be properly rewritten.

Electrical Specifications

V_{DD} = 5V, T_A = 0 – 70°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Positive Supply Voltage	V_{DD}	wrt V_{SS}	2	5	5.5	V
Total Supply Current	I_{DD}	V_{DD} = 5V, Inputs at V_{DD} or V_{SS}		12	20	μA
		V_{DD} = 3V, Inputs at V_{DD} or V_{SS}		5	8	μA
Interface Lines						
Input High Voltage	V_{IH}		2.4		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		0.8	V
Output High Voltage	V_{OH}	I_{OH} = 2.0mA	2.4			V
Output High Voltage for $\overline{IRQ}$	V_{OH}	100k pull-up to V_{DD}	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	V
Input Leakage Current	I_L	$V_{SS} \leq V_{in} \leq V_{DD}$			1	μA
3-State HI-Z Leakage Current	$I_{HI\text{-}Z}$	OE or CS at V_{DD}			1	μA
Switching Characteristics		C_L = 50pF				
Chip Select Duration	t_{CS}	See Note	0.2			μs
Time between 2 Transfers	t_W		1.0			μs
Ram Access Time	t_{ACC}			0.15	0.2	μs
Data Valid to High Impedance	t_{DF}				0.18	μs
Data Settle Time	t_{DW}		0.2			μs
Data Hold Time	t_{DH}		0			μs
TE Response Delay	t_{TE}				0.18	μs
Oscillator						
Starting Voltage	V_{START}	C_T = 18pF	1.8			V
Input Capacitance	C_{IN}	V_{BATT} = 0		3.7		pF
Output Capacitance	C_{OUT}	V_{BATT} = 0		25		pF
Build up Time	T_{START}	C_T = 18pF		0.6	5	s
Stability	$\Delta f/f$	C_T = 5pF, $2V \leq V_{BATT} \leq 5V$		5	10	ppm/V
Crystal Characteristics						
Frequency	F			32,768		Hz
R_{Quartz}	R_q			40	60	kΩ
C_O	C_O			1.5		pF
C_I	C_I			1.7		fF
Trimmer Capacitance	C_T		5		40	pF

Note: $\overline{CS}$ glitches even shorter than 0.2μs may be recorded by the M 3003 and cause malfunction

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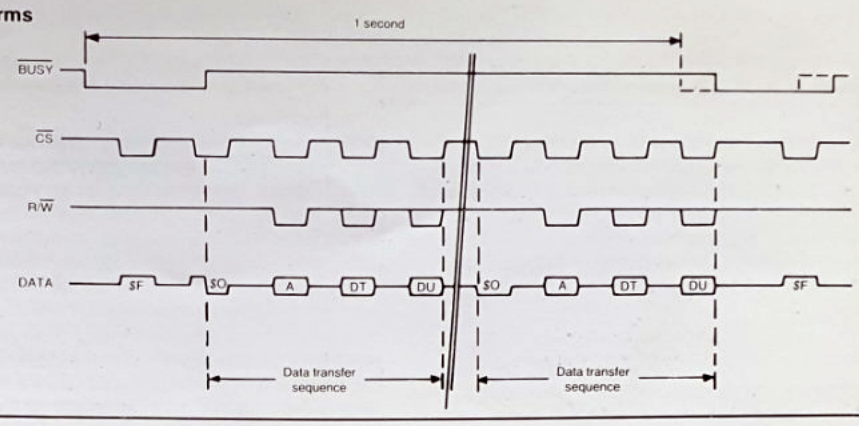
Transfer Waveforms



A = Address
DT = Data, tens
DU = Data, units

Fig. 4

Read Timing

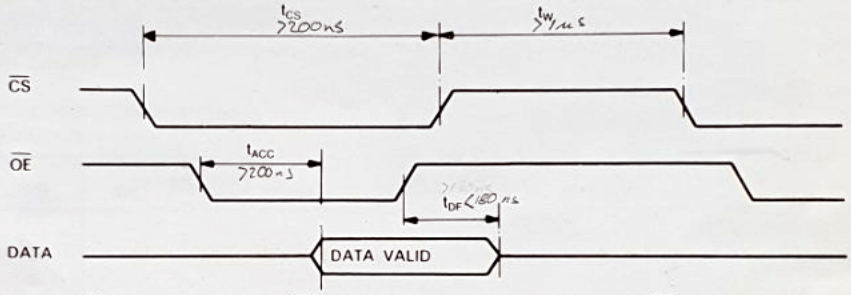


Fig. 5a

Note: If $\overline{CS}$ = 0 starts later than $\overline{OE}$ = 0, then t_{ACC} and t_{DF} are referred to $\overline{CS}$.

Write Timing

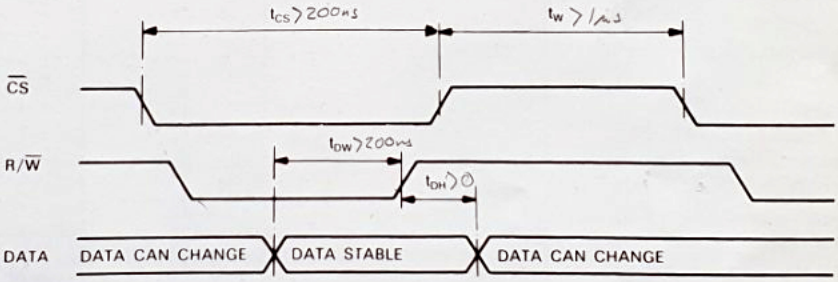
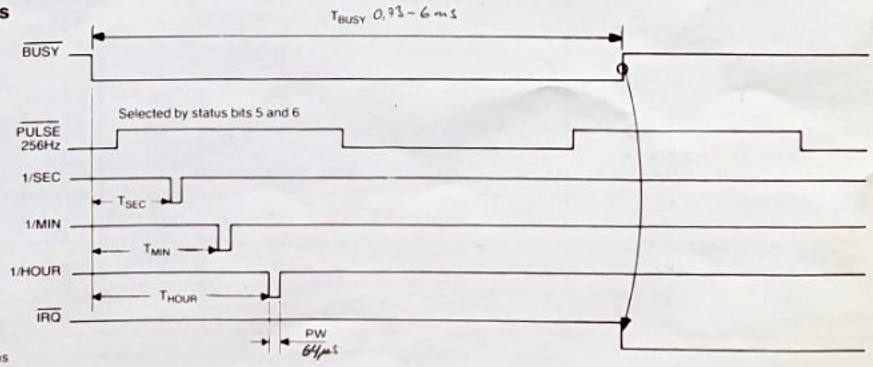


Fig. 5b

Note: If $\overline{CS}$ = 0 ends sooner than R/$\overline{W}$ = 0, t_{DW} and t_{DH} are referred to $\overline{CS}$.

Output Signals



T_{SEC} = 0.730ms
T_{MIN} = 1.04 to 1.16ms
T_{HOUR} = 1.34 to 1.58ms
T_{BUSY} = 0.73 to 6ms
PW = 64µs

Fig. 6

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8. Typical Application and Test Configuration

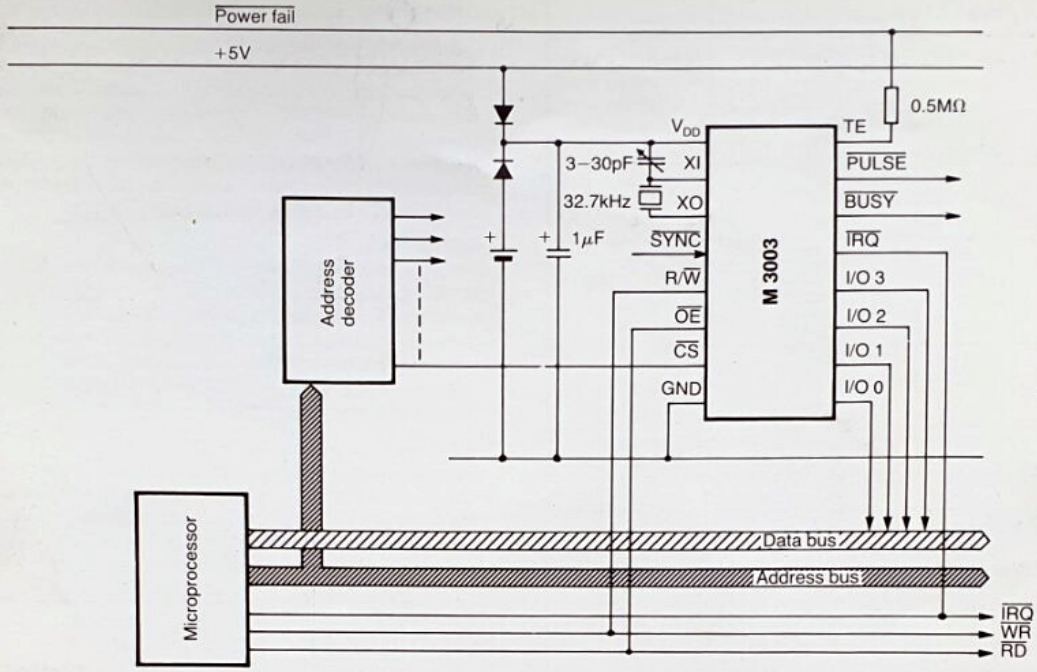


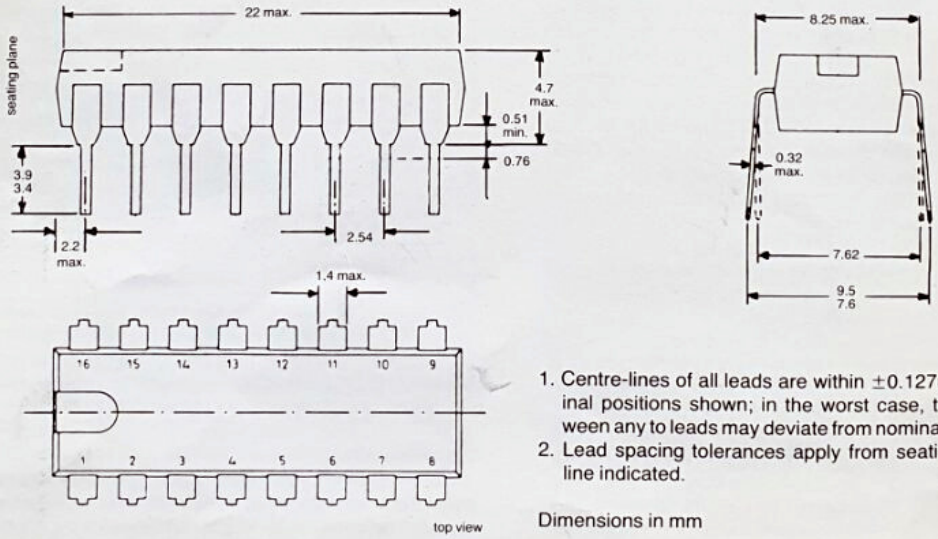
Fig. 7

9. Package and Ordering Information

The M 3003 is available in the following packages:

DIL 16 plastic package	M 3003 - 16 PI
SO 16W plastic package (wide)	M 3003 - 16 SI
TAB and other packages	on request

16-Lead Dual In-Line, Plastic



1. Centre-lines of all leads are within ±0.127mm of the nominal positions shown; in the worst case, the spacing between any to leads may deviate from nominal by ±0.254mm.
2. Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Fig. 8

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