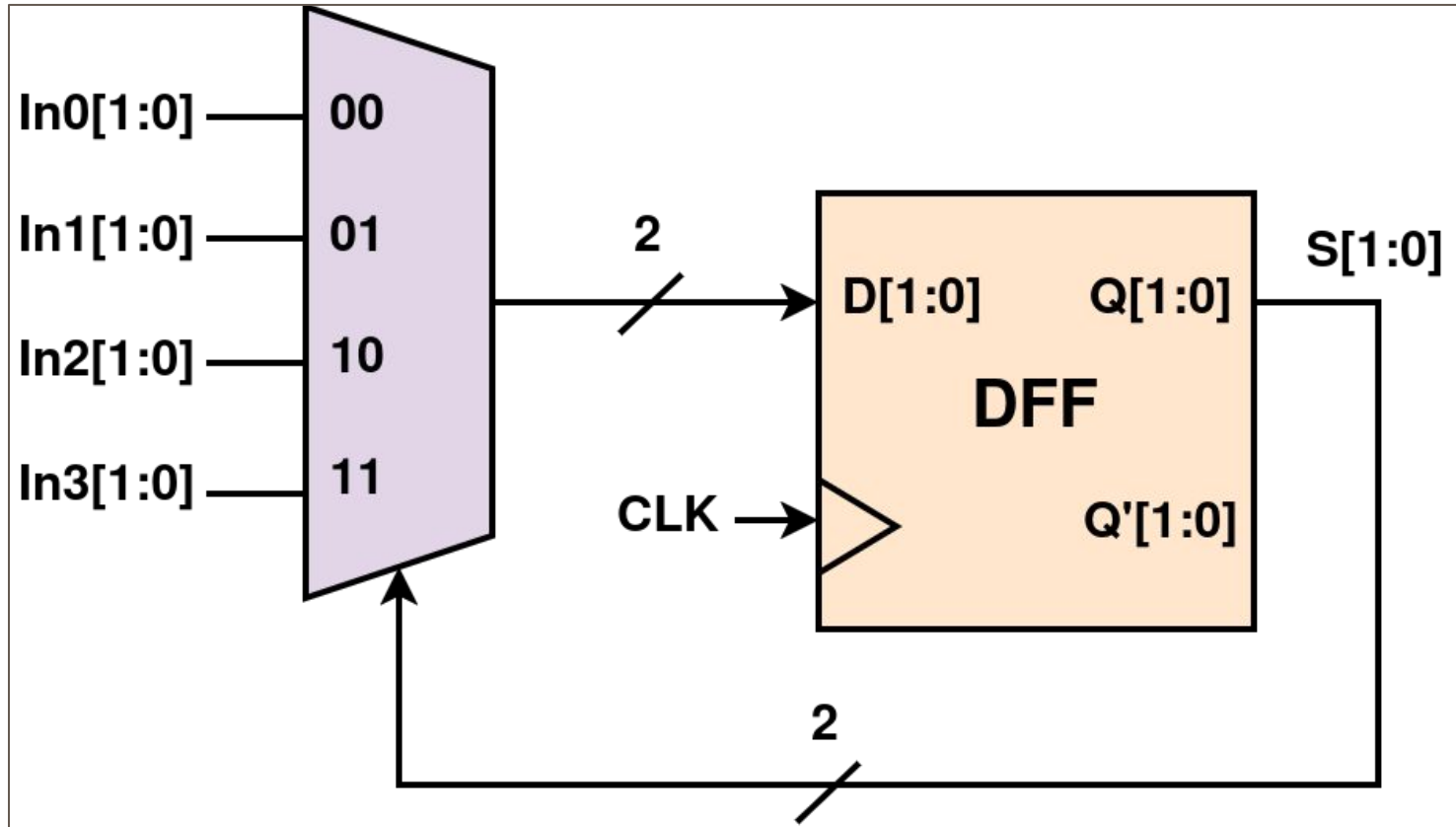


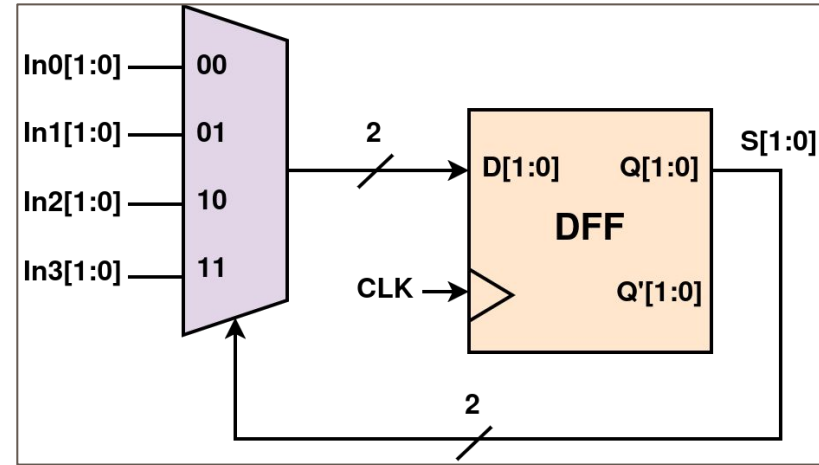
Self-Selecting Mux

Self-Selecting Clocked Mux!!



Some Questions to Ask

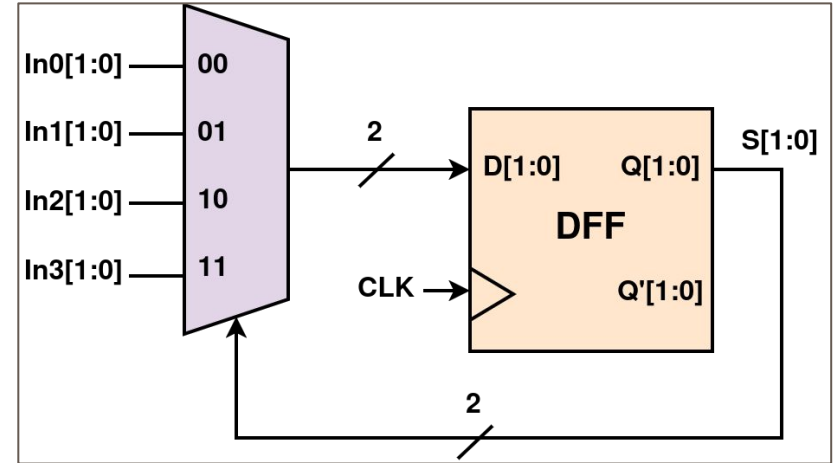
1. What is a DFF?
2. What is CLK?
3. What is the diagram even doing?
4. How many states exist in this circuit?
5. What are those states?



State Assignments

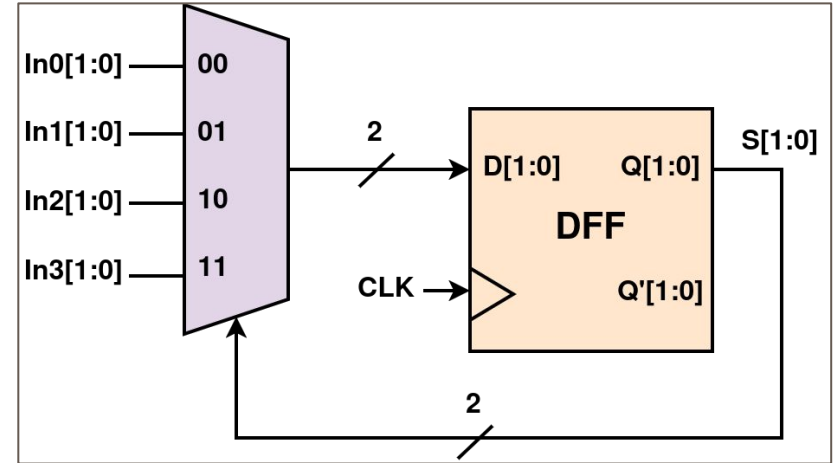
Build a State Assignment Table

State Bits		State Name
?	?	



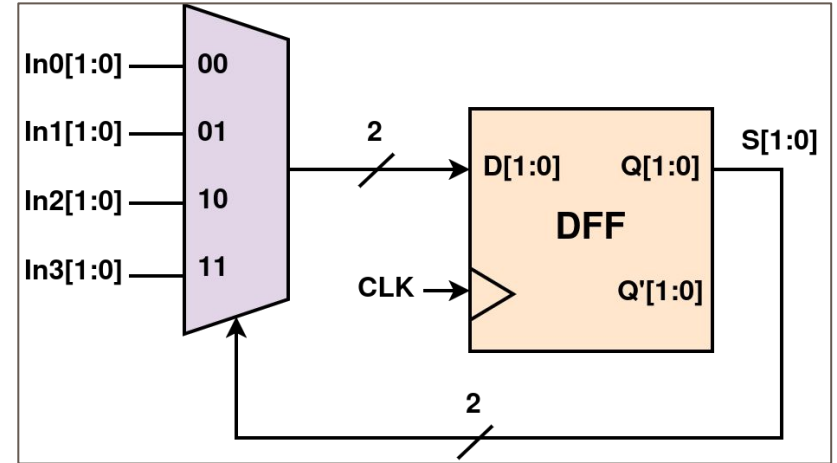
Build a State Assignment Table

State Bits		State Name
S[1]	S[0]	
?	?	
?	?	
?	?	
?	?	



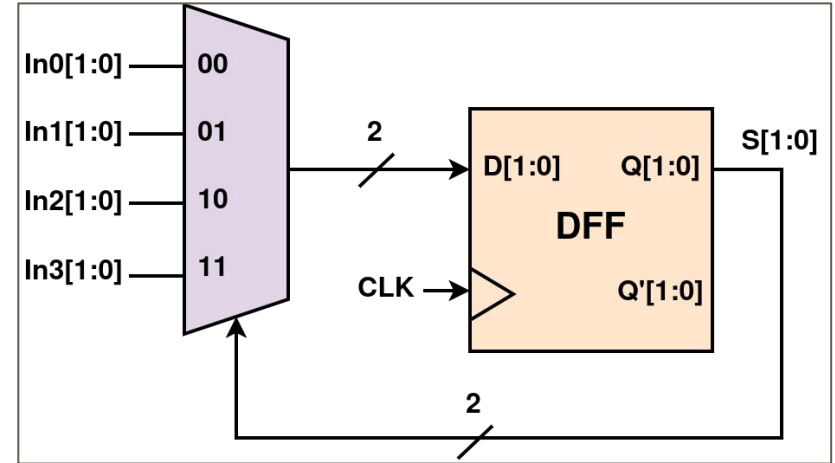
Build a State Assignment Table

State Bits		State Name
S[1]	S[0]	
0	0	?
0	1	?
1	0	?
1	1	?



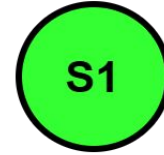
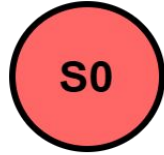
Build a State Assignment Table

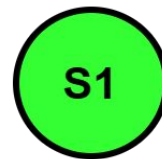
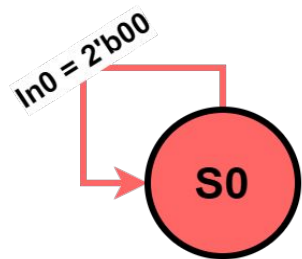
State Bits		State Name
S[1]	S[0]	
0	0	S0
0	1	S1
1	0	S2
1	1	S3

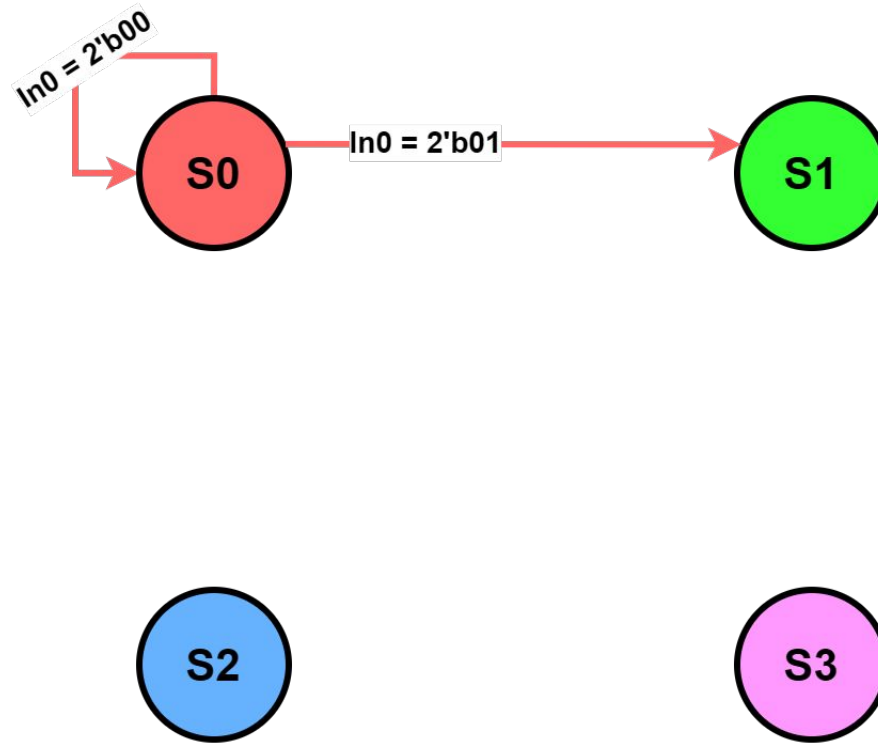


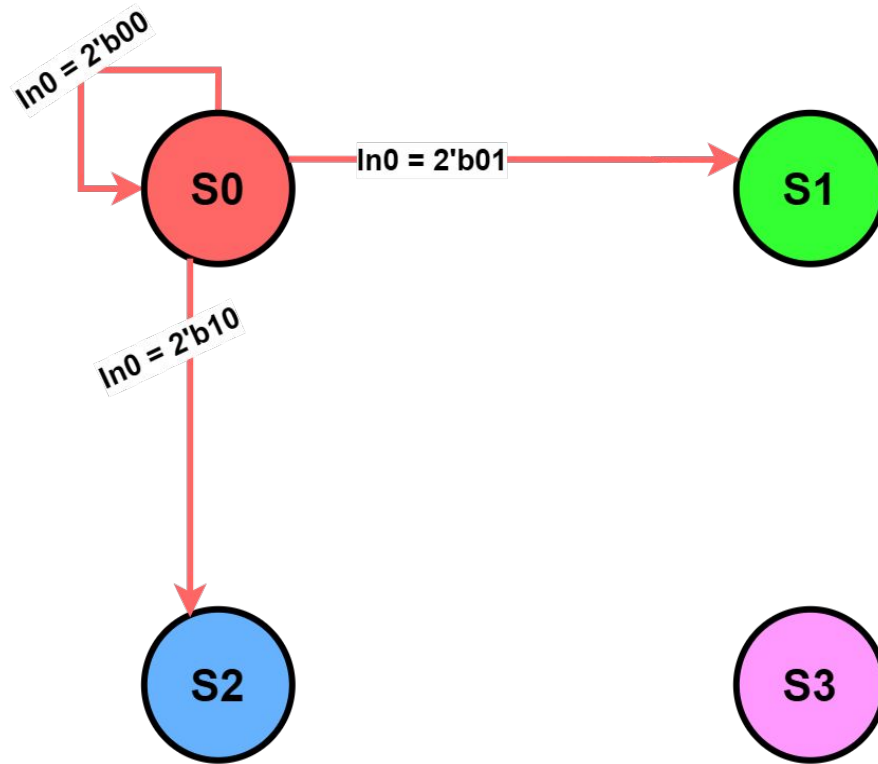
Constructing State Transition Diagram

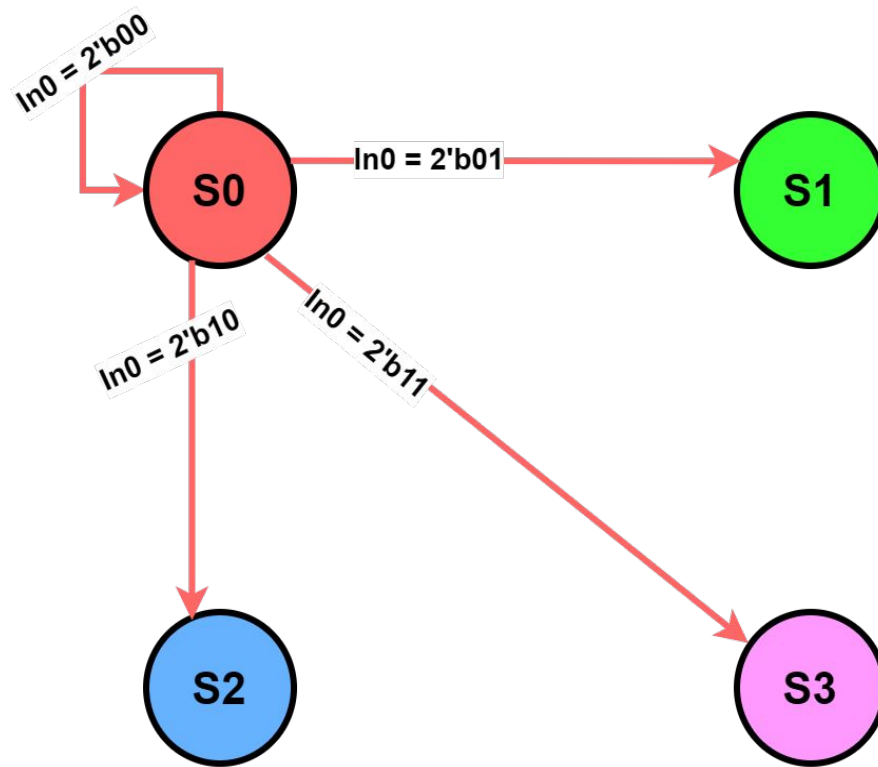
Let's Build a State Diagram

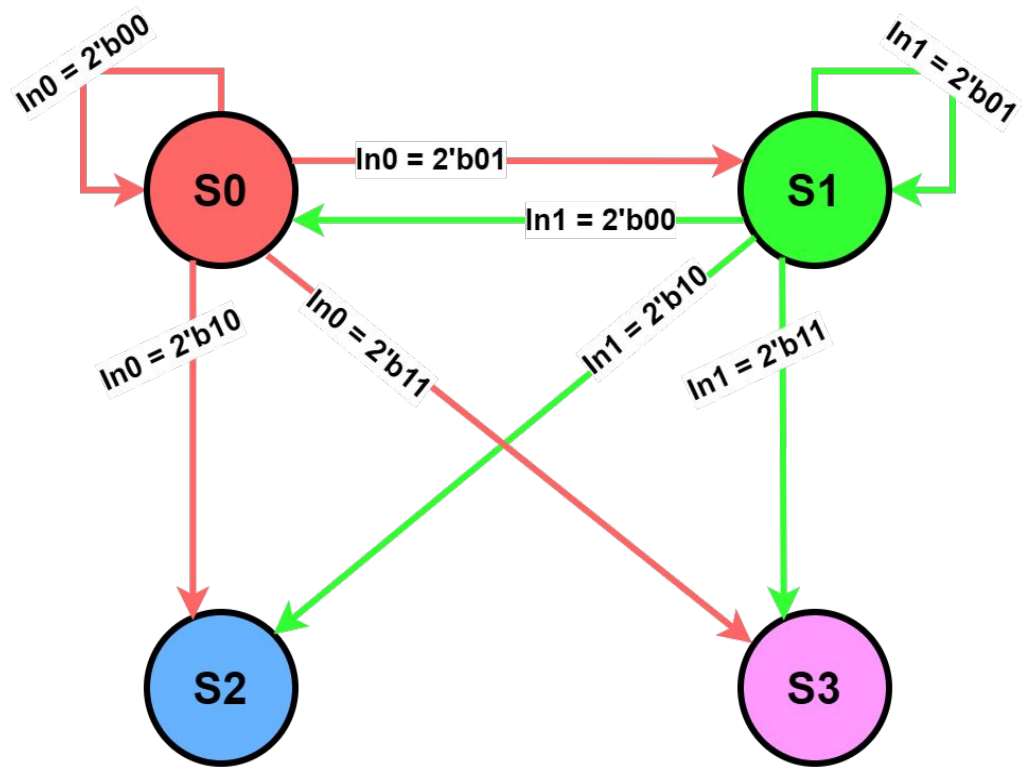


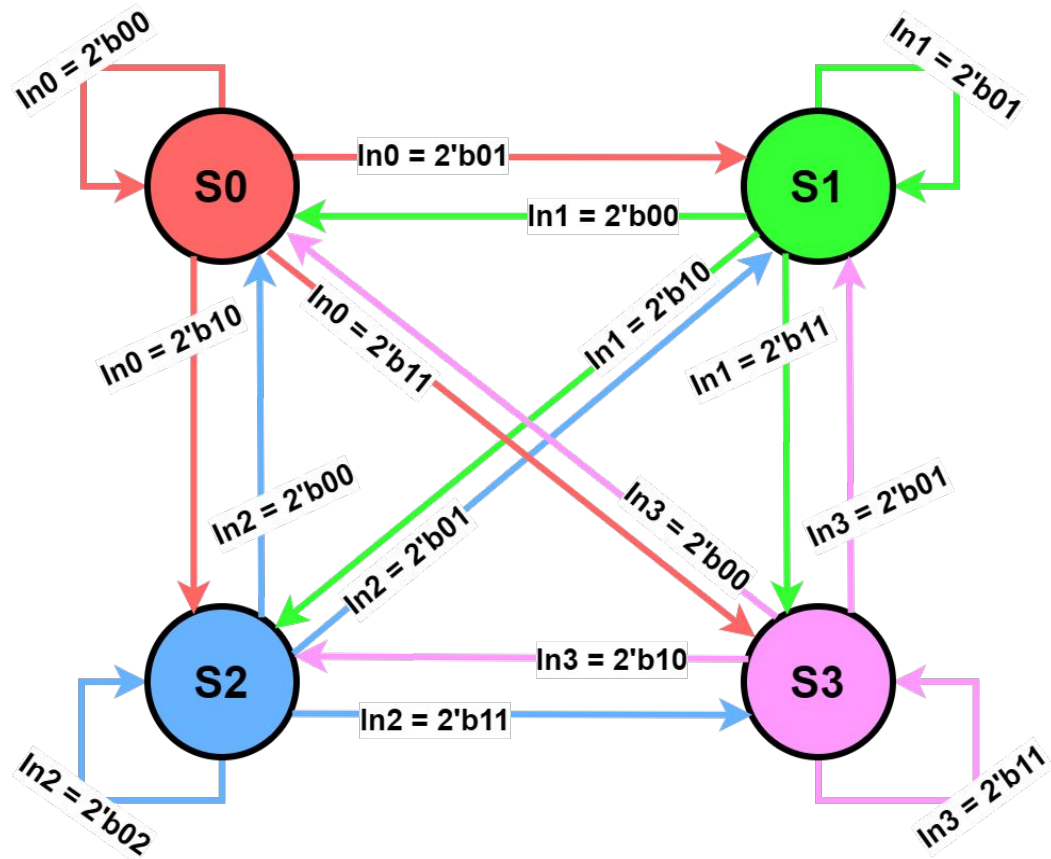








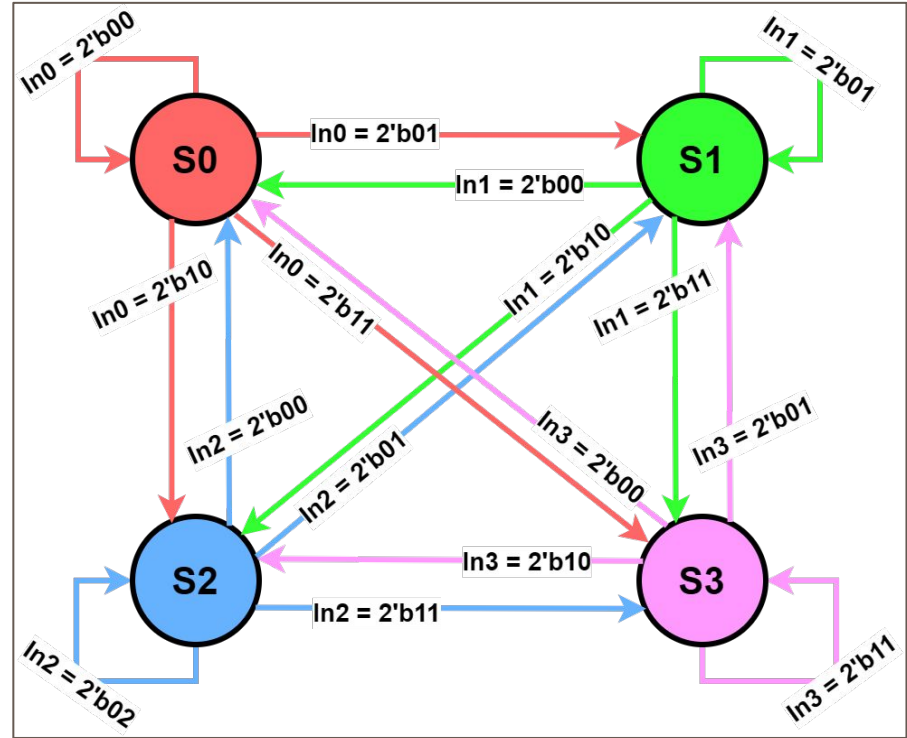




Generating High-Level Next State Equation

Generating High-Level Next State Equation

```
if (S = ??):  
    S+ = ??  
else if (S = ??):  
    S+ = ??  
else if (S = ??):  
    S+ = ??  
else:  
    S+ = ??
```



Generating High-Level Next State Equation

if ($S = S_0$):
 $S^+ = In_0$
else if ($S = S_1$):
 $S^+ = In_1$
else if ($S = S_2$):
 $S^+ = In_2$
else:
 $S^+ = In_3$

