EECS 270 W25
Discussion 9

March 20th, 2025

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1. Recap of Discussion 8 & Project 5
2. Our Processor’s Clock
3. Project 6 Overview
4. Team Project/Research!!!
5. Team Presentations

Recap of Discussion 8 & Project 5

Sequential Circuit Design Process

1. **Read the specs thoroughly to understand full behavior of system**

2. **BEFORE YOU START CODING ANYTHING, Construct:**
   a. State assignment
   b. State diagram
   c. State / Transition / Output table(s)
3. Generate logic equations for transition and output terms

4. **THEN, start your coding in Verilog**

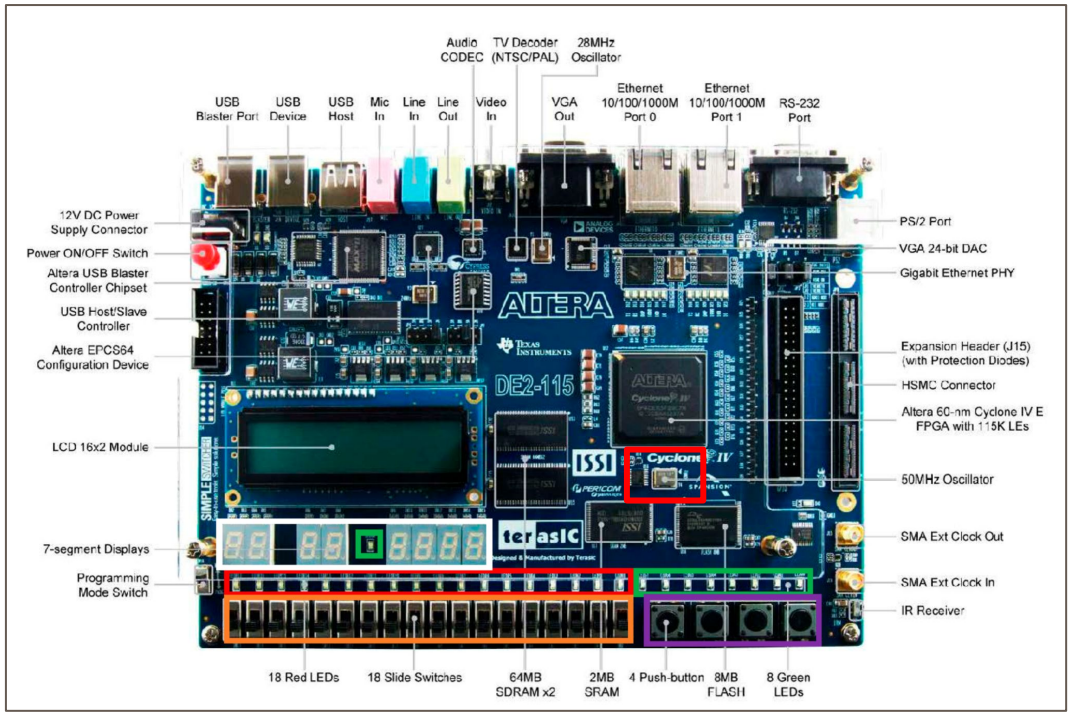
UpDown Counter (Project 5) Recap

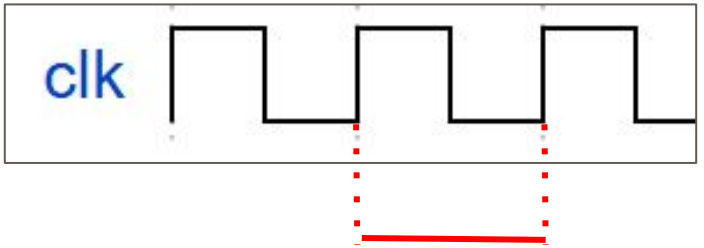
- Your first synchronous sequential circuit!
- Dealt with D Flip-Flops to handle synchronization
- Used the push button as our fake clock

Our Processor’s Clock

Clock Within Our FPGAs

- Our FPGAs come with a built-in 50 MHz Oscillator clock that we can utilize





Period (s) = 1 / f
= 1 / (50 MHz)
= 1 / (50 * 10^6 Hz)
= ((0.02) * 10^{-6}) s
= (2 * 10^{-8}) s
= (20 * 10^{-9}) s
= **20 ns**

How to Interact with the 50 Mhz FPGA Clock

- Declare ‘CLOCK_50’ as an input to your **Top-Level module**

```
module Project6
    (
        input CLOCK_50,           // Clock
        input [17:0] SW,                    // E =
        output [6:0] HEX7, HEX6, // Timer
        output [6:0] HEX3,                // ETL
        output [6:0] HEX2,                // NLTL
        output [6:0] HEX1,                // ELTL
        output [6:0] HEX0                 // WTL
    );

// Instantiate Clock_Div module

 // Instantiate TLC module

endmodule // Project6
```

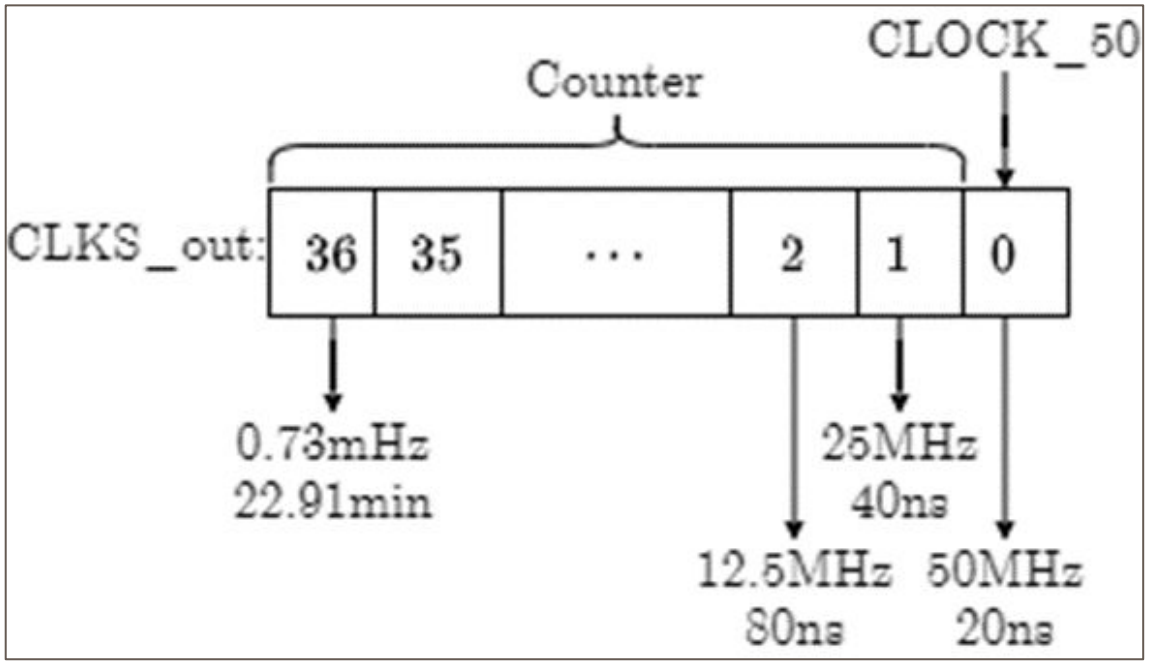
Using Clock_Div to Scale Down Clock

```
// Clock Divider by Powers of 2 (Table of frequ
module Clock_Div
    #(parameter SIZE = 36)  // divides by 2^i f
    (
        input CLK_in,
        output [SIZE:0] CLKS_out
    );

    reg [SIZE:1] Counter;
    initial Counter = 'd0;

    always @(posedge CLK_in)
        Counter <= Counter + 1;

    assign CLKS_out = {Counter, CLK_in};
endmodule // Clock_Div
```



Visualization on Clock_Div Module


```
    reg [SIZE:1] Counter;
    initial Counter = 'd0;

    always @(posedge CLK_in)
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    assign CLKS_out = {Counter, CLK_in};
endmodule // Clock_Div
```
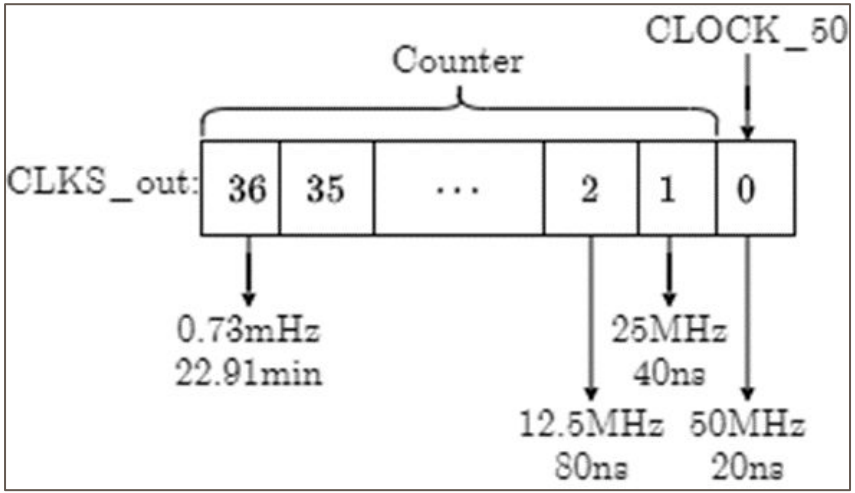
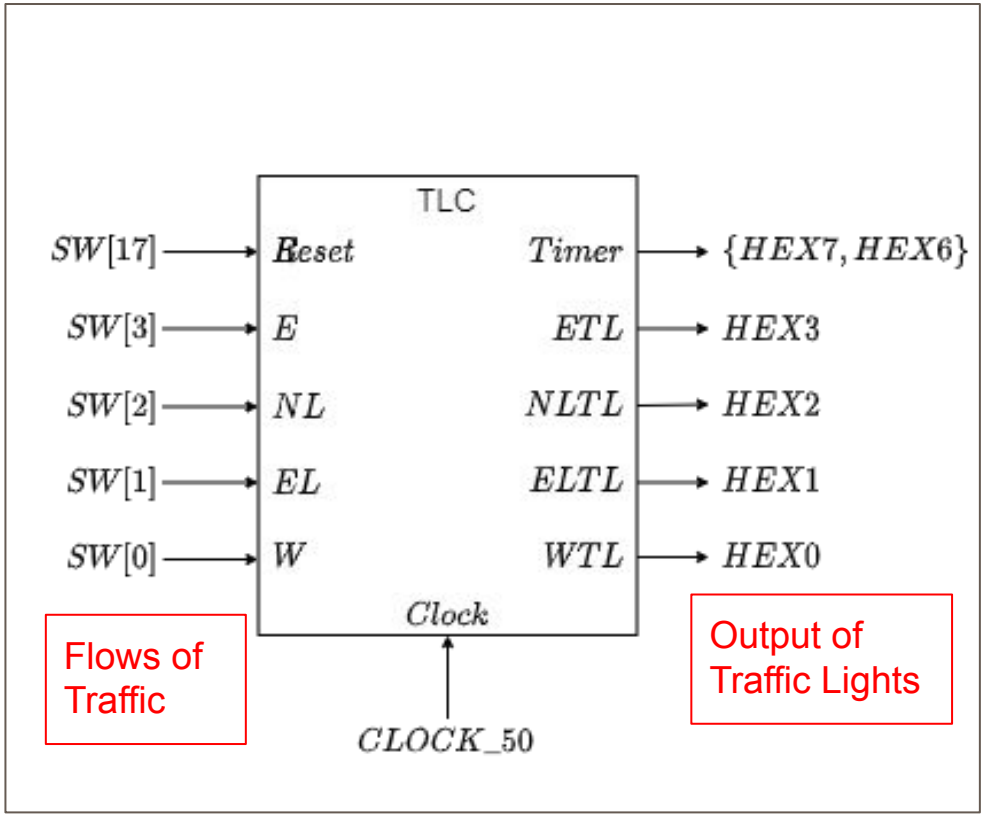
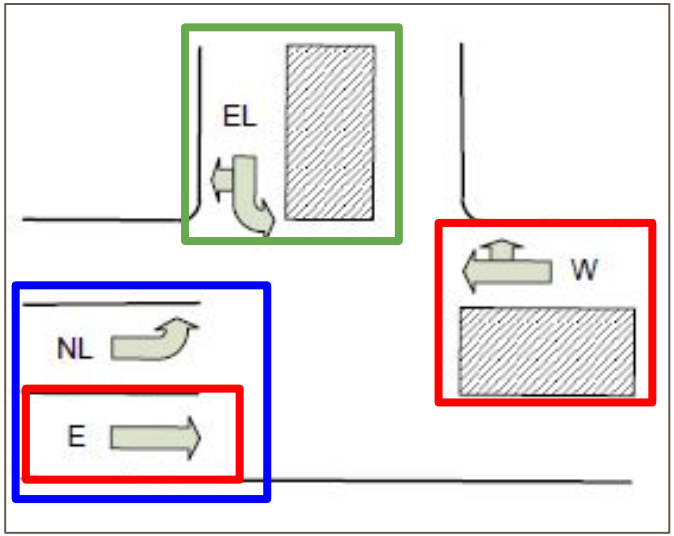



Project 6 (Traffic Light Controller) Overview

Project 6: Traffic Light Controller





FLOW A

FLOW B

FLOW C

Using the Clock for Project 6

Rule #1: A Green light should remain "Green" for intervals that are **multiples of 10 seconds**.

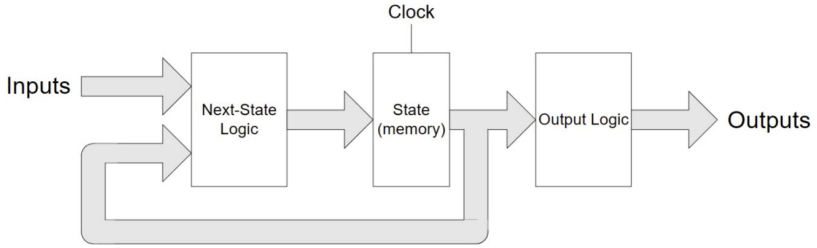
Rule #5a: When a light is to change from Green to Red, it **should be Yellow for exactly one second** in between the Green and Red.

How can you ensure that a light stays on for 1 or 10 seconds using the 50 MHz Clock?

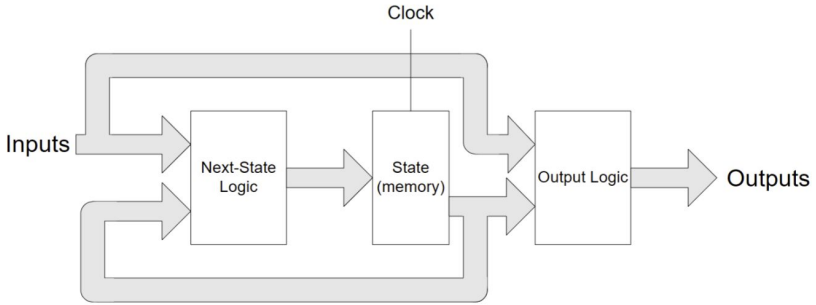
How much do you need to scale down the clock?

Are We Dealing with Moore/Mealy Outputs?

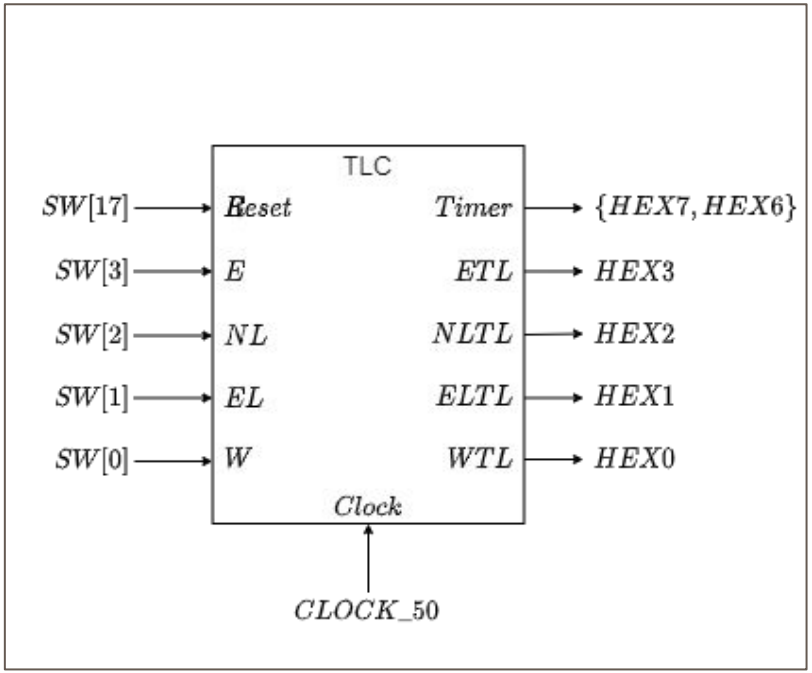
- **Moore Output**: output = g(current state)



- **Mealy Output**: output= g(current state, inputs)



States vs. Outputs of TLC



Starvation and Fairness in Project 6

- Need to ensure there is **no starvation**
  - **What do we mean by starvation?**
  - **How can starvation occur in this project?**

- Would also like to provide some sort of fairness as well

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FLOW A > FLOW B > FLOW C > FLOW A

Project 6: Traffic Light Controller

- **WARNING:** This project is extensive (Lots of specification to read)
  - Don’t wait to start it to the last day (Pleaseeeeee)

- Please read the specification thoroughly

- Refer back to Modelsim tutorials from previous discussion to get better at making your testbenches

Team Project/Research!!!

Team Project/Research

- **Everyone will be taking over discussion now!**

- Your job for the next 30-45 minutes
  1. Create groups of ~4-5 people (Come up with a team name)
  2. Choose one of the suggested projects/research to build/learn about
  3. Create a short presentation (5-minutes) of around 5-10 slides showcasing your work

- At the end, your group give your 5 minute presentation about the topic you worked on in front of the class

Possible Team Projects Ideas

- Verilog Projects
  - Ripple Counter
  - Parallel Counter (w/ Optional Enable, Load, Reset)
  - Johnson Counter (w/ Optional Enable, Load, Reset)
  - Universal Shift Register
  - Linear Feedback Shift Registers (LFSRs)
  - Continuous 3/4-bit Stream Sequence Detector
  - Continuous 4-bit Stream “Is One-Hot”
  - Willing to consider any other reasonable synchronous, sequential project ideas!

- Possible Research / Talks
  - The FPGA Design Flow (How does our Verilog code make it to the board?)
  - Similarity/Difference/Pros/Cons of another HDL (VHDL, SystemVerilog, …)
  - Where are FPGAs used today in industry and why

What I am Looking For in Your Project Presentation

- Description of what your project is about
  - What exactly is the behavior of your project?
  - What more could you add to your current implementation?

- Video/Live demonstration of LabsLand
  - **Use of a working clock and synchronous reset**

- (Optional) Clean ModelSim testing of many cases
  - Show snippets of your ModelSim output and label/point stuff out

- (Optional) Give quick related questions for class exercises
  - Ex. Given a counter in state XXXX, what will the next state be given X, X, and X

What I am Looking For in Your Research Presentation

- Discussion of your research topic
  - The who and what of your research
  - Any history behind the topic of your research
  - Is the product still being used today (if so, how and where)

- **Use of big visuals, the less words on the slides the better**

- Ending slide that cites the main resources you used
  - Allows students (and myself) to learn more about the topic you presented!

- Time for Open-Discussion Topics / Q&A
  - Will be okay with extending 5-minute time to allow for open discussion

Your Goal

- Make your presentation interesting and fun!!!

- Visuals, visuals, visuals
- Minimize words on your slides as much as possible

- Remember: You only have 5 minutes to present, so be smart about how you do it
  - Don’t need to go too in-depth about your topic
  - Have your live demos ready to go, maybe do videos of your demo instead
  - If you have time for a quick Q&A, great!

Team #1 (The Counters)

(Johnson Counter)

(People in Team)

Team #2 (Dave)

(Is One-Hot)

(People in Team)

Team #3 (Ripplers)

(Linear Shift Feedback Register)

(People in Team)

Team #4 (270 Warriors)

(Universal Shift Register)

(People in Team)