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Digital Logic Design

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# Selected Review questions

This problem set includes several exercises to help you study for exam2. Solutions to some of the problems will be discussed in the lab sessions on Nov 7th. You should review your class notes and try to work out the problems before the lab sessions.

**Selected Review Questions**

A.**Using MCI chip to realize a logic function**

**Exercise 1**

We want to design a circuit for a 3 input function F(A,B,C)=A'·C' + B·C + B'·C' using an 8 input one 1 bit multiplexer with an enable signal EN.

- First draw a truth table for F
- Use the truth to determine the input of the multiplexer

**Exercise 2**

We want to design a circuit for a 4 input function F(A,B,C,D)=A·C' + B·C'·D' + A·B'·C' using one 8-input (1 bit) multiplexer with an enable signal EN.

- First draw a truth table for F
- Use the truth to determine the input of the multiplexer

**Exercise 3**

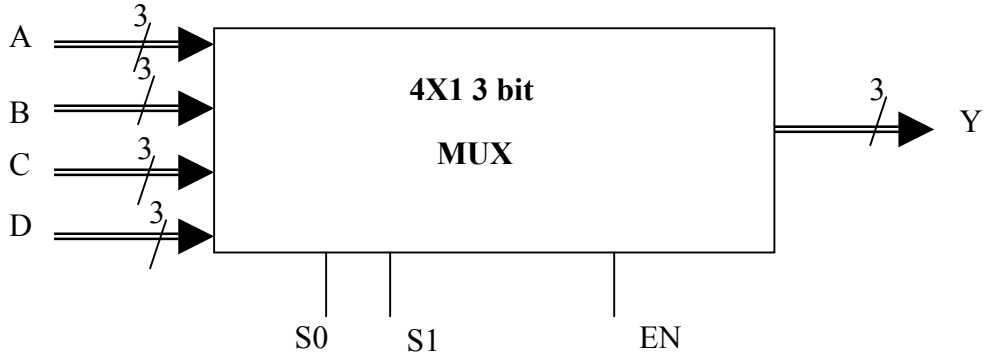
We want to implement the following 3 variables functions
F1 = AB + BC + A'B'
F2 = A'B' + AC

a) Implement the two functions using 3-to-8 one decoder.
b) Implement the two functions using 4-to-1 2 bit multiplexer (see 74X153 in text book)
c) Implement the two functions using a 3X2 (three input variables, two output) PLA with 6 product terms.

B.**Multiple bits and cascaded MCI**

**Exercise 1**

In class we have discussed n (=2, 4, 8, 16) inputs to 1 output multiplexers. The input and output are 1 bit variables. In practical applications input and output variables often have more than one bit. We wish to design a 4X1 3 bits multiplexers using 4X1 1 bit multiplexers. Ecah 1 bit multiplexer has 2 select lines and and enable signal. Design the following 4X1 3 bit MUX.



**Exercise 2**

a) Design an 8-to-1 multiplexer using 4-to-1 multiplexer.
b) Design a 4-to-16 decoder using 2-to-4 decoder. Repeat the same design using 3-to-8 decoders.

**Exercise 3**
1. Draw a truth table for a full adder, which has 3 input Xi, Yi and Ci-1 (carry in) and two output Si and Ci (carry out).
a) Design a circuit for Si as a function of Xi, Yi, Ci-1 using an 8-input multiplexer as the only component. Repeat the question for output Ci.
b) Design a circuit for S as a function of Xi, Yi , Ci-1 using a 4-input multiplexer and no more than one inverter. repeat the question for output Ci

2. Draw a truth table for a full subtractor, which has 3 input Xi, Yi and Bi-1 (borrow in) and two output Di and Bi (borrow out).

2.a) Repeat question 1.a above.
2.b) Repeat question 1.b above.

**Exercise 4. Expanding and cascading multiplexers.**
Expanding is used to expand and increase the number of input of multiplexers. For example if we need a 32-to-1 multiplexer, we can build it using use multipliers with smaller number of inputs. Discuss how the enable signal of the chips are used.
Design a 32-to1 MUX (provide for an enable signal) using

- 8-to-1 MUX and 2-to-4 decoders
- 8-to-1 MUX and 1-to-2 decoders
- 4-to-1 MUX and 2-to-4 decoders

C.**Iterative design**

**Exercise 1**
Use the full adder described above to design a 3 bit ripple adder; the initial carry $C_{-1}$ is set to 0. Illustrate the operation of the ripple adder on the following additions (X + Y):
a) X=110, Y=011 ; b) X=001, Y=011.
For each of the cases draw a timing diagram showing how the output S and C of the component adders evolve. Assume that each component adder has a timing delay $\Delta$.

**Exercise 2**
Repeat question 1 above using full substractors to design a 3 bit ripple substractor.
Compute the differences X-Y and give a timing diagram to illustrate the operation of the ripple substractor.