Switches, Transistors, Logic Gates, and Combinatorial Circuits

CS 350: Computer Organization & Assembly Language Programming

Lab 6, due Fri Mar 7

A. Why?

- On/off switches are a natural way to represent and control binary data.
- Transistors are switches.
- Logic gates are the lowest level of hardware that deal with logical values.
- Combinatorial logic circuits correspond to pure (state-free) calculations on booleans.

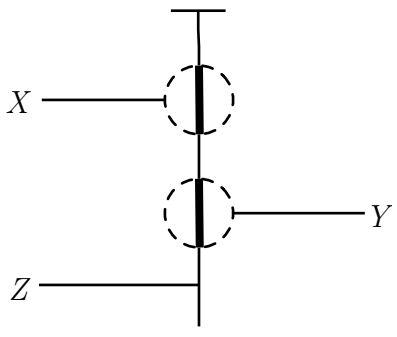
B. Outcomes

After this lab, you should be able to

- Be able to read and write simple voltage/current diagrams, transistor-level diagrams, and logic gates-level diagrams.
- Convert between truth tables, logical formulas, and loop-free logic circuits.
- Be able to analyze/draw the circuitry for simple arithmetic/logical calculations.

C. Problems [100 points total]

1. [16 = 4*4 pts] Shown here is a voltage-level diagram for the partial circuit from the previous problem, when $\overline{X}\ \overline{Y} = 1$. (I.e, $X = Y = 0$.)

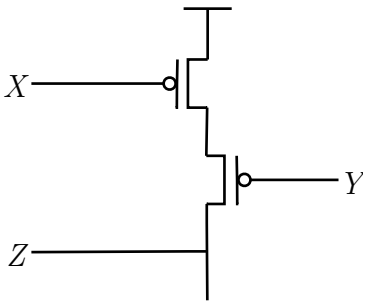
   

   (a) Complete the voltage diagram using the transistors from your solution to the previous problem. (Don't forget to mark which switches are open or closed.)

   Draw three more copies of your voltage-level

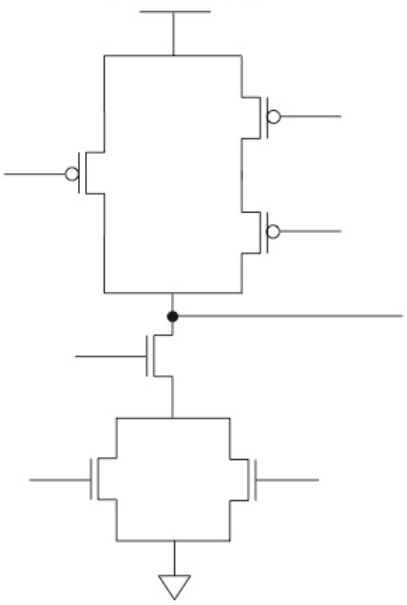
diagram and indicate which switches are open or closed when (b) $X\ \overline{Y} = 1$, (c) $\overline{X}\ Y = 1$, and (d) $X\ Y = 1$.

2. [9 pts] The transistor-level diagram shown here is supposed to calculate $Z = \overline{X}\ \overline{Y}$, but it's incomplete: Add wires and transistors so that Z is connected to ground exactly when $X + Y$ holds.

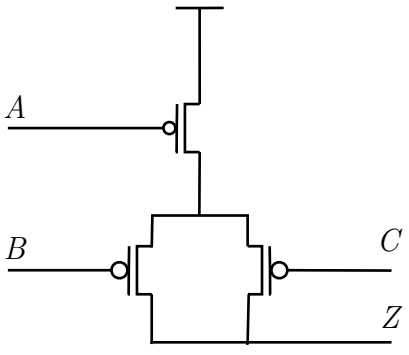


3. [9 pts] (Exercise 3.8, p.85) The transistor-level shown here implements $Y = \overline{A} + \neg(B + C)$. Label the inputs to all the transistors; also, label the output Y.

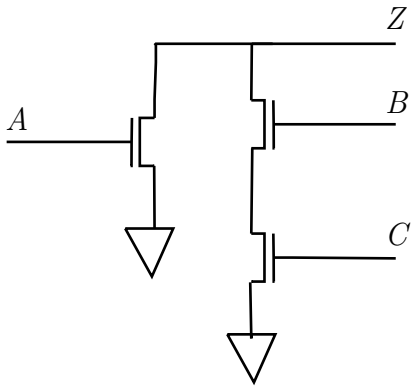
Notes: Some copies of the text have a typo: They leave out the *NOT* in $\neg(B + C)$. Also, the natural reading of the circuit is $\overline{A} + \overline{B}\ \overline{C}$.



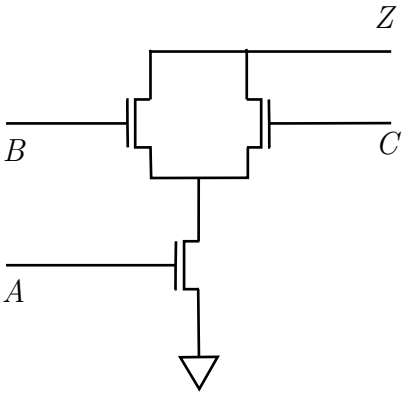
4. [3 pts] When does the partial circuit to the right connect Z to power?



5. [9 = 3*3 pts] (a) When does the partial circuit to the right connect Z to ground? (b) If we connect this partial circuit to the partial circuit from Question 4, do we get a legal circuit? (c) If so, what does it calculate? If not, when does it have a short circuit or open circuit?



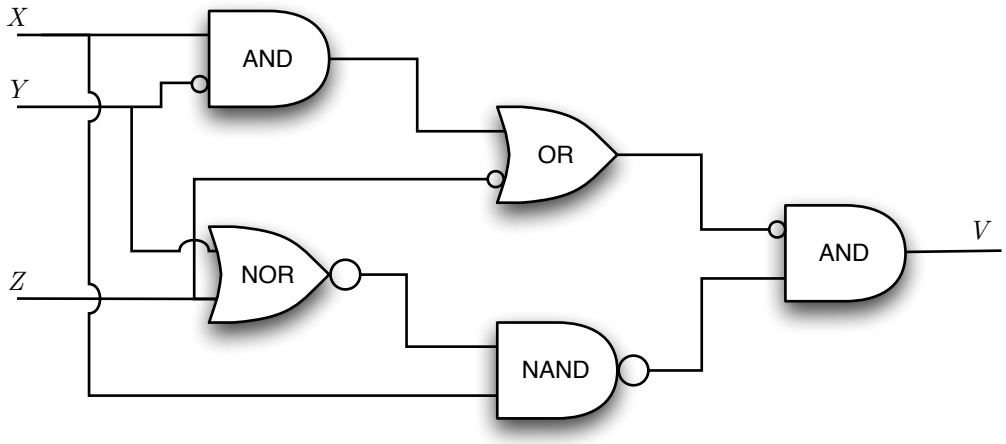
6. [9 pts] Repeat Question 5 on the partial circuit to the right.



7. [16 = 8+8 pts] Draw a transistor-level circuit for $Z = \overline{A}\,(\overline{B} + \overline{C})\,\overline{D}$. Be sure to (a) Connect output Z and power iff $\overline{A}\,(\overline{B} + \overline{C})\,\overline{D}$ is true; also (b) Connect ground and output Z iff $\overline{A}\,(\overline{B} + \overline{C})\,\overline{D}$ is false.

   (In addition, don't forget which transistors need to be p-type and which need to be n-type.)

8. [16 = 4*4 pts] Consider the circuit below with inputs X, Y, Z and output V.



(a) Translate the logic circuit to get a boolean expression definition for V.

(b) Draw a PLA-based logic circuit for V. Feel free to drop unused AND gates, but keep 3 inputs per AND gate. If you want, include a truth table.

(c) Write a Karnaugh map for V and use it to find a simplest equivalent boolean expression definition for V.

(d) Draw a logic circuit for the V using the simplified definition.

9. [13 = 3 + 10 pts] Exercise 3.24: [The figure on the next page] shows a block-level logic circuit that appears in many of today's processors. Each of the boxes labelled "+" is a full-adder circuit. [(a)] What does the value on the wire X do? That is, what is the difference in the output of this circuit if $X = 0$ versus if $X = 1$? (b) Modify the logic diagram below so that implements an adder/subtracter. That is, the logic circuit will compute $A + B$ or $A - B$ depending on the value of X. [Hint: Replace each C_i with a circuit that uses B_i and possibly other inputs.]

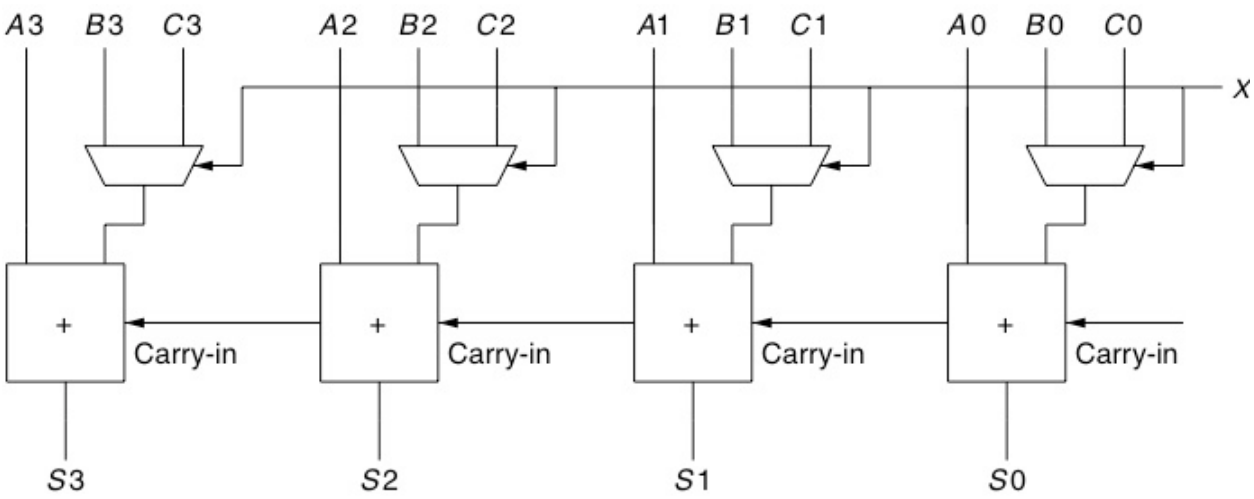


Figure for Exercise 3.24

