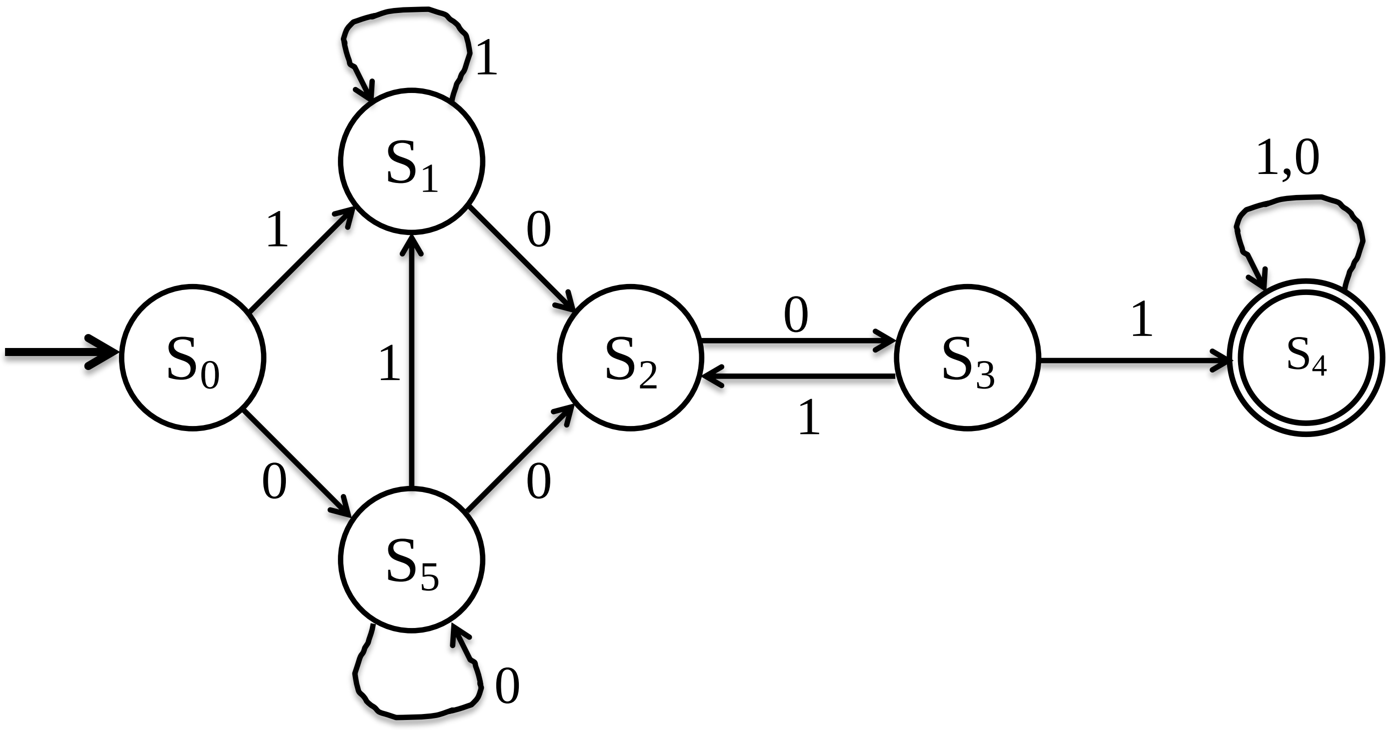
1.
   a) $a' = \bar{a} + S$
   b) The circuit has a logically stable value for a when iff S=1 and a=1
   c) Yes, this circuit can be used to remember a bit of 1.
2.
   a) $Q' = (D + Q)(D + \bar{S})(S + Q)$
   b) The circuit has logically stable values for Q:
      i. Q=0 and D=0
      ii. Q=0 and S=0
      iii. Q=1 and D=1
      iv. Q=1 and S=0
   c) Yes, this circuit can be used to remember a bit. D = 1 and S=1 and Q=0, then Q=1; D=0 and S=1 and Q=1, then Q=0.
3. Address size = 0, addressability = 32
4. Address size = 12, addressability = 24
5. Diagram:



Transition table:

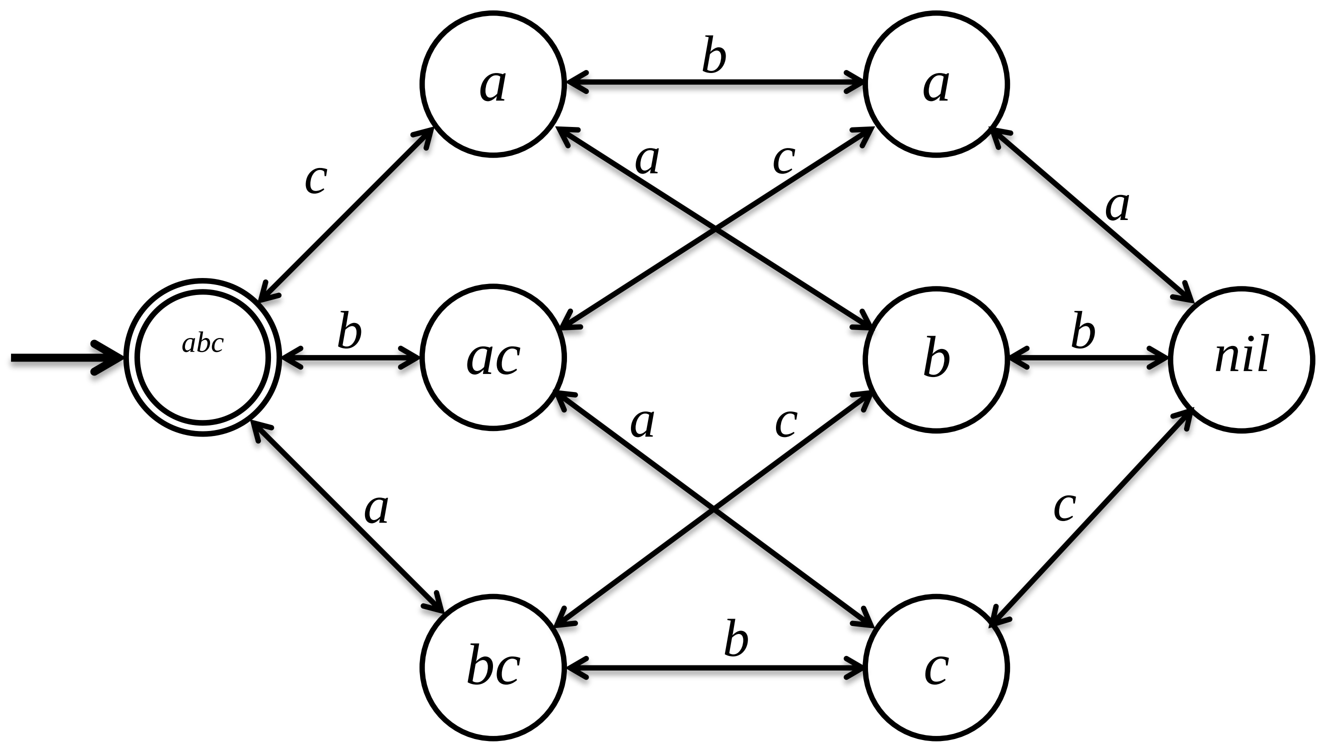
State	Input	New State
S_0	*0*	S_5
S_0	*1*	S_1
S_1	*0*	S_2
S_1	*1*	S_1
S_2	*0*	S_5
S_2	*1*	S_3
S_3	*0*	S_2
S_3	*1*	S_4
S_4	*0*	S_4
S_4	*1*	S_4
S_5	*0*	S_5
S_5	*1*	S_1

Initial State: S_0*; Accepting State:* S_4

Trace of Execution:

	0		*1*		*0*		*1*		*0*		*1*		*1*		*0*	
S_0		S_5		S_1		S_2		S_3		S_2		S_3		S_4		S_4

6. Diagram:



Transition table:

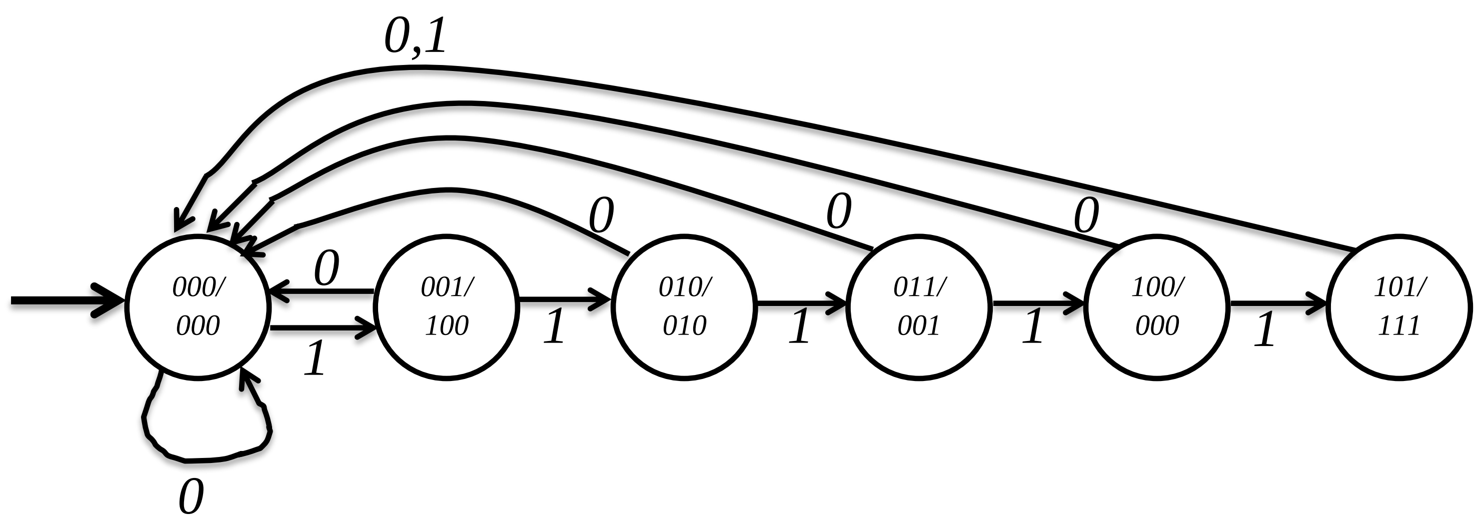
State	Input	New State
abc	*a*	*bc*
abc	*b*	*ac*
abc	*c*	*ab*
bc	*a*	*abc*
bc	*b*	*c*
bc	*c*	*b*
ac	*a*	*c*
ac	*b*	*abc*
ac	*c*	*a*
ab	*a*	*b*
ab	*b*	*a*
ab	*c*	*abc*
c	*a*	*ac*
c	*b*	*bc*
c	*c*	*None*
b	*a*	*ab*
b	*b*	*None*
b	*c*	*bc*
a	*a*	*None*
a	*b*	*ab*
a	*c*	*ac*
None	*a*	*a*
None	*b*	*b*
None	*c*	*c*

Initial State: abc; Accepted State: abc

Trace of Execution:

	a		*b*		*a*		*c*		*b*		*c*			c		a		b		a		c	
abc		*bc*		*c*		*ac*		*a*		*ab*		*abc*	abc		ab		b		None		a		ac

7. Diagram:



Transition table:

State	Input	New State
000 / 000	*0*	*000 / 000*
000 / 000	*1*	*001 / 100*
001 / 100	*0*	*000 / 000*
001 / 100	*1*	*010 / 010*
010 / 010	*0*	*000 / 000*
010 / 010	*1*	*011 / 001*
011 / 001	*0*	*000 / 000*
011 / 001	*1*	*100 / 000*
100 / 000	*0*	*000 / 000*
100 / 000	*1*	*101 / 111*
101 / 111	*0*	*000 / 000*
101 / 111	*1*	*000 / 000*

Initial State: 000 / 000

Logic expressions:

I_0, I_1, I_2 stand for current state, S'_0, S'_1, S'_2 stand for new state, and L_0, L_1, L_2 stand for light's on or off.

$L_0 = S\,(I_0\overline{I_1}\,\overline{I_2} + I_0\,\overline{I_1}\,I_2)$

$L_1 = S\,(\overline{I_0}\,I_1\,\overline{I_2} + I_0\,\overline{I_1}\,I_2)$

$L_2 = S\,(\,I_0\,I_1\overline{I_2} + I_0\,\overline{I_1}\,I_2)$

$S'_0 = S\,(\overline{I_0}\,\overline{I_1}\,\overline{I_2} + \overline{I_0}\,I_1\,\overline{I_2} + \overline{I_0}\,\overline{I_1}I_2)$

$S'_1 = S\,(\,I_0\overline{I_1}\,\overline{I_2} + \overline{I_0}\,I_1\,\overline{I_2})$

$S'_2 = S\,(\,I_0\,I_1\overline{I_2} + \overline{I_0}\,\overline{I_1}I_2)$