* 1. The circuit has a logically stable value for a when iff S=1 and a=1
  2. Yes, this circuit can be used to remember a bit of 1.
  3. The circuit has logically stable values for Q:
     1. Q=0 and D=0
     2. Q=0 and S=0
     3. Q=1 and D=1
     4. Q=1 and S=0
  4. Yes, this circuit can be used to remember a bit. D = 1 and S=1 and Q=0, then Q=1; D=0 and S=1 and Q=1, then Q=0.

1. Address size = 0, addressability = 32
2. Address size = 12, addressability = 24
3. Diagram:  
     
   Transition table:

1

0

1

1

1

0

0

0

0

1

1,0

|  |  |  |
| --- | --- | --- |
| State | Input | New State |
| *S0* | *0* | *S5* |
| *S0* | *1* | *S1* |
| *S1* | *0* | *S2* |
| *S1* | *1* | *S1* |
| *S2* | *0* | *S5* |
| *S2* | *1* | *S3* |
| *S3* | *0* | *S2* |
| *S3* | *1* | *S4* |
| *S4* | *0* | *S4* |
| *S4* | *1* | *S4* |
| *S5* | *0* | *S5* |
| *S5* | *1* | *S1* |

*Initial State: S0; Accepting State: S4*

Trace of Execution:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | *0* |  | *1* |  | *0* |  | *1* |  | *0* |  | *1* |  | *1* |  | *0* |  |
| *S0* |  | *S5* |  | *S1* |  | *S2* |  | *S3* |  | *S2* |  | *S3* |  | *S4* |  | *S4* |

1. Diagram:

*c*

*b*

*b*

*a*

*c*

*a*

*c*

*a*

*b*

*a*

*b*

*c*

Transition table:

|  |  |  |
| --- | --- | --- |
| State | Input | New State |
| *abc* | *a* | *bc* |
| *abc* | *b* | *ac* |
| *abc* | *c* | *ab* |
| *bc* | *a* | *abc* |
| *bc* | *b* | *c* |
| *bc* | *c* | *b* |
| *ac* | *a* | *c* |
| *ac* | *b* | *abc* |
| *ac* | *c* | *a* |
| *ab* | *a* | *b* |
| *ab* | *b* | *a* |
| *ab* | *c* | *abc* |
| *c* | *a* | *ac* |
| *c* | *b* | *bc* |
| *c* | *c* | *None* |
| *b* | *a* | *ab* |
| *b* | *b* | *None* |
| *b* | *c* | *bc* |
| *a* | *a* | *None* |
| *a* | *b* | *ab* |
| *a* | *c* | *ac* |
| *None* | *a* | *a* |
| *None* | *b* | *b* |
| *None* | *c* | *c* |

*Initial State: abc; Accepted State: abc*

Trace of Execution:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | *a* |  | *b* |  | *a* |  | *c* |  | *b* |  | *c* |  |  | c |  | a |  | b |  | a |  | c |  |
| *abc* |  | *bc* |  | *c* |  | *ac* |  | *a* |  | *ab* |  | *abc* | abc |  | ab |  | b |  | None |  | a |  | ac |

1. Diagram:

*1*

*0*

*0,1*

*0*

*1*

*1*

*1*

*1*

*0*

*0*

*0*

Transition table:

|  |  |  |
| --- | --- | --- |
| State | Input | New State |
| *000 / 000* | *0* | *000 / 000* |
| *000 / 000* | *1* | *001 / 100* |
| *001 / 100* | *0* | *000 / 000* |
| *001 / 100* | *1* | *010 / 010* |
| *010 / 010* | *0* | *000 / 000* |
| *010 / 010* | *1* | *011 / 001* |
| *011 / 001* | *0* | *000 / 000* |
| *011 / 001* | *1* | *100 / 000* |
| *100 / 000* | *0* | *000 / 000* |
| *100 / 000* | *1* | *101 / 111* |
| *101 / 111* | *0* | *000 / 000* |
| *101 / 111* | *1* | *000 / 000* |

*Initial State: 000 / 000*

Logic expressions:

I0, I1, I2 stand for current state, S’0, S’1, S’2 stand for new state, and L0, L1, L2 stand for light’s on or off.