Miguel (Mico) Santiago

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github.com/micodocious Interim Secret Clearnace

Education

Oregon State University *Sept 2019 – June 2024*
BS in Electrical & Computer Engineering, Minor in Computer Science

- GPA: 3.6/4.0 Focus: CS, FPGA, Embedded, Verilog, Verification

Experience

Computer Engineer *Point Mugu, CA*
NAVAIR NAWCWD *Sept 2024 – Current*

- Under Test & Evaluation at NAVAIR, first rotation with E71 Mission Modules at NAVSEA.
- Identified and resolved duplicate IP addresses in two MPPCE RAID servers, eliminating duplicate network responses. This fixed USV latency issues and GUI duplication, enabling regression testing.
- Identified a transmission line issue caused by a broken console inside the LCS, by recognizing one-way communication, signal integrity using a Fluke device, and ping tests in the console during anti mine mission package installation.
- Transitioned from two-way ranging to multilateration in the Game of Drones tracking system by assigning unique IDs to each anchor and modifying the position engine to use the equation on Multilateration on Wiki, resulting in accurate and scalable tag localization.

Embedded Engineering Intern *Tualatin, OR*
Schneider Electric *Jun 2023 – Dec 2023*

- Utilized an oscilloscope to debug RS232 during HDPM6000 regression testing, demonstrating to third-party contractors that the issue was with their driver. This led to the deployment of the correct driver version and a calibrated three-phase power supply.

Product Engineering Intern *Wilsonville, OR*
Siemens EDA *Mar 2022 – Sep 2022*

- Debugged Python code for generating heat maps from an n x n matrix, reducing execution time from six hours to three minutes by recording data output time to identify the root cause and collaborating with the library's creator on a solution.
- Created a Python script to aggressively test a data collection tool by automating unit tests for error detection on user input to a table, enabling a four-week, round-the-clock sprint that successfully met a two-month deadline.

Professional Tennis Player *Internationally*
ATP Tour *2012 – 2017*

- Former top 50 American mens tennis player. Achieved men's world ranking of 684 (2015.09.14) only which six Oregon natives have achieved.

Projects

Memory Controller Creation and Verification

- Identified and debugged a testbench issue during early-stage memory controller verification, where incorrect use of data type logic instead of bit in randomization for assertion testing and coverpoints impacted coverage. Resolved the issue, increasing test coverage Increasing test coverage from $< 30\%$ to 100%.
- Tools Used: HDL, Verilog, ModelSim, System Verilog, Questa, Cadence JaspurGold.

ALU Creation in Virtuoso

- In ROM, using logic gates in my P-ROM caused it to be much slower, implementing a PLA. Reduced 21 transistors compared to 100+ transistors and resulted in 30ns faster or 7x faster speeds.
- Tools Used: Cadence, Virtuoso

References

- NAVSEA SSA Engineering Lead Dominick Ballesteros: dominick.b.ballesteros.civ@us.navy.mil
- NAVSEA MPAS Engineering Lead Leo Sotto: leonardo.v.sotto.civ@us.navy.mil
- NAVAIR Game of Drones Lead Alberto Izarraraz: alberto.izarraraz.civ@us.navy.mil