Miguel (Mico) Santiago

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Interim Secret Clearnace

Education

Oregon State University *Sept 2019 – June 2024*
BS in Electrical & Computer Engineering, Minor in Computer Science

- GPA: 3.6/4.0 (link)

Experience

Computer Engineer *Point Mugu, CA*
NAVAIR NAWCWD *Sept 2024 – Current*

- Integrated and installed software on Littoral Combat Ships (LCS) using Unix tools, ensuring on-time embarkation to save taxpayers millions. (Video on LCS)
- Integrated hardware and software for Mine Countermeasures (MCM) USVs on Hunt and Sweep boats, ensuring functionality in half the allotted deadline. (Video on MCM USV)
- Conducted regression testing for MCM USVs from the Mission Package Computing Environment (MPCE), identifying IP and cabling issues, saving tens of thousands in future tests. (Link to LCS MM Fact Sheet)
- Completed Acquisition, Systems Engineering, Test & Evaluation, and Basic Electronic Warfare training in 5 months instead of 2 years, gaining a strong understanding of NAVAIR engineering objectives to support the warfighter.
- Hired to work in Test & Evaluation at NAVAIR, first rotation with E71 Mission Modules at NAVSEA.

Undergrad Lab Assistant (ULA) for Digital Logic Design Class *Corvallis, OR*
Oregon State University *Mar 2024 – Jun 2024*

- Performed lab help and checkoffs of material pertaining to projects involving programming the DE-10 FPGA with Quartus, simulating test benches with ModelSim, building projects with K-Maps and the RTL with Verilog.

Embedded Engineering Intern *Tualatin, OR*
Schneider Electric *Jun 2023 – Dec 2023*

- Developed a testbench for HDPM6000, a modular power monitoring solution with Ethernet communication, waveform capture, and data logging. Conducted regression testing using a three-phase power source, documented findings, and published results on the official website. Weekly scrums.

Product Engineering Intern *Wilsonville, OR*
Siemens EDA *Mar 2022 – Sep 2022*

- Developed an automated testbench for a data collection tool in machine learning using Python in a Unix environment. Bridged R&D and customer teams, debugging code for presentations and contributing to the creation of Calibre nmDRC Recon, which uses ML to predict design rule violations. Team used Agile.

Professional Tennis Player *Internationally*
ATP Tour *2012 – 2017*

- Former top 50 American mens tennis player. Achieved men's world ranking of 684 (2015.09.14) only which six Oregon natives have achieved. (link)

Projects

Memory Controller Creation and Verification *github.com/name/repo*

- Created a memory controller in System Verilog. Ran Code & Functional Coverage. Ran System Verilog Assertions. Ran Formal Property Verification. Made TCL scripts to a set of commands inside JaspurGold.
- Tools Used: HDL, Verilog, ModelSim, System Verilog, Questa, Cadence JaspurGold.

Synchronized Desktop Calendar *github.com/name/repo*

- Developed a desktop calendar with globally shared and synchronized calendars, allowing users to schedule meetings with other users
- Tools Used: C#, .NET, SQL, XML