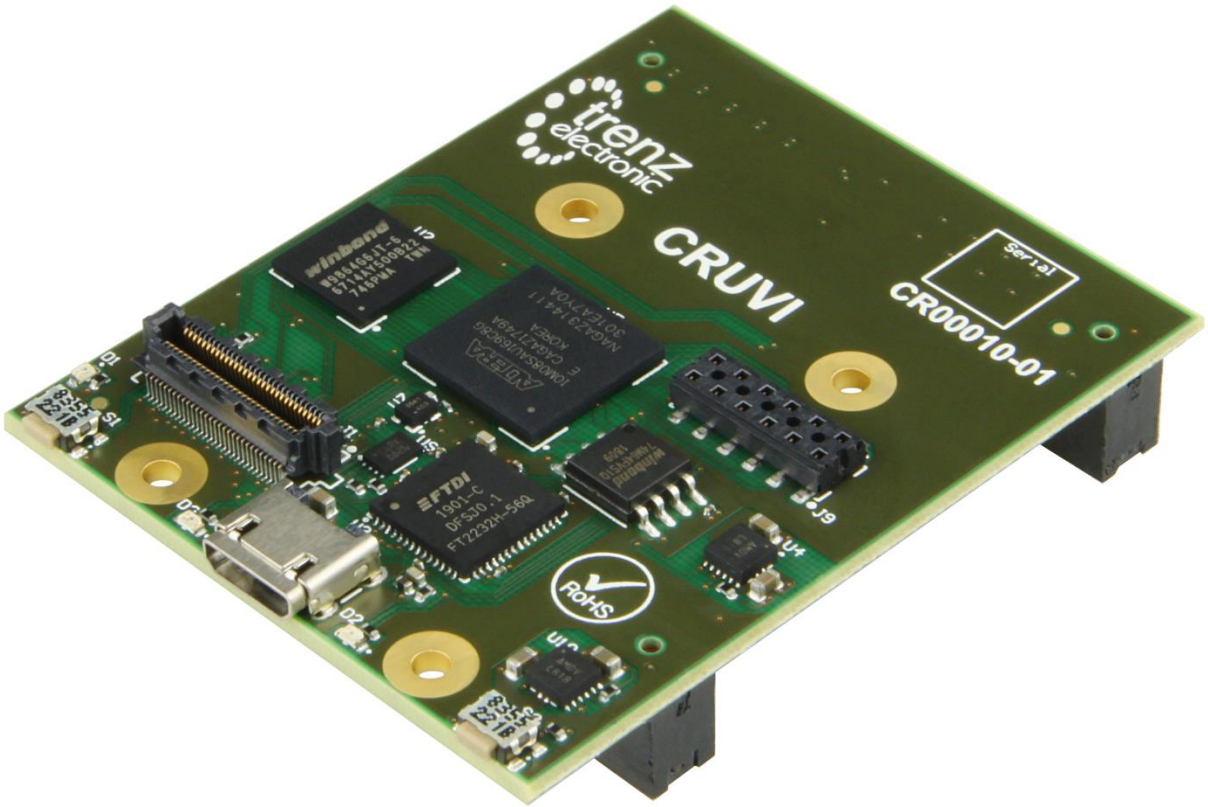
CRUVI

Draft Version 1.0.3-alpha

December 9, 2020



Introduction

The purpose of this standard is to create an open ecosystem of function modules. Main focus is on support for FPGA's and FPGA SoC devices.

Objectives

The initial design was driven by following constraints

- Mechanically fixed (mounting holes)
- Cost optimized variants
- Size:
  - two modules must fit "inside" VITA 57.1 FMC Card
  - size scaling
  - B2B connector mating height: 5mm max
- Front panel accessible I/O Connectors, optimized for connector density
- Variable I/O Voltage
- High speed transceiver support (option 1 to 4 lanes)
- I^2C/SMBUS Support (with ALERT/IRQ)
  - Plug & Play EEPROM (optional, recommended)
- Predefined I/O mappings, for relevant interfaces
  - QSPI/OctalSPI/xSPI/eSPI
  - SDIO/eMMC
  - NAND
  - HyperBus (HyperRAM/Flash)
  - LVDS ADC (1 to 4 data lane)
  - FTDI FIFO (8 bit)
  - ULPI
- Recommended Differential pair mapping for FPGA with unidirectional LVDS
- "Ecosystem friendly" – adaptable to existing ecosystem with adapters
- Standard heatsink available

Contributors

Name	**Company**
Helmut Plötz	Arrow
Paul Gardner-Stephen	Flinders University
Benjamin Gittins	Synaptic Laboratories Ltd
Antti Lukats	MicroFPGA UG
Matthew Burns	Samtec
Edmund Humenberger	Symbiotic EDA
Thorsten Trenz	Trenz Electronic GmbH

Electrical

CRUVI 1.0 does specify two board-to-board connectors: HS (High Speed) and LS (Low Speed).

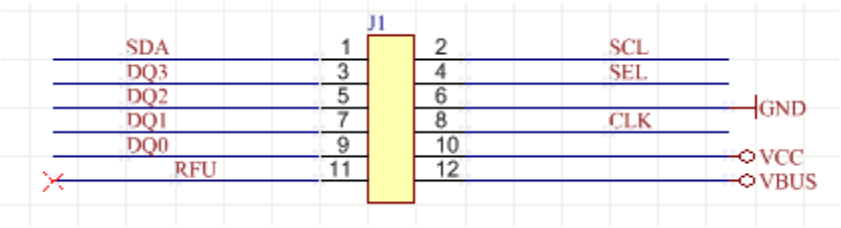
There may be more connector types defined in future specification releases.

Detailed CRUVI Pinouts are currently maintained in Google doc spreadsheet.

LS Connector

LS (Low Speed) connector, this is low profile (5mm mating height) 12-pin header with 2mm spacing.

Pin	Primary Function	Notes
1	SDA	If I2C supported then pullup on the module
2	SCL	If I2C supported then pullup on the module
3	D3	
4	SEL	Chip select
5	D2	
6	GND	
7	D1	
8	CLK	Primary clock/strobe
9	D0	
10	VCC	3.3V nominal (some host may support variable voltage)
11	RFU	Reserved for future use, do not connect to anything
12	VBUS	5V nominal (optional power supply)



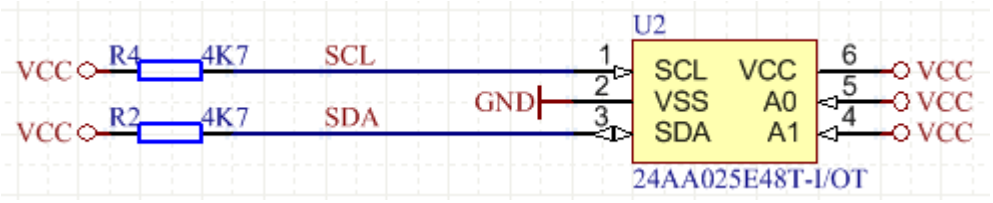
Example schematic for LS connector (SPI + I2C). Other mappings are possible as defined in online google pin mapping document.

I2C Bus

Modules that implement I2C function should use fixed pins for the bus.

Identification EEPROM

It is recommended to have I2C EEPROM for module identification. Some modules may however use the I2C pins for other purposes (GPIO, etc.).



Recommended EEPROM type 24AA025E48, this EEPROM includes unique identifier from factory. Address bits should be pulled high. I2C pullups must be on the module. I2C Address is 1010_011x.

This EEPROM provides 128 Bytes for user data (128 upper bytes include the EUI-64 identifier).

I/O Voltage

There is no separate I/O voltage pin, so the I/O voltage should be same as the main supply VCC (nominal at 3.3V). If VCC is lower than 3.3V then the I/O voltage should scale with it.

Power Supply Requirements

Most modules require only power from VCC pin. Some LS modules may also work at 2.5 or 1.8V if supplied with lower VCC. Some baseboards may support variable VCC for LS slots. VBUS (nominal voltage 5V) is optional; many modules do not use or require it.

PMoD compatibility

CRUVI LS modules have same amount of I/O as PMoD. With simple passive adapter CRUVI LS modules can be used with any PMoD host boards. A fixed IO mapping between CRUVI and PMoD exists; all adapters should use this mapping. Note: not all CRUVI modules will map to same PMoD electrical signals when using an adapter.

Feature	**CRUVI**	**PMoD**
Main supply voltage VCC	3.3V	3.3V
VBUS 5V supply	Optional	No
Number of I/O pins	8	8
Connector	12 pin 2 mm header	12 pin 100 mil header
Mechanical fixture	One or two mounting holes	No mounting holes
Module max width	22 mm	800 mil
Module to module spacing	900 mil	900 mil
I2C identification EEPROM	Option	no

HS Connector

HS connector provides 28 I/O in Adjustable power domain (maximum 12 LVDS) and 9 I/O in fixed 3.3V power domain.

Pin	Label/Function	VCCIO	Note
1	RFU		
3	ALERT/IRQ	VCC	If interrupt supported then pullup on the module
5	SDA	VCC	If I2C supported then pullup on the module
7	SCL	VCC	If I2C supported then pullup on the module
9	VCC		+3.3V
11	REFCLK	VCC	
13	GND		
15	B0_P	VADJ	
17	B0_N	VADJ	
19	GND		
21	B1_P	VADJ	
23	B1_N	VADJ	
25	GND		
27	B2_P	VADJ	
29	B2_N	VADJ	
31	GND		
33	B3_P	VADJ	
35	B3_N	VADJ	
37	GND		
39	B4_P	VADJ	
41	B4_N	VADJ	
43	GND		
45	B5_P	VADJ	
47	B5_N	VADJ	
49	GND		
51	DI/TDI	VCC	DI or TDI
53	DO/TDO	VCC	DO or TDO
55	SEL/TMS	VCC	Select or TMS
57	MODE	VCC	JTAG enable/mux or mode pin
59	SCK/TCK	VCC	Clock or TCK
2	HSIO	VADJ	
4	VCC		+3.3V
6	HSO	VADJ	
8	HSRST	VADJ	Peripheral reset if supported
10	HSI	VADJ	
12	GND		
14	A0_P	VADJ	
16	A0_N	VADJ	
18	GND		
20	A1_P	VADJ	
22	A1_P	VADJ	
24	GND		

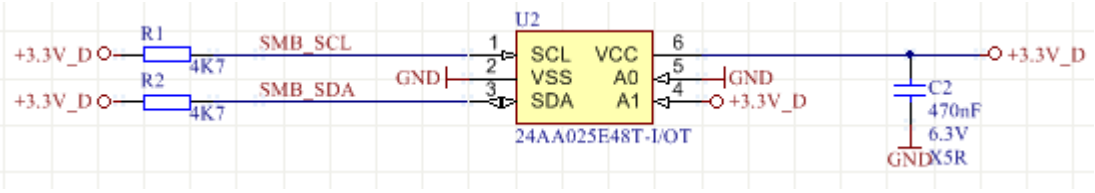
26	A2_P	VADJ	
28	A2_N	VADJ	
30	GND		
32	A3_P	VADJ	
34	A3_N	VADJ	
36	VADJ		VCCIO Adjustable (1.2V … 3.3V)
38	A4_P	VADJ	
40	A4_N	VADJ	
42	GND		
44	A5_P	VADJ	
46	A5_N	VADJ	
48	GND		
50	RFU		
52	RFU		
54	GND		
56	RFU		
58	RFU		
60	VBUS		5V nominal

RFU (Reserved for Future Use) pins should remain unconnected on modules and bases.

I2C/SMBus

The standard defines three pins (SCL/SDA/ALERT) for I2C bus or SMBUS devices. All pullups should be on the module. It is not recommended to use those pins for any other purpose. There should be no pin sharing between module slots on the baseboards.

Identification EEPROM



Recommended EEPROM type 24AA025E48, this EEPROM includes unique identifier from factory. Address bits A1, A0 should be set to high and low. I2C Address is 1010_010x.

This EEPROM provides 128 Bytes for user data (128 upper bytes include the EUI-64 identifier).

JTAG

If JTAG is implemented it shall be at fixed location with 3.3V I/O voltage. If JTAG muxing (enable) is implemented this shall also be at fixed location.

I/O Voltage

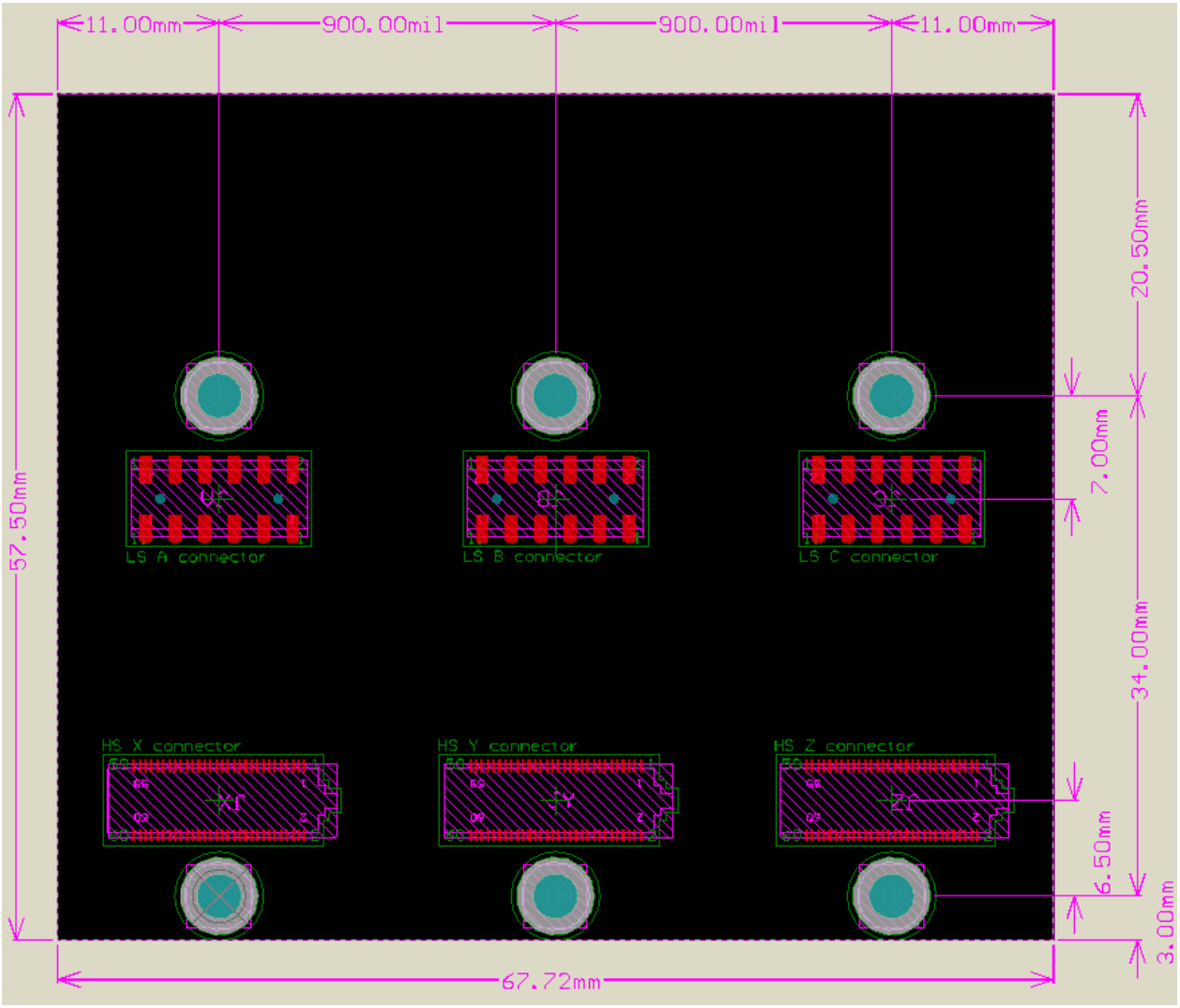
The main functional pins are in adjustable power domain, useable voltages depend on the module and/or carrier. Not all combinations of module to carrier will be compatible. Some modules and carrier may only support one fixed IO voltage.

Power Supply Requirements

Main supply VCC has nominal voltage 3.3V. Module I/O voltage (VADJ) is provided separately in the range 1.2 to 3.3V. Optional VBUS supply has nominal voltage of 5V. Modules that use main power as I/O voltage should take power from the adjustable I/O Voltage and not from VCC.

Mechanical

Maximum size triple module/base dimensions:

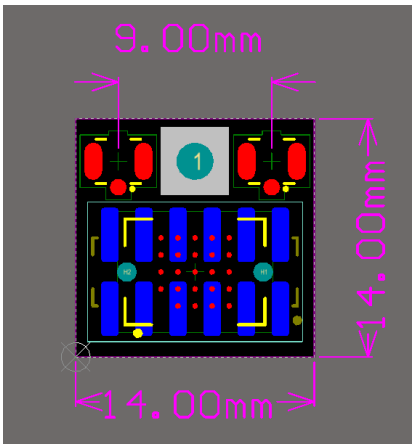


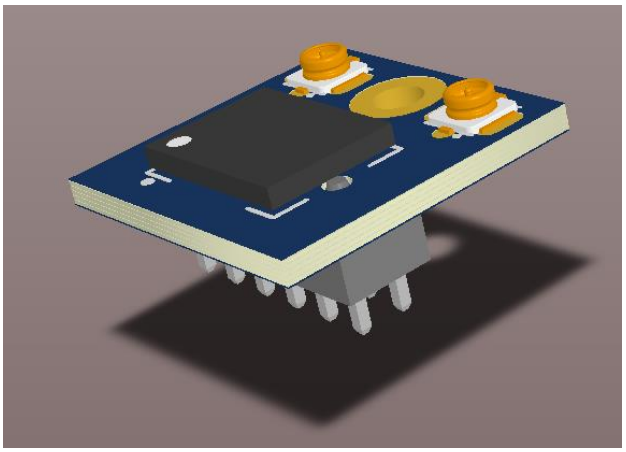
Possible module sizes from 14 x 14 mm to 67.7 x 57.5 mm.

Standard full-length single slot module: 22 x 57.5 mm.

LS Modules

Smallest CRUVI module size is 14 by 14 mm, recommended PCB thickness 1.2mm (1.6mm acceptable). This format is suitable for modules that have one small main IC with 3.3V tolerant IO. External I/O is possible also via front panel using U.fl style mini coax connectors. Recommended location for them is shown. This format can extend to 22 by 16 mm.





As example BGA 6x8 mm SPI Flash Device is placed.

Possible IC/Functions

- I^2C EEPROM
- Microwire or SPI EEPROM
- I^2C ADC, DAC, Sensor or special function
- UN I/O EEPROM
- 1-Wire EEPROM or special function
- (Q)SPI Flash or SRAM
- SPI ADC, DAC or special function
- I2S/PDM MEMS microphone
- Special function IC with low pin count interface (PWM, etc.)
- CRUVI Signal breakout to connector(s)
- I^2C programmable Oscillator or PLL
- Status LED and User button

Connectors

Connector stacking height is 5mm

Type	Carrier/Base	Module/Function
High Speed/Transceiver	SS4-30-3.50-L-D-K	ST4-30-1.50-L-D-P
Low Speed	CLT-106-02-F-D-A-K	TMMH-106-04-F-DV-A-M

Mounting hardware

Use 5mm threaded spacers for M2 screws. Carrier boards may use soldered down SMD spacer's type

9774050243R  from Würth.

Module formats

CRUVI modules can be one, two or three slot-wide. One-slot wide modules can be 14 to 22 mm wide. Two-slot wide module max width is 22 mm + 900 mil; three-slot wide module max width is 22 mm + 1800 mil (67.72mm).

Host Adapters

For cases where host FPGA/SoC has limited I/O connectors should be fitted in special order to maximize the variety of supported add-module combinations.

Recommendation: if possible on host boards all LS connectors should be fitted, small FPGA can be used to add more I/O and perform local preprocessing and/or protocol/interface conversion.

Host 2 slot wide 2 connectors

Slot	**Connectors**		
A	HS	HS	LS or HS
B	LS	LS	

This is the minimal configuration that support single and double wide modules with LS or HS connectors.

Host 3 slot wide with 3 connectors supporting GT4

Slot	**Connectors**				
A	HS	HS	HS	HS	LS or HS or GT
B	-	Empty		LS or GT4	
C	GT4 + LS	LS or GT4	LS or GT4		

This is the minimal configuration that support all types of possible modules up to 3 slot wide. If two single wide modules are fitted one slot would remain empty.

Host 3 slot wide with 4 connectors supporting GT4

Slot	**Connectors**				
A	HS	HS	LS or HS	HS	LS or HS or GT
B	LS	LS		LS or GT4	
C	GT4 + LS	LS or GT4	LS or GT4		

This is the minimal configuration that support all type of possible modules up to 3 slot wide and all types at same time if all are single slot wide.

CAD Support

CRUVI standard was developed using Altium Designer as CAD Tool. Primary designs and design templates are all in Altium Designer format. It is recommended do start a design from some existing Altium project or template.

TODO: Provide github link to downloadable Altium projects!

Production Support

Trenz Electronic GmbH offers special production support for CRUVI modules and bases if they are developed in Altium using special database library from Trenz Electronic (this library can be made accessible to interested parties).

Use Cases

List of some common use cases.

I2C Device

A module with some I2C device(s) can be in LS format with one or two mounting holes.

HyperBus/xSPI/OctaBus

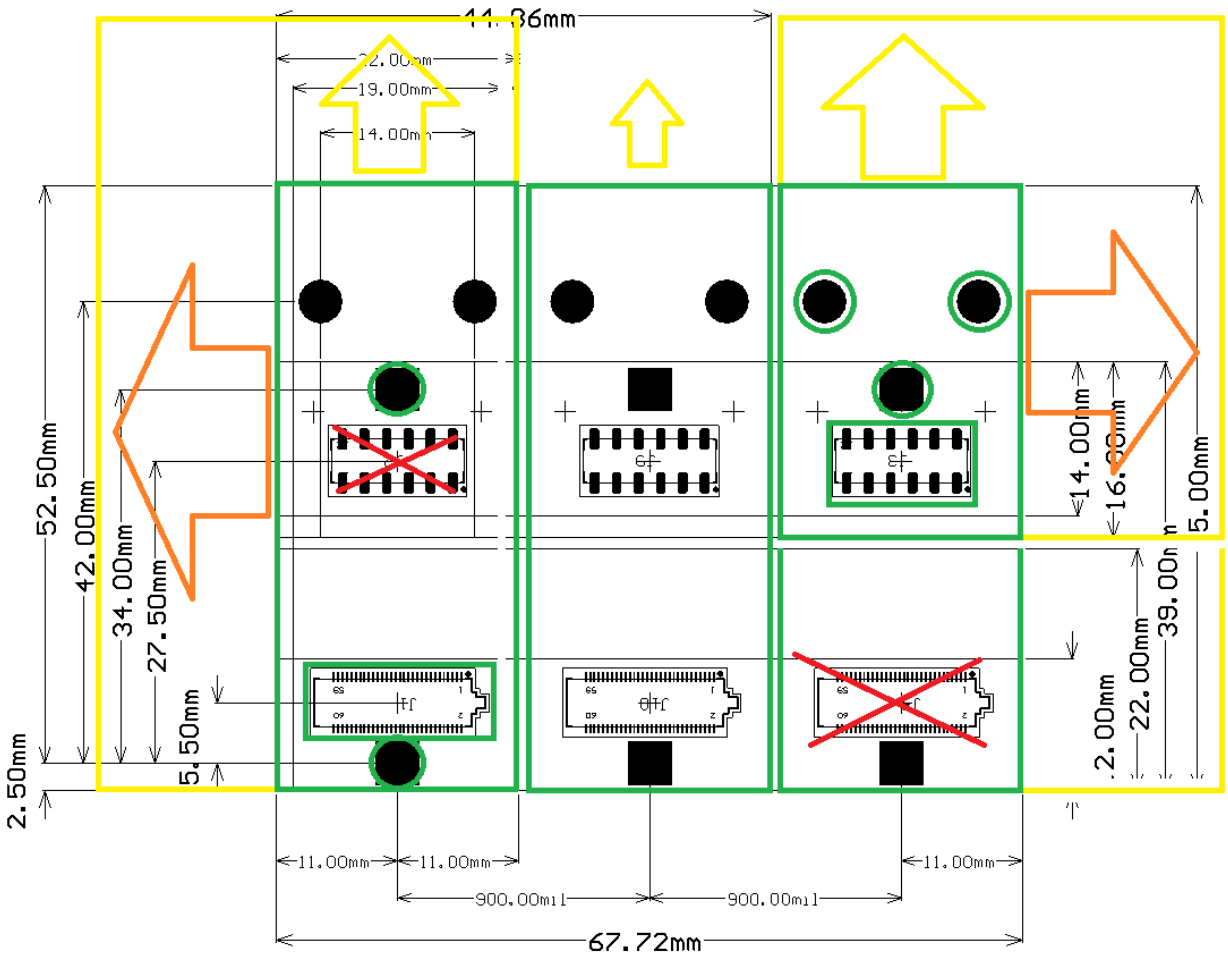
HyperBus, OctaBus and xSPI devices can be used on small HS modules with only one mounting hole. An example is CR00041 module. Space required on the baseboard is about 20x22 mm.

SPI (boot) Flash

SPI and QSPI Flash modules can be in smallest LS format sized 14x14 mm. On the baseboard same amount of free space is needed, only one mounting hole is used. With passive PMoD adapter it is also possible use those modules with PMoD host boards.

Evaluation or Demo Board

It is recommended when possible to design all boards to be complaint to standard recommended CRUVI module formats. If needed the PCB sizes can be extended for boards designed for evaluation and demo or prototype use only.



TODO – update graphics

For evaluation use, if PCB size has to extend over standard format, then use above as guidance for the priority direction how to extend the board size. The above example shows that a 3 slot base board could accept at the same time 2 oversized modules and one standard format module.

TODO: Make exact templates for all possible (reasonable) variants showing which mounting holes are mandatory and which one recommended only.

Disclaimer

Links/References

- Semantic Versioning Specification http://semver.org
- RFC2119 https://tools.ietf.org/html/rfc2119
- JESD251 xSPI
- Digilent PMoD ™ Specification
- VHDPLus CRUVI Products