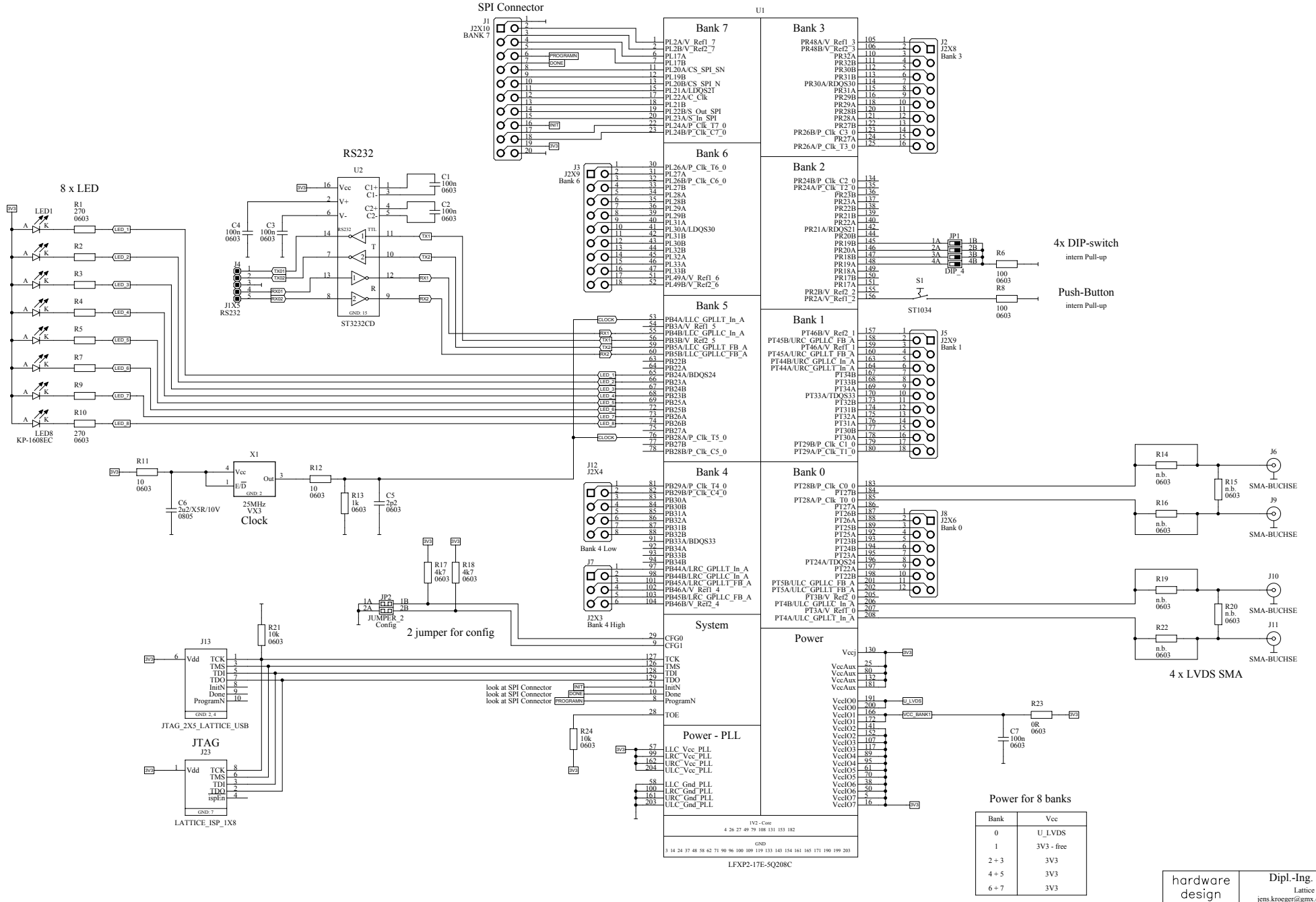
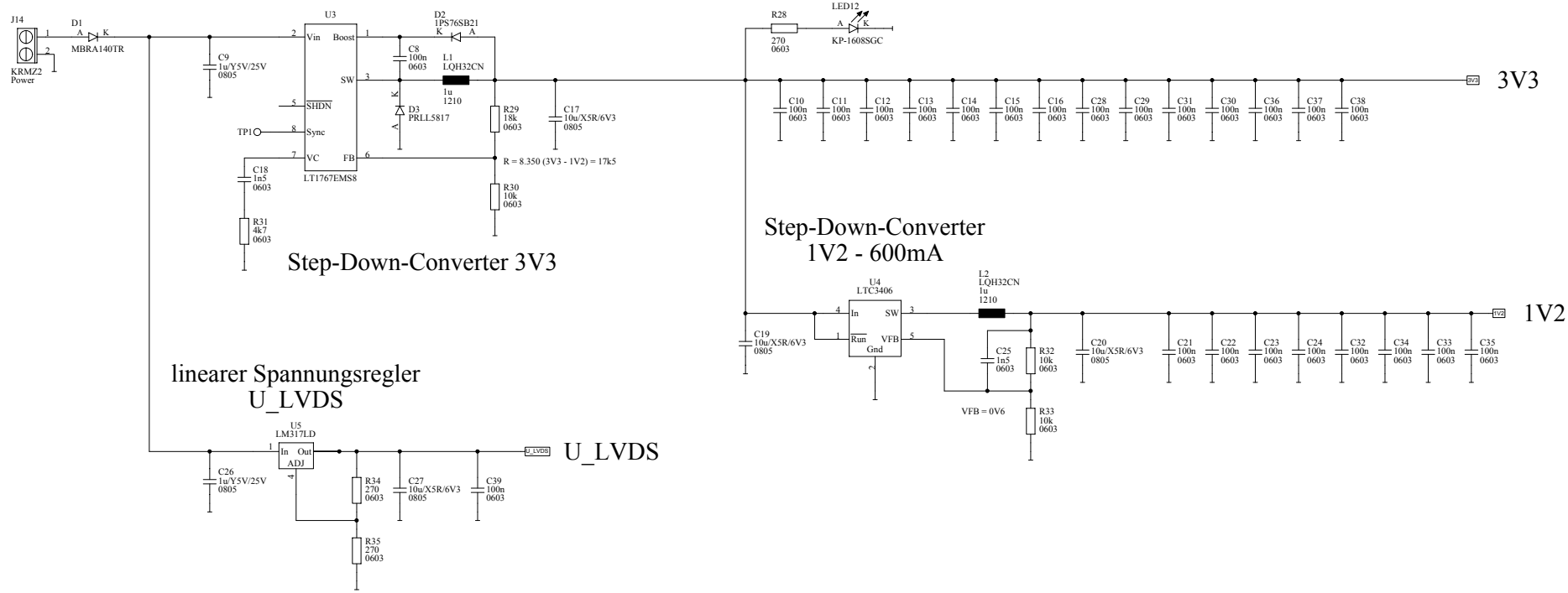


hardware design www.hardware-design.de	Dipl.-Ing. Jens Kroeger Lattice EV-Boards jens.kroeger@gmx.de - Tel: 05305 202836 Dr.-Bockemüller-Ring 35 * 38173 Sickte
Title	LFXP2-17, LEDs, Switch, Ports, JTAG, LVDS
Projekt	Lattice FPGA-Demoboard — Rev 1.4
Engineering Jens Kroeger	Worksize A2
Start 03.08.2007 — Drawn by Jens Kroeger	Printsize A3
Last Update 22.02.2008 — Filename LFXP2_1.SCH	Sheet 1 of 2

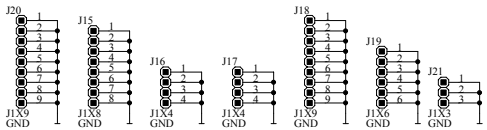
Power - In

5 to 25V

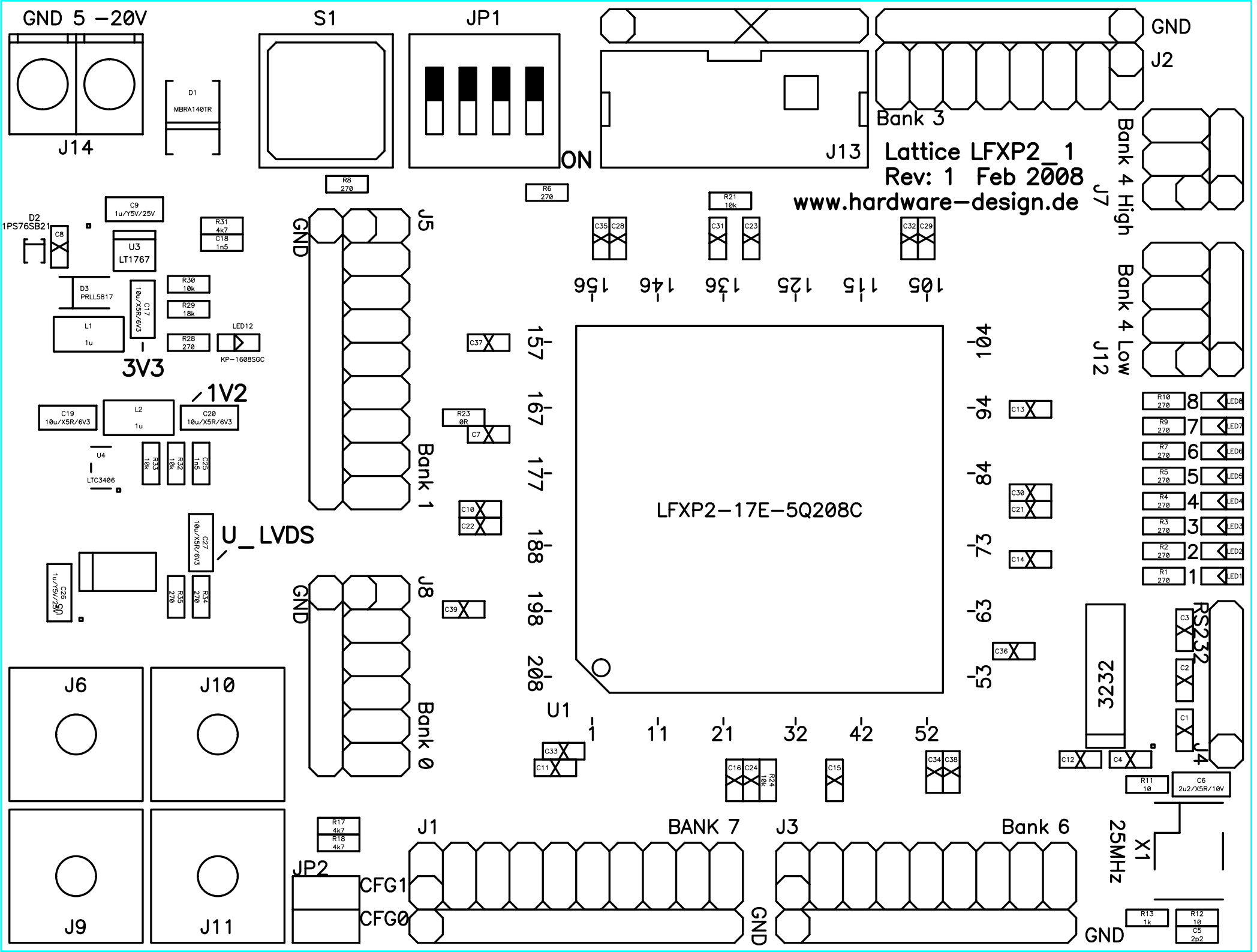


2V5 for LVDS at Bank 0

Vout = 1,25V (1 + R_top/R_buttom) + 0,1mA * R_buttom
I max = 100mA



hardware design www.hardware-design.de	Dipl.-Ing. Jens Kroeger Lattice EV-Boards jens.kroeger@gmx.de - Tel: 05305 202836 Dr.-Bockemüller-Ring 35 * 38173 Sickte	
Title Power		
Projekt Lattice FPGA-Demoboard		Rev 1.4
Engineering Jens Kroeger		Worksize A2
Start 03.08.2007	Drawn by Jens Kroeger	Printsize A3
Last Update 22.02.2008	Filename LFXP2_1.SCH	Sheet 2 of 2


GND 5 –20V
J14
D1
MBRA140TR
S1
JP1
ON
J13
Bank 3
GND
J2
Lattice LFXP2_1
Rev: 1 Feb 2008
www.hardware-design.de
Bank 4 High
J7
Bank 4 Low
J12
D2
1PS76SB21
C8
C9
1u/Y5V/25V
U3
LT1767
R31
4k7
C18
1n5
D3
PRLL5817
C17
10u/X5R/6V3
L1
1u
R30
10k
R29
18k
R28
270
LED12
KP-1608SGC
3V3
1V2
C19
10u/X5R/6V3
L2
1u
C20
10u/X5R/6V3
U4
LTC3406
R33
10k
R32
10k
C25
1n5
U_LVDS
C27
10u/X5R/6V3
C26
1u/Y5V/25V
R35
270
R34
270
R8
270
R6
270
R21
10k
J5
GND
Bank 1
J8
GND
Bank 0
C35
C28
C31
C23
C32
C29
C37
R23
0R
C7
C10
C22
C39
LFXP2-17E-5Q208C
U1
C33
C11
C16
C24
R24
10k
C15
C34
C38
C13
C30
C21
C14
C36
R10
270
R9
270
R7
270
R5
270
R4
270
R3
270
R2
270
R1
270
LED8
LED7
LED6
LED5
LED4
LED3
LED2
LED1
3232
C12
C4
C3
C2
C1
RS232
J4
R11
10
C6
2u2/X5R/10V
X1
25MHz
R13
1k
R12
10
C5
2p2
J6
J10
J9
J11
R17
4k7
R18
4k7
JP2
CFG1
CFG0
J1
BANK 7
GND
J3
Bank 6
GND