Cyclone V GT FPGA Development Board

Reference Manual

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1. Overview

This document describes the hardware features of the Cyclone® V GT FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Cyclone V GT FPGA development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Cyclone V GT FPGA device. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Cyclone V GT designs.

Two high-speed mezzanine card (HSMC) connectors are available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP, partial reconfiguration, and hard memory controller implementation ensure that designs implemented in the Cyclone V GTs operate faster, with lower power, and have a faster time to market than previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Cyclone V device family, refer to the *Cyclone V Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The development board features the following major component blocks:

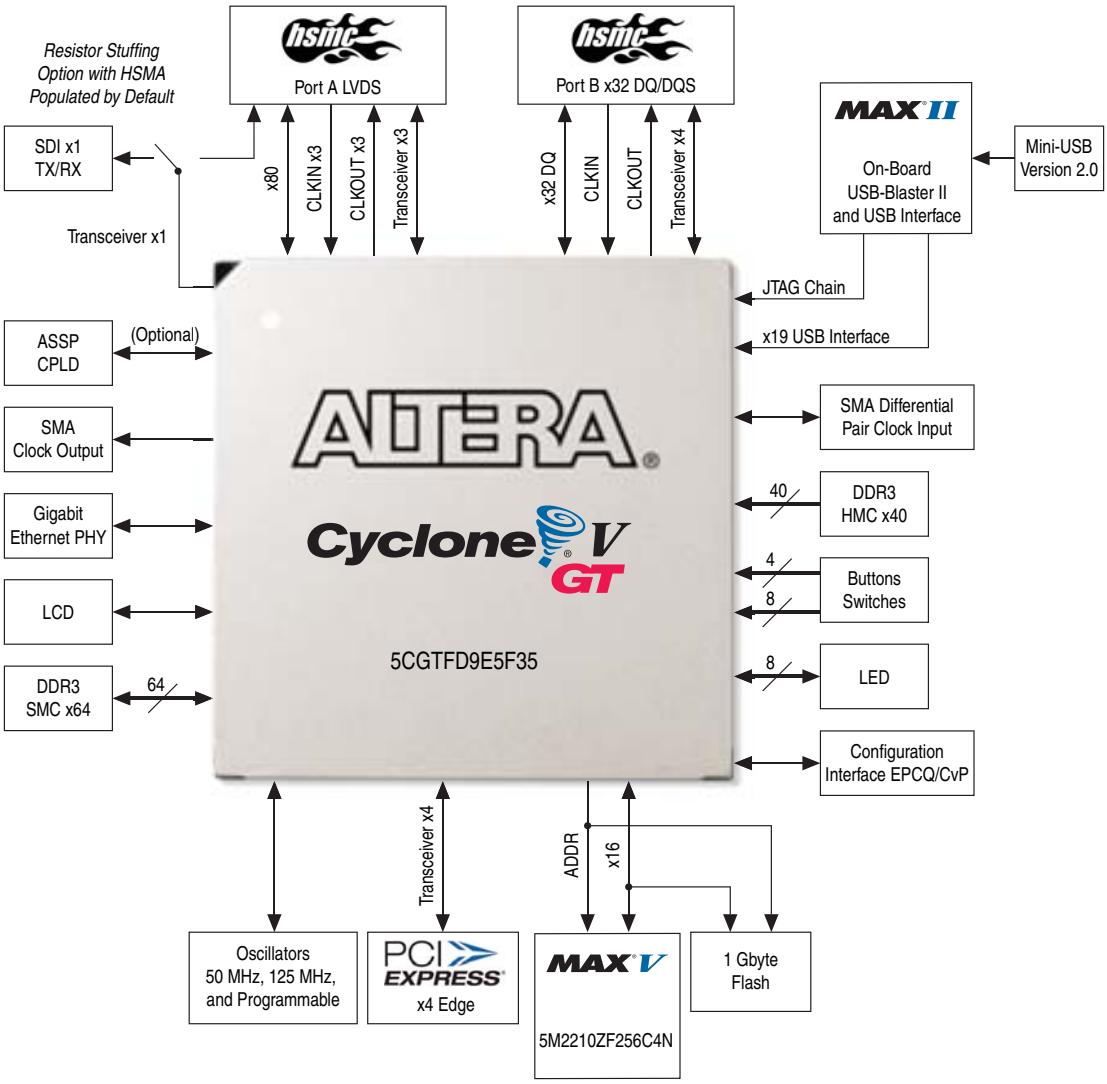
- One Cyclone V GT FPGA (5CGTFD9E5F35C7N) in a 1152-pin FineLine BGA (FBGA) package
- FPGA configuration circuitry
  - MAX® V CPLD (5M2210ZF256C4N) in a 256-pin FBGA package as the System Controller
  - MAX II CPLD (EPM570GT100C3N) in a 100-pin FBGA package as part of the embedded USB-Blaster™ II for use with the Quartus® II Programmer
  - MAX II CPLD (EPM570ZM100) in a 100-pin MBGA package for use with ASSP (optional)
  - Flash fast passive parallel (FPP) configuration
- Clocking circuitry
  - Si570 and Si571 programmable oscillators
  - 50-MHz, 100-MHz, and 125-MHz oscillators
- Memory
  - DDR3 SDRAM
    - DDR3A provides 256 Mbyte (MB) with ECC using three devices, each having a 16-bit interface to a hard memory controller
    - DDR3B provides 512 MB using four devices, each having a 16-bit interface to a soft memory controller
  - One 1-gigabit (Gb) synchronous flash with a 16-bit data bus
- Communication Ports
  - One PCI Express x4 Gen1 socket
  - Two universal HSMC ports
  - One Gigabit Ethernet port
  - One serial digital interface (SDI) port (optional)
  - One SMA clock or data output

- General user input/output
  - LEDs and displays
    - Eight user LEDs
    - One configuration load LED
    - One configuration done LED
    - One error LED
    - Four embedded USB-Blaster II status LEDs
    - Six HSMC interface LEDs
    - Four PCI Express link width LEDs (mirrored on top and bottom)
    - Five Ethernet LEDs
    - One SDI carrier detect LED
    - One power on LED
    - One two-line character LCD display
  - Push buttons
    - One CPU reset push button
    - One MAX V reset push button
    - One program select push button
    - One program configuration push button
    - Three general user push buttons
  - DIP switches
    - Two board settings DIP switches
    - JTAG chain control or PCI Express link width DIP switch
    - FPGA configuration mode DIP switch
    - One general user DIP switch
- Power supply
  - 19-V (laptop) DC input
  - PCI Express edge connector
- Mechanical
  - PCI Express half-length form factor (4.376" x 6.600")
- System Monitoring—Power (voltage, current, wattage)

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Cyclone V GT FPGA development board.

Figure 1–1. Cyclone V GT FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces the major components on the Cyclone V GT FPGA development board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and fabrication files for the development board reside in the Cyclone V GT FPGA development kit board design files directory.

For information about powering up the board and installing the demonstration software, refer to the *Cyclone V GT FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Cyclone V GT FPGA development board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the board features.

Figure 2–1. Overview of the Cyclone V GT FPGA Development Board Features

Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Board Components (Part 1 of 4)

Board Reference	Type	Description
Featured Devices		
U13	FPGA	Cyclone V GT, 5CGTFD9E5F35C7N, 1152-pin FBGA.
U32	CPLD	MAX V CPLD, 5M2210ZF256C4N, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J13	JTAG chain header	Provides access to the JTAG chain and disables the embedded USB-Blaster II when using an external USB-Blaster cable.
SW3	JTAG chain control or PCI Express DIP switch	Remove or include devices in the active JTAG chain. Also controls the PCI Express lane width by connecting the `prsnt` pins together on the PCI Express edge connector.

Table 2–1. Board Components (Part 2 of 4)

Board Reference	Type	Description
J5	Mini USB type-AB connector	USB interface for FPGA programming and debugging through the embedded USB-Blaster II JTAG via a mini-USB type-B cable.
SW4	Board settings DIP switch	Controls the MAX V CPLD 5M2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
SW5	FPGA configuration mode DIP Switch	Controls the supported FPGA configuration mode by altering the MSEL input pins. This switch can also control the fan speed by forcing it to run at full speed, over-riding the fan control block in the MAX V CPLD.
S6	Program select push button	Toggles the program select LEDs, which selects the program image that loads from flash memory to the FPGA.
S5	Program configuration push button	Load image from flash memory to the FGPA based on the settings of the program select LEDs.
D7	Configuration done LED	Illuminates when the FPGA is configured.
D6	Load LED	Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA.
D5	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D21	Power LED	Illuminates when 5.0-V power is present.
D12, D13, D14	Program select LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program select push button. Refer to Table 2–6 for the LED settings.
D22, D23, D24, D25, D26	Ethernet LEDs	Illuminates to show the connection speed as well as transmit or receive activity.
D32	SDI LEDs	Illuminates to show the transmit or receive activity.
D3, D4, D19, D20	HSMC port LEDs	You can configure these LEDs to indicate transmit or receive activity.
D1, D2	HSMC port present LED	Illuminates when a daughtercard is plugged into the HSMC port.
D34, D35, D44, D45	PCI Express link LEDs	You can configure these LEDs to indicate the PCI Express link width (x1, x4) and Gen1 link.
Clock Circuitry		
X6	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic. This oscillator is the input source to a clock buffer with two outputs. One output clock goes to the FPGA and one goes to the MAX V CPLD 5M2210 System Controller.
X2	100-MHz oscillator	100.000-MHz crystal oscillator for the MAX V CPLD 5M2210 System Controller.
X3	148.500-MHz oscillator	148.500-MHz voltage controlled oscillator for the serial digital interface (SDI) video. This oscillator is programmable to any frequency between 20–810 MHz using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X4	100-MHz oscillator	Programmable oscillator (10–810 MHz) with a default frequency of 100.000 MHz. This clock is the clock input source to a 6-output clock buffer (U3). The buffer can select between this clock source or a pair of SMA connectors as the input clock source.
X5	125-MHz oscillator	125.000-MHz voltage controlled oscillator for the FPGA.
J11, J12	SDI transceiver connectors	Drives serial data input/output to or from the SDI video port.

Table 2–1. Board Components (Part 3 of 4)

Board Reference	Type	Description
J3, J6	Clock input SMA connectors	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer.
J4, J7	Clock output SMA connectors	Drives out 2.5-V CMOS clock output from the clock buffer (U3).
J14	SMA connector	SMA to or from the FPGA, which can be an I/O or a clock output.
General User Input/Output		
D8–D11, D15–D18	User LEDs	Eight user LEDs. Illuminates when driven low.
SW1	User DIP switch	Quad user DIP switches. When the switch is ON, a logic 0 is selected.
S4	CPU reset push button	Reset the FPGA logic.
S7	MAX V reset push button	Reset the MAX V CPLD 5M2210 System Controller.
S1–S3	General user push buttons	Three user push buttons. Driven low when pressed.
Memory Devices		
U26, U27, U28	DDR3 x40 memory	Three 128-MB DDR3A SDRAM with ECC, each with a 16-bit data bus for a hard memory controller.
U8, U15, U22, U30	DDR3 x64 memory	Four 128-MB DDR3B SDRAM, each with a 16-bit data bus for a soft memory controller.
U20	Flash x16 memory	1-Gb synchronous flash devices with a 16-bit data bus for non-volatile memory.
Communication Ports		
J16	PCI Express edge connector	Gold-plated edge fingers connector for up to ×4 signaling in Gen1 mode.
J1, J2	HSMC port	Two ports, one with four transceiver channels and 84 CMOS or 17 LVDS channels as per the HSMC specification, and one with CMOS I/O assignments and DQS/DQx32 assignments for future use.
J9	Gigabit Ethernet port	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Video and Display Ports		
J10	Character LCD	Connector that interfaces to a provided 16 character × 2 line LCD module along with four standoffs.
J11, J12	SDI video port	Two 75-Ω sub-miniature version B (SMB) connectors that provide a full-duplex SDI interface through a LMH0303 cable driver and LMH0384 cable equalizer. By default, this is not an active interface but is only available when you switch the resistor placement. After making this resistor change, the HSMC port A transceiver channel 3 is no longer available.
Power Supply		
J16	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J8	DC input jack	Accepts a 19-V DC power supply. Do not use this input jack while the board is plugged into a PCI Express slot.

Table 2–1. Board Components (Part 4 of 4)

Board Reference	Type	Description
SW2	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.
J15	Fan power	Fan power header.

Featured Device: Cyclone V GT FPGA

The Cyclone V GT FPGA development board features a Cyclone V GT 5CGTFD9E5F35C7N device in a 1152-pin FBGA package.

For more information about Cyclone V device family, refer to the *Cyclone V Device Handbook*.

Table 2–2 describes the features of the Cyclone V GT 5CGTFD9E5F35C7N device.

Table 2–2. Cyclone V GT Features

Resource		5CGTFD9E5F35C7N
LEs (K)		301
ALMs		113,560
Register		454,240
Memory (Kb)	M10K	12,200
	MLAB	1,717
18-bit × 18-bit Multiplier		684
PLLs		8
Transceivers (6 Gbps)		12

I/O Resources

The Cyclone V GT 5CGTFD9E5F35C7N device has total of 560 user I/Os and 12 transceiver channels. Table 2–3 lists the Cyclone V GT device I/O pin count and usage by function on the board.

Table 2–3. Cyclone V GT Device I/O Pin Count

Function	I/O Standard	I/O Count	Special Clock Pins
DDR3A	1.5-V SSTL	81	—
DDR3B	1.5-V SSTL	114	—
MAX V System Controller	1.8-V CMOS	4	—
Flash	1.8-V CMOS	49	—
PCI Express x4 port	2.5-V CMOS	8	One reference clock
HSMA port	2.5-V CMOS + LVDS	87	—
HSMB port	1.2-V–2.5-V CMOS DQ/DQS (Default: 2.5-V)	88	—
Gigabit Ethernet port	2.5-V CMOS + LVDS	16	—
On-Board USB-Blaster II	1.5-V or 2.5-V CMOS	19	—

Table 2–3. Cyclone V GT Device I/O Pin Count

Function	I/O Standard	I/O Count	Special Clock Pins
SDI video port	2.5-V CMOS + XCVR	6	—
Push buttons	1.5-V CMOS	4	—
DIP switches	1.5-V CMOS	8	—
Character LCD	1.5-V CMOS	2	—
LEDs	1.5-V CMOS	8	—
SMA	CMOS	1	—
Clock or Oscillators	1.8-V CMOS + LVDS	9	Four differential clocks, 1 1 single-ended
ASSP	1.5-V CMOS	8	—
Configuration	—	30	—
Total I/O Used:		**540**	

Table 2–4 lists the Cyclone V GT device transceiver count and usage by function on the board.

Table 2–4. Cyclone V GT Transceivers

Function	Count
HSMA port	3
HSMA port or SDI (supports HSMA by default)	1
HSMB port	4
PCI Express x4 port	4
Total Transceivers	**12**

MAX V CPLD 5M2210 System Controller

The board utilizes the 5M2210 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash
- Power measurement
- Control and status registers (CSRs) for remote system update

Figure 2–2 illustrates the MAX V CPLD 5M2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–2. MAX V CPLD 5M2210 System Controller Block Diagram

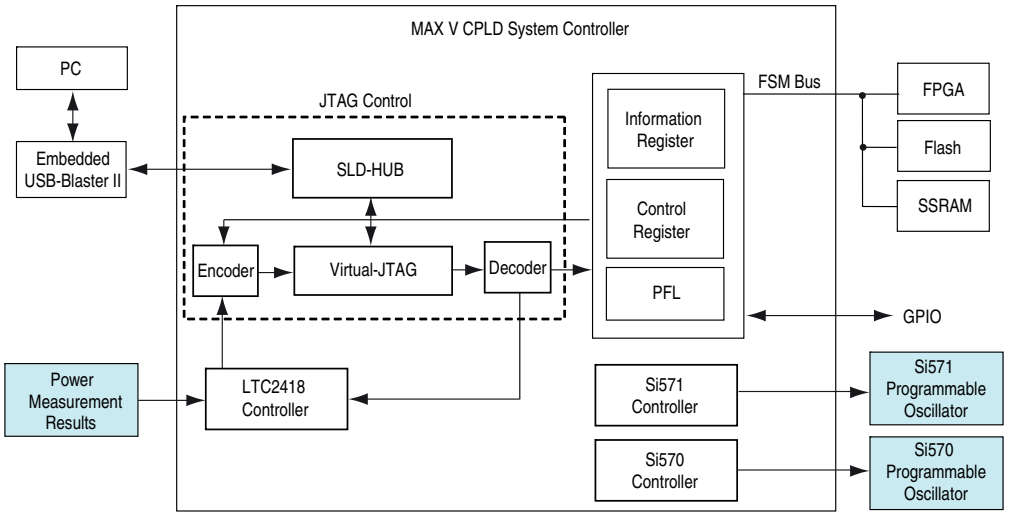


Table 2–5 lists the I/O signals present on the MAX V CPLD 5M2210 System Controller. The signal names and functions are relative to the MAX V device.

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 1 of 5)

Board Reference (U32)	Schematic Signal Name	I/O Standard	Description
L2	ASSP_CPLD_MRN	2.5-V	For ASSP design (optional)
R12	ASSP_MODE	2.5-V	For ASSP design (optional)
B9	CLK125_EN	2.5-V	125 MHz oscillator enable
E9	CLK50_EN	2.5-V	50 MHz oscillator enable
J5	CLK_CONFIG	2.5-V	100 MHz configuration clock input
A15	CLK_ENABLE	2.5-V	DIP switch for clock oscillator enable
A13	CLK_SEL	2.5-V	DIP switch for clock select—SMA or oscillator
J12	CLKIN_MAX_50	2.5-V	50 MHz clock input
C9	CLOCK_SCL	2.5-V	Programmable oscillator I^2C clock
D9	CLOCK_SDA	2.5-V	Programmable oscillator I^2C data
D10	CPU_RESETN	2.5-V	FPGA reset push button
M1	EXTRA_SIG0	2.5-V	Embedded USB-Blaster II interface. Reserved for future use
T13	EXTRA_SIG1	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T15	EXTRA_SIG2	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
R14	FACTORY_REQUEST	1.8-V	Embedded USB-Blaster II request to send FACTORY command
N12	FACTORY_STATUS	1.8-V	Embedded USB-Blaster II FACTORY command status
A2	FACTORY_USER	1.8-V	DIP switch to load factory or user design at power-up

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 2 of 5)

Board Reference (U32)	Schematic Signal Name	I/O Standard	Description
N7	FLASH_ADVN	1.8-V	FM bus flash memory address valid
R5	FLASH_CEN	1.8-V	FM bus flash memory chip enable
R6	FLASH_CLK	1.8-V	FM bus flash memory clock
M6	FLASH_OEN	1.8-V	FM bus flash memory output enable
T5	FLASH_RDYBSYN	1.8-V	FM bus flash memory ready
P7	FLASH_RESETN	1.8-V	FM bus flash memory reset
N6	FLASH_WEN	1.8-V	FM bus flash memory write enable
C14	FM_A1	1.8-V	FM address bus
C15	FM_A2	1.8-V	FM address bus
E13	FM_A3	1.8-V	FM address bus
E12	FM_A4	1.8-V	FM address bus
D15	FM_A5	1.8-V	FM address bus
F14	FM_A6	1.8-V	FM address bus
D16	FM_A7	1.8-V	FM address bus
F13	FM_A8	1.8-V	FM address bus
E15	FM_A9	1.8-V	FM address bus
E16	FM_A10	1.8-V	FM address bus
F15	FM_A11	1.8-V	FM address bus
G14	FM_A12	1.8-V	FM address bus
F16	FM_A13	1.8-V	FM address bus
G13	FM_A14	1.8-V	FM address bus
G15	FM_A15	1.8-V	FM address bus
G12	FM_A16	1.8-V	FM address bus
G16	FM_A17	1.8-V	FM address bus
H14	FM_A18	1.8-V	FM address bus
H15	FM_A19	1.8-V	FM address bus
H13	FM_A20	1.8-V	FM address bus
H16	FM_A21	1.8-V	FM address bus
J13	FM_A22	1.8-V	FM address bus
R3	FM_A23	1.8-V	FM address bus
P5	FM_A24	1.8-V	FM address bus
T2	FM_A25	1.8-V	FM address bus
P4	FM_A26	1.8-V	FM address bus
J14	FM_D0	1.8-V	FM data bus
J15	FM_D1	1.8-V	FM data bus
K16	FM_D2	1.8-V	FM data bus
K13	FM_D3	1.8-V	FM data bus
K15	FM_D4	1.8-V	FM data bus
K14	FM_D5	1.8-V	FM data bus

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 3 of 5)

Board Reference (U32)	Schematic Signal Name	I/O Standard	Description
L16	FM_D6	1.8-V	FM data bus
L11	FM_D7	1.8-V	FM data bus
L15	FM_D8	1.8-V	FM data bus
L12	FM_D9	1.8-V	FM data bus
M16	FM_D10	1.8-V	FM data bus
L13	FM_D11	1.8-V	FM data bus
M15	FM_D12	1.8-V	FM data bus
L14	FM_D13	1.8-V	FM data bus
N16	FM_D14	1.8-V	FM data bus
M13	FM_D15	1.8-V	FM data bus
N15	FORCE_FAN	1.8-V	DIP switch to enable or disable the fan
K5	FPGA_CEN	2.5-V	FPGA chip enable
K1	FPGA_CONF_DONE	2.5-V	FPGA configuration done LED
D3	FPGA_CONFIG_D0	2.5-V	FPGA configuration data
C2	FPGA_CONFIG_D1	2.5-V	FPGA configuration data
C3	FPGA_CONFIG_D2	2.5-V	FPGA configuration data
E3	FPGA_CONFIG_D3	2.5-V	FPGA configuration data
D2	FPGA_CONFIG_D4	2.5-V	FPGA configuration data
E4	FPGA_CONFIG_D5	2.5-V	FPGA configuration data
D1	FPGA_CONFIG_D6	2.5-V	FPGA configuration data
E5	FPGA_CONFIG_D7	2.5-V	FPGA configuration data
F3	FPGA_CONFIG_D8	2.5-V	FPGA configuration data
E1	FPGA_CONFIG_D9	2.5-V	FPGA configuration data
F4	FPGA_CONFIG_D10	2.5-V	FPGA configuration data
F2	FPGA_CONFIG_D11	2.5-V	FPGA configuration data
F1	FPGA_CONFIG_D12	2.5-V	FPGA configuration data
F6	FPGA_CONFIG_D13	2.5-V	FPGA configuration data
G2	FPGA_CONFIG_D14	2.5-V	FPGA configuration data
G3	FPGA_CONFIG_D15	2.5-V	FPGA configuration data
N3	FPGA_CVP_CONFDONE	2.5-V	FPGA configuration via protocol done LED
J3	FPGA_DCLK	2.5-V	FPGA configuration clock
B10	FPGA_MSEL0	2.5-V	FPGA mode select 0
B3	FPGA_MSEL1	2.5-V	FPGA mode select 1
C10	FPGA_MSEL2	2.5-V	FPGA mode select 2
C12	FPGA_MSEL3	2.5-V	FPGA mode select 3
C6	FPGA_MSEL4	2.5-V	FPGA mode select 4
N1	FPGA_NCONFIG	2.5-V	FPGA configuration active
J4	FPGA_NSTATUS	2.5-V	FPGA configuration ready
H1	FPGA_PR_DONE	2.5-V	FPGA partial reconfiguration done

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 4 of 5)

Board Reference (U32)	Schematic Signal Name	I/O Standard	Description
P2	FPGA_PR_ERROR	2.5-V	FPGA partial reconfiguration error
E2	FPGA_PR_READY	2.5-V	FPGA partial reconfiguration ready
F5	FPGA_PR_REQUEST	2.5-V	FPGA partial reconfiguration request
B8	HSMA_PRSNTN	2.5-V	HSMC port A present
A8	HSMB_PRSNTN	2.5-V	HSMC port B present
M5	JTAG_BLASTER_TDI	2.5-V	MAX V CPLD JTAG chain data out
L6	JTAG_EPM2210_TDI	2.5-V	MAX V CPLD JTAG chain data in
P3	JTAG_TCK	2.5-V	JTAG chain clock
N4	JTAG_TMS	2.5-V	JTAG chain mode select
P11	M570_CLOCK	1.8-V	25-MHz clock to embedded USB-Blaster II for sending FACTORY command
P12	M570_PCIE_JTAG_EN	1.8-V	Low signal to disable the embedded USB-Blaster II when PCI Express is the master to the JTAG chain
H2	MAX_AS_CONF	2.5-V	MAX V active serial configuration
T11	MAX_CLK	2.5-V	Clock source from the FPGA PLL
E11	MAX_CONF_DONE	2.5-V	Embedded USB-Blaster II configuration done LED
R10	MAX_CSN	1.8-V	FM bus MAX V chip select
A4	MAX_ERROR	2.5-V	FPGA configuration error LED
A6	MAX_LOAD	2.5-V	FPGA configuration active LED
M10	MAX_OEN	1.8-V	FM bus MAX V output enable
M9	MAX_RESETN	1.8-V	MAX V reset push button
N10	MAX_WEN	1.8-V	FM bus MAX V write enable
B7	OVERTEMP	2.5-V	Temperature monitor fan enable
D12	PGM_CONFIG	2.5-V	Load the flash memory image identified by the PGM LEDs
B14	PGM_LED0	2.5-V	Flash memory PGM select indicator 0
C13	PGM_LED1	2.5-V	Flash memory PGM select indicator 1
B16	PGM_LED2	2.5-V	Flash memory PGM select indicator 2
B13	PGM_SEL	2.5-V	Toggles the PGM_LED[2:0] LED sequence
D5	SDI_A_RX_BYPASS	2.5-V	SDI equalization bypass
E8	SDI_A_RX_EN	2.5-V	SDI receive enable
D11	SDI_A_TX_EN	2.5-V	SDI transmit enable
E7	SENSE_CSN	2.5-V	Power monitor chip select
A5	SENSE_SCK	2.5-V	Power monitor SPI clock
D7	SENSE_SDI	2.5-V	Power monitor SPI data in
B6	SENSE_SDO	2.5-V	Power monitor SPI data out
A10	SI570_EN	2.5-V	Variable voltage oscillator enable
D4	SI571_EN	2.5-V	SDI variable voltage oscillator enable
R4	USB_CFG0	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T4	USB_CFG1	1.8-V	Embedded USB-Blaster II interface. Reserved for future use

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 5 of 5)

Board Reference (U32)	Schematic Signal Name	I/O Standard	Description
P8	USB_CFG2	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T7	USB_CFG3	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
N8	USB_CFG4	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
R8	USB_CFG5	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T8	USB_CFG6	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T9	USB_CFG7	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
R9	USB_CFG8	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
P9	USB_CFG9	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
M8	USB_CFG10	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
T10	USB_CFG11	1.8-V	Embedded USB-Blaster II interface. Reserved for future use
H5	USB_CLK	2.5-V	Embedded USB-Blaster II interface clock

Configuring the MAX V Device to Program EPCQ

It is possible to configure the FPGA from the EPCQ device. However, the MAX V design provided with the Cyclone V GT FPGA development kit does not allow you to store a design in the EPCQ configuration device.

To enable FPGA configuration using the EPCQ device, reconfigure the MAX V device with the design file found at How do I access the EPCQ configuration device on the Cyclone V GT FPGA Development Kit?.

FPGA Configuration

The Cyclone V GT development board supports the following three configuration methods:

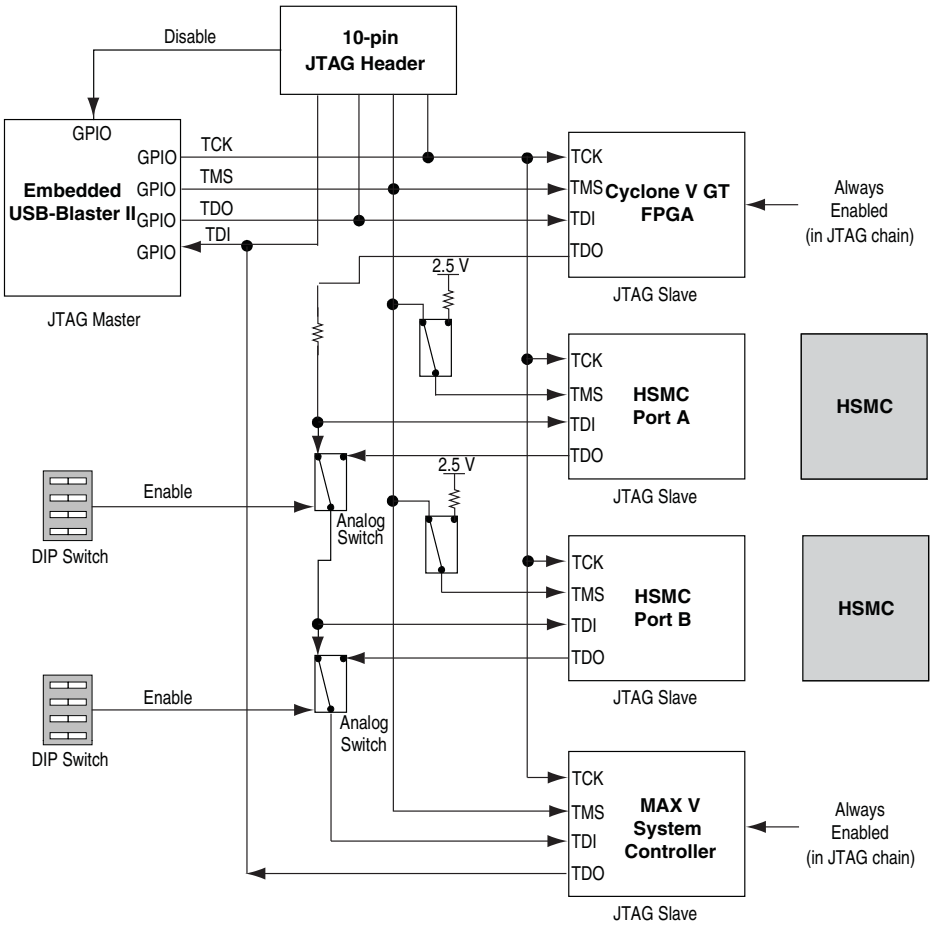
- Embedded USB-Blaster II is the default method for configuring the FPGA using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the program configuration push button (S6).
- External USB-Blaster for configuring the FPGA using an external USB-Blaster that connects to the JTAG chain header (J13).

FPGA Programming over Embedded USB-Blaster

This configuration method implements a type-B mini USB connector (J5), a USB 2.0 PHY device (U4), and an Altera MAX II CPLD EPM570GT100C3N (U49) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB connector on the board and a USB port of a PC running the Quartus II software.

The embedded USB-Blaster II in the MAX II CPLD EPM570GT100C3N normally masters the JTAG chain. Figure 2–3 illustrates the JTAG chain.

Figure 2–3. JTAG Chain



The JTAG chain control DIP switch (SW3) controls the device connection. To connect a device or interface in the chain, their corresponding switch must be in the OFF position. Slide all the switches to the ON position to only have the FPGA and MAX V CPLD 5M2210 System Controller in the chain.

A Cypress EZ-USB CY7C68013A device in a 56-pin VBGA package device is used to interface to a single type-B mini-USB connector. This device has an on-board 8051 CPU used in conjunction with embedded MAC logic to translate USB data into other formats for use by the FPGA. This CPU uses internal RAM and a small external serial boot ROM.

FPGA Programming from Flash Memory

Flash memory programming is possible through a variety of methods. The default method is to use the factory design—Board Update Portal. This design is an embedded web server, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

On either power-up or by pressing the program configuration push button, PGM_CONFIG (S5), the MAX V CPLD 5M2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 8-bit data is then written to the dedicated configuration pins in the FPGA during configuration.

Pressing the PGM_CONFIG push button (S5) loads the FPGA with a design page based on which PGM_LED[2:0] (D12, D13, D14) illuminates. You can select the design stored in the flash by pressing the PGM_SEL push button (S6) to cycle through the LEDs as defined in Table 2–6.

Table 2–6 lists the design that loads when you press the PGM_CONFIG push button.

Table 2–6. PGM_LED Settings *(1)*

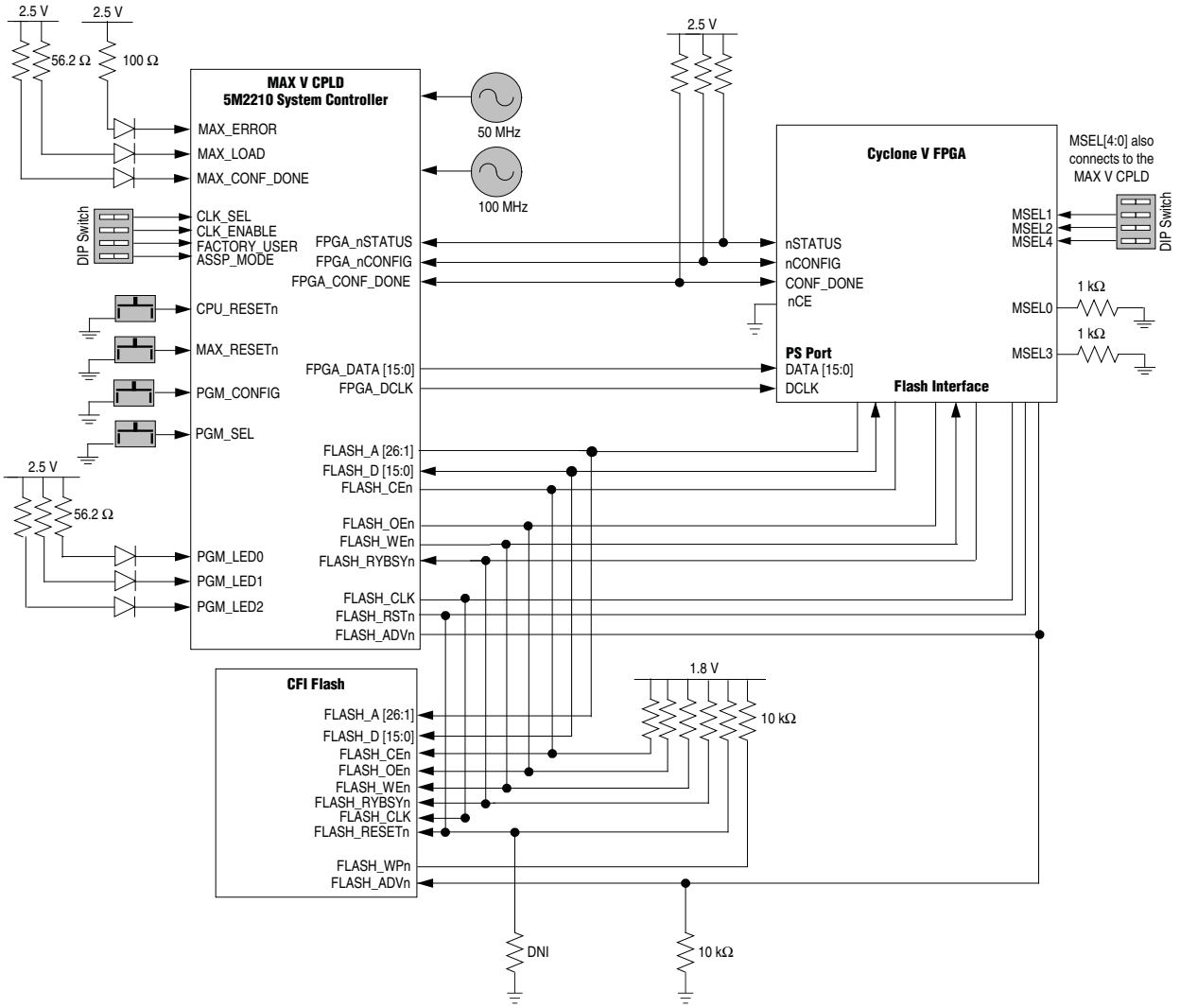
PGM_LED0 (D14)	PGM_LED1 (D13)	PGM_LED2 (D12)	Design
ON	OFF	OFF	Factory design
OFF	ON	OFF	User design 1
OFF	OFF	ON	User design 2

Note to Table 2–6:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Figure 2–4 shows the PFL configuration.

Figure 2–4. PFL Configuration



For more information on the following topics, refer to the respective documents:

- Board Update Portal, PFL design, and flash memory map storage, refer to the *Cyclone V GT FPGA Development Kit User Guide*.
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

Using the EPCQ Flash Memory

To enable FPGA configuration using the EPCQ device, you must reconfigure the MAX V device with a specific hardware design, which you can download.

For further information, refer to "Configuring the MAX V Device to Program EPCQ" on page 2–11.

FPGA Programming over External USB-Blaster

The JTAG chain header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. To prevent contention between the JTAG masters, the embedded USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG chain header.

Status Elements

The development board includes status LEDs. This section describes the status elements. Table 2–7 lists the LED board references, names, and functional descriptions.

Table 2–7. Board-Specific LEDs (Part 1 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D21	Power	5.0-V	Blue LED. Illuminates when 5.0 V power is active.
D7	MAX_CONF_DONE	2.5-V	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD 5M2210 System Controller.
D6	MAX_LOAD	2.5-V	Green LED. Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D5	MAX_ERROR	2.5-V	Red LED. Illuminates when the MAX V CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D14 D13 D12	PGM_LED[0] PGM_LED[1] PGM_LED[2]	2.5-V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM_SEL push button.
D27, D28 D29, D30	JTAG_RX, JTAG_TX SC_RX, SC_TX	2.5-V	Green LEDs. Illuminates to indicate USB-Blaster II receive and transmit activities.
D22	ENET_LED_TX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D23	ENET_LED_RX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D24	ENET_LED_LINK10	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D25	ENET_LED_LINK100	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D26	ENET_LED_LINK1000	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D32	SDI_RX_CDn	3.3-V	Green LED. Illuminates to indicate that input signal is detected at the SDI RX port. Driven by the SDI cable equalizer.

Table 2–7. Board-Specific LEDs (Part 2 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D3	HSMA_PRSNTn	3.3-V	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D2	HSMB_PRSNTn	3.3-V	Green LED. Illuminates when HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG chain control or PCI Express control DIP switch
- FPGA configuration mode DIP switch
- CPU reset push button
- MAX V reset push button
- Program configuration push button
- Program select push button

For more information about the default settings of the DIP switches, refer to the *Cyclone V GT FPGA Development Kit User Guide*.

Board Settings DIP Switch

The board settings DIP switch (SW4) controls various features specific to the board and the MAX V CPLD 5M2210 System Controller logic design. Table 2–8 lists the switch controls and descriptions.

Table 2–8. Board Settings DIP Switch Controls

Switch Position	Schematic Signal Name	Description
1	CLK_SEL	ON: Select programmable oscillator clock OFF: Select SMA input clock
2	CLK_ENABLE	ON: Disable on-board oscillator OFF: Enable on-board oscillator
3	FACTORY_USER	ON: Load the factory design at power up OFF: Load the user design from flash at power up
4	ASSP_MODE	Not used

JTAG Chain Control or PCI Express Control DIP Switch

The JTAG chain control DIP switch (SW3) either remove or include devices in the active JTAG chain. The Cyclone V GT FPGA is always in the JTAG chain. This switch also enables or disables different link width configurations for the PCI Express connector. Table 2–9 lists the switch controls and its descriptions.

Table 2–9. JTAG Chain Control DIP Switch

Switch Position	Schematic Signal Name	Description
1	PCIe_PRSNT2n_X1	ON: PCI Express edge connector in-chain and enable x1 presence detect OFF: Bypass PCI Express edge connector
2	PCIe_PRSNT2n_X4	ON: PCI Express edge connector in-chain and enable x4 presence detect OFF: Bypass PCI Express edge connector
3	HSMB_JTAG_EN	ON: Bypass HSMC port B OFF: HSMC port B in-chain
4	HSMA_JTAG_EN	ON: Bypass HSMC port A OFF: HSMC port A in-chain

FPGA Configuration Mode DIP Switch

The FPGA configuration mode DIP switch (SW5) defines the mode to use to configure the FPGA. Table 2–10 lists the switch controls and its descriptions.

Table 2–10. FPGA Configuration Mode DIP Switch

Switch Position	Schematic Signal Name	Description
1	FPGA_MSEL1	ON: Select logic 0 OFF: Select logic 1
2	FPGA_MSEL2	ON: Select logic 0 OFF: Select logic 1
3	FPGA_MSEL4	ON: Select logic 0 OFF: Select logic 1
4	FORCE_FAN	Optional fan control function to add into the MAX V CPLD System Controller. Not used by default.

CPU Reset Push Button

The CPU reset push button, CPU_RESETn (S4), is an input to the Cyclone V GT DEV_CLRn pin and is an open-drain I/O from the MAX V CPLD System Controller. This push button is the default reset for both the FPGA and CPLD logic. The MAX V CPLD 5M2210 System Controller also drives this push button during power-on-reset (POR).

MAX V Reset Push Button

The MAX V reset push button, MAX_RESETn (S7), is an input to the MAX V CPLD 5M2210 System Controller. This push button is the default reset for the CPLD logic.

Program Configuration Push Button

The program configuration push button, PGM_CONFIG (S5), is an input to the MAX V CPLD 5M2210 System Controller. This input forces a FPGA reconfiguration from the flash memory. The location in the flash memory is based on the settings of PGM_LED[2:0], which is controlled by the program select push button, PGM_SEL. Valid settings include PGM_LED0, PGM_LED1, or PGM_LED2 on the three pages in flash memory reserved for FPGA designs.

Program Select Push Button

The program select push button, PGM_SEL (S6), is an input to the MAX V CPLD System Controller. This push button toggles the PGM_LED[2:0] sequence that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–6 for the PGM_LED[2:0] sequence definitions.

Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

The development board includes oscillators with a frequency of 50 MHz, 125 MHz, 148.50 MHz, and two programmable oscillators with a default frequencies of 100 MHz. The programmable oscillators have a frequency range from 10–810 MHz and can be programmed through the clock control application in the **examples/board_test_system** directory.

Figure 2–5 shows the default frequencies of all external clocks going to the Cyclone V GT FPGA on the development board.

Figure 2–5. Cyclone V GT FPGA Development Board Clocks

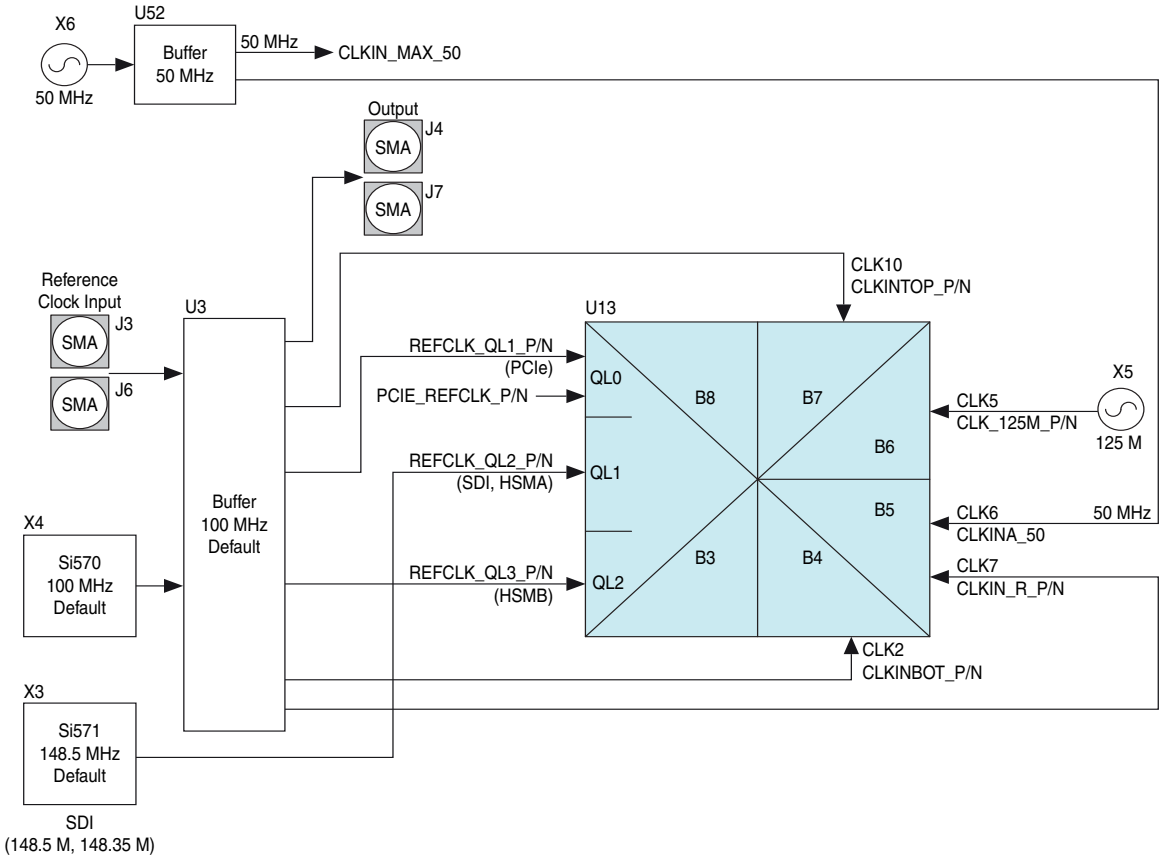


Table 2–11 lists the oscillators, its I/O standard, and voltages required for the development board.

Table 2–11. On-Board Oscillators (Part 1 of 2)

Source	Schematic Signal Name	Frequency	I/O Standard	Cyclone V GT Pin Number	Application
X6	CLKIN_50	50.000 MHz	1.5-V CMOS	V28	FPGA bank 5B (CLK6p) for general purpose logic
	CLKIN_MAX_50			—	FPGA bank 5B (CLK6p) for general purpose logic in the MAX V CPLD
X5	CLK_125M_P	125.000 MHz	LVDS	U31	FPGA bank 6A (CLK5p)
	CLK_125M_N			U30	FPGA bank 6A (CLK5n)

Table 2–11. On-Board Oscillators (Part 2 of 2)

Source	Schematic Signal Name	Frequency	I/O Standard	Cyclone V GT Pin Number	Application
X4 to U3	CLKINTOP_P	100.000 MHz (Programmable between 10–810 MHz)	LVDS (fanout buffer)	H19	Top edge (CLK10p) for general purpose logic
	CLKINTOP_N			H18	Top edge (CLK10n) for general purpose logic
	CLKINBOT_P			AF18	Bottom edge (CLK2p)
	CLKINBOT_N			AG18	Bottom edge (CLK2n)
	CLKIN_R_P			W26	Right edge (CLK7p) for general purpose logic
	CLKIN_R_N			W27	Right edge (CLK7n) for general purpose logic
	REFCLK_QL1_P			AA11	Transceiver bank QL0 for PCI Express edge connector
	REFCLK_QL1_N			AB10	
	REFCLK_QL3_P			R11	Transceiver bank QL3 for HSMC port B transceivers
	REFCLK_QL3_N			P10	
	SMA_CLKOUT_P			—	Oscilloscope trigger output
	SMA_CLKOUT_N			—	
X3	REFCLK_QL2_P	148.500 MHz (Programmable between 10–810 MHz)	LVDS	U11	SDI video or HSMC port A transceivers
	REFCLK_QL2_N			T10	
X1	ENET_XTAL_25MHZ	25.000 MHz	2.5-V CMOS	—	Reference clock for the Ethernet PHY

Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–12 lists the clock inputs for the development board.

Table 2–12. Off-Board Clock Inputs (Part 1 of 2)

Source	Schematic Signal Name	I/O Standard	Cyclone V GT Pin Number	Description
SMA	CLKIN_SMA_P	LVPECL	—	Input to LVDS fan-out buffer (drives two reference clocks and three GPLL inputs)
	CLKIN_SMA_N	LVPECL	—	
Samtec HSMC	HSMA_CLK_IN0	2.5-V	G11	Single-ended input from the installed HSMC cable or board.
	HSMA_CLK_IN_P1	LVDS/2.5-V	G18	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N1	LVDS/LVTTL	F18	
	HSMA_CLK_IN_P2	LVDS/LVTTL	H17	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N2	LVDS/LVTTL	H16	

Table 2–12. Off-Board Clock Inputs (Part 2 of 2)

Source	Schematic Signal Name	I/O Standard	Cyclone V GT Pin Number	Description
Samtec HSMC	HSMB_CLK_IN0	2.5-V	A22	Single-ended input from the installed HSMC cable or board.
	HSMB_CLK_IN_P1	LVDS/2.5-V	K25	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMB_CLK_IN_N1	LVDS/LVTTL	J25	
	HSMB_CLK_IN_P2	LVDS/LVTTL	J20	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMB_CLK_IN_N2	LVDS/LVTTL	K19	
PCI Express Edge	PCIE_REFCLK_P	HCSL	W11	HCSL input from the PCI Express edge connector.
	PCIE_REFCLK_N	HCSL	V10	

Table 2–13 lists the clock outputs for the development board.

Table 2–13. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Cyclone V GT Pin Number	Description
LVDS SMA	CLKOUT_SMA_P	LVPECL	—	Driven from LVDS clock buffer U3
	CLKOUT_SMA_N	LVPECL	—	
Samtec HSMC	HSMA_CLK_OUT0	2.5V CMOS	F10	FPGA CMOS output (or GPIO)
	HSMA_CLK_OUT_P1	LVDS/2.5V CMOS	C1	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N1	LVDS/2.5V CMOS	B1	
	HSMA_CLK_OUT_P2	LVDS/2.5V CMOS	B18	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N2	LVDS/2.5V CMOS	A18	
Samtec HSMC	HSMB_CLK_OUT0	2.5V CMOS	D25	FPGA CMOS output (or GPIO)
	HSMB_CLK_OUT_P1	LVDS/2.5V CMOS	L22	LVDS output. Can also support 2x CMOS outputs.
	HSMB_CLK_OUT_N1	LVDS/2.5V CMOS	K22	
	HSMB_CLK_OUT_P2	LVDS/2.5V CMOS	F26	LVDS output. Can also support 2x CMOS outputs.
	HSMB_CLK_OUT_N2	LVDS/2.5V CMOS	G26	
SMA	SMA_CLKOUT	2.5V CMOS	AF33	FPGA CMOS output (or GPIO)

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, LEDs, and character LCD.

User-Defined Push Buttons

The development board includes three user-defined push buttons. For information on the system and safe reset push buttons, refer to "Setup Elements" on page 2–17.

Board references S1, S2, and S3 are push buttons for controlling the FPGA designs that loads into the Cyclone V GT device. When you press and hold down the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–14 lists the user-defined push button schematic signal names and their corresponding Cyclone V GT device pin numbers.

Table 2–14. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard
S3	USER_PB0	AK13	2.5-V
S2	USER_PB1	AA15	2.5-V
S1	USER_PB2	AN8	2.5-V

User-Defined DIP Switch

Board reference SW1 is a eight-pin DIP switch. This switch is user-defined and provides additional FPGA input control. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected. There are no board-specific functions for this switch.

Table 2–15 lists the user-defined DIP switch schematic signal names and their corresponding Cyclone V GT device pin numbers.

Table 2–15. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard
1	USER_DIPSW0	H12	2.5-V
2	USER_DIPSW1	A2	2.5-V
3	USER_DIPSW2	E10	2.5-V
4	USER_DIPSW3	D9	2.5-V
5	USER_DIPSW4	E9	2.5-V
6	USER_DIPSW5	D7	2.5-V
7	USER_DIPSW6	E8	2.5-V
8	USER_DIPSW7	E7	2.5-V

User-Defined LEDs

The development board includes general and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to "Status Elements" on page 2–15.

General LEDs

Board references D8–D11 and D15–D18 are eight user-defined LEDs. The status and debugging signals are driven to the LEDs from the designs loaded into the Cyclone V GT device. Driving a logic 0 on the I/O port turns the LED on while driving a logic 1 turns the LED off. There are no board-specific functions for these LEDs.

Table 2–16 lists the general LED schematic signal names and their corresponding Cyclone V GT device pin numbers.

Table 2–16. General LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard
D18	USER_LED0	AM23	1.5-V
D17	USER_LED1	AE25	1.5-V
D16	USER_LED2	AK29	1.5-V
D15	USER_LED3	AL31	1.5-V
D11	USER_LED4	AF25	1.5-V
D10	USER_LED5	AJ27	1.5-V
D9	USER_LED6	AC22	1.5-V
D8	USER_LED7	AH27	1.5-V

HSMC LEDs

Board references D3, D4, D19, and D20 are LEDs for the HSMC port. There are no board-specific functions for the HSMC LEDs. The LEDs are labeled TX and RX, and are intended to display data flow to and from the connected daughtercards. The LEDs are driven by the Cyclone V GT device.

Table 2–17 lists the HSMC LED schematic signal names and their corresponding Cyclone V GT device pin numbers.

Table 2–17. HSMC LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard
D19	HSMA_RX_LED	D12	2.5-V
D20	HSMA_TX_LED	B3	2.5-V
D3	HSMB_RX_LED	B30	2.5-V
D4	HSMB_TX_LED	C24	2.5-V

PCI Express LEDs

Board references D34, D45, D35, and D44 are PCI Express LEDs for link width indication. There are no board-specific functions for the PCI Express LEDs. You can configure the LEDs to display the functions as listed in Table 2–18. The LEDs are driven by the Cyclone V GT device.

Table 2–18 lists the PCI Express LED schematic signal names and their corresponding Cyclone V GT device pin numbers.

Table 2–18. PCI Express LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
D35, D44	PCIE_LED_X1	AK19	2.5-V	Green LED. Configure this LED to display the PCI Express link width x1.
D34, D45	PCIE_LED_X4	AD22	2.5-V	Green LED. Configure this LED to display the PCI Express link width x4.

Character LCD

The development board includes a single 10-pin 0.1" pitch single-row header that interfaces to a 2 line × 16 character character LCD. The character LCD has a 10-pin receptacle that mounts directly to the board's 10-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or for I^2C expansion.

Table 2–19 summarizes the character LCD pin assignments.

Table 2–19. Character LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J10)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
5	DISP_SPISS	AH13	2.5-V	SPI slave select (only used in SPI mode)
7	DISP_I2C_SCL	AL6	2.5-V	I^2C LCD serial clock
8	DISP_I2C_SDA	AJ10	2.5-V	I^2C LCD serial data

For more information such as timing, character maps, interface guidelines, and other documents related to the character LCD, visit www.newhavendisplay.com.

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Cyclone V GT device. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- HSMC
- SDI video output/input

PCI Express

The Cyclone V GT FPGA development board is designed to fit entirely into a PC motherboard with a ×4 PCI Express slot that can accommodate a full height short form factor add-in card. This interface uses the Cyclone V GT's PCI Express hard IP block, saving logic resources for the user logic application. The PCI express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

The PCI Express interface supports auto-negotiating channel width from ×1 to ×4 by using Altera's PCIe MegaCore IP. You can also configure this board to a ×1 or ×4 interface through a DIP switch that connects the PRSNTn pins for each bus width.

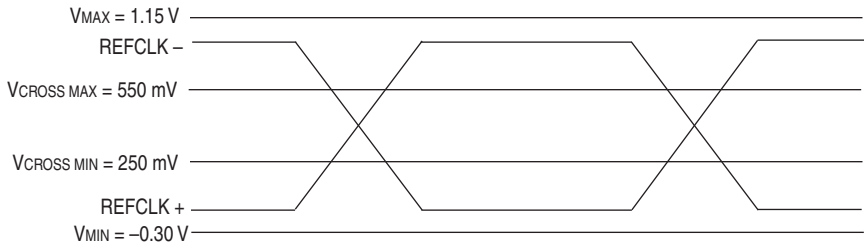
The PCI Express interface has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps in full-duplex (Gen1) and 5.0 Gbps/lane for a maximum of 40 Gbps in full-duplex (Gen2).

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, Altera recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_REFCLK_P/N signal is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This signal connects directly to a Cyclone V GT REFCLK input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–6 shows the PCI Express reference clock levels.

Figure 2–6. PCI Express Reference Clock Levels



The SMB connections are optional signals in the PCI Express specification. The signals are wired to the Cyclone V GT device but are not required for normal operation.

Table 2–20 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Cyclone V GT device.

Table 2–20. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (J16)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
A11	PCIE_PERSTN	AA22	LVTTL	Reset
A1	PCIE_PRSNT1N	—	LVTTL	Link width DIP switch
B17	PCIE_PRSNT2N_X1	—	LVTTL	Hot plug present detect
B31	PCIE_PRSNT2N_X4	—	LVTTL	Hot plug present detect
A13	PCIE_REFCLK_P	W11	HCSL	Reference clock input
A14	PCIE_REFCLK_N	V10	HCSL	Reference clock input
B14	PCIE_RX_P0	AJ2	1.5-V PCML	Receive bus
B15	PCIE_RX_N0	AJ1	1.5-V PCML	Receive bus
B19	PCIE_RX_P1	AG2	1.5-V PCML	Receive bus
B20	PCIE_RX_N1	AG1	1.5-V PCML	Receive bus
B23	PCIE_RX_P2	AE2	1.5-V PCML	Receive bus
B24	PCIE_RX_N2	AE1	1.5-V PCML	Receive bus
B27	PCIE_RX_P3	AC2	1.5-V PCML	Receive bus

Table 2–20. PCI Express Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (J16)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
B28	PCIE_RX_N3	AC1	1.5-V PCML	Receive bus
B5	PCIE_SMBCLK	AP5	LVTTL	SMB clock
B6	PCIE_SMBDAT	AJ12	LVTTL	SMB data
A16	PCIE_TX_P0	AH4	1.5-V PCML	Transmit bus
A17	PCIE_TX_N0	AH3	1.5-V PCML	Transmit bus
A21	PCIE_TX_P1	AF4	1.5-V PCML	Transmit bus
A22	PCIE_TX_N1	AF3	1.5-V PCML	Transmit bus
A25	PCIE_TX_P2	AD4	1.5-V PCML	Transmit bus
A26	PCIE_TX_N2	AD3	1.5-V PCML	Transmit bus
A29	PCIE_TX_P3	AB4	1.5-V PCML	Transmit bus
A30	PCIE_TX_N3	AB3	1.5-V PCML	Transmit bus
B11	PCIE_WAKEn	AP6	LVTTL	Wake signal

10/100/1000 Ethernet

The development board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs a RGMII interface. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses 2.5-V and 1.0-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a RJ45 model with internal magnetics for driving copper lines with Ethernet traffic.

Figure 2–7 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–7. RGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

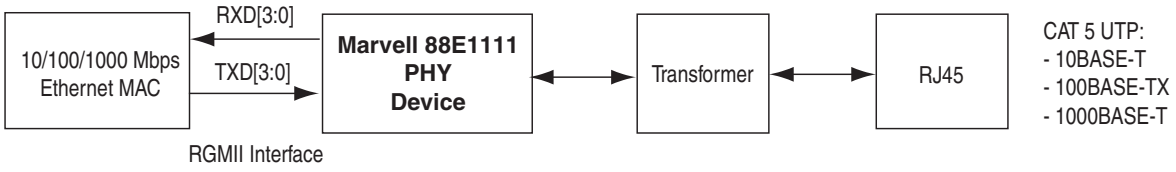


Table 2–21 lists the Ethernet PHY interface pin assignments.

Table 2–21. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U11)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
8	ENET_GTX_CLK	AP7	2.5-V CMOS	125-MHz RGMII transmit clock
23	ENET_INTN	AK10	2.5-V CMOS	Management bus interrupt
60	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex or collision LED. Not used
70	ENET_LED_DUPLEX	—	2.5-V CMOS	Duplex or collision LED. Not used

Table 2–21. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U11)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
76	ENET_LED_LINK10	—	2.5-V CMOS	10-Mb link LED
74	ENET_LED_LINK100	—	2.5-V CMOS	100-Mb link LED
73	ENET_LED_LINK1000	—	2.5-V CMOS	1000-Mb link LED
58	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
69	ENET_LED_RX	—	2.5-V CMOS	RX data active LED
68	ENET_LED_TX	—	2.5-V CMOS	TX data active LED
25	ENET_MDC	AM8	2.5-V CMOS	Management bus data clock
24	ENET_MDIO	AG14	2.5-V CMOS	Management bus data
28	ENET_RESETN	AN9	2.5-V CMOS	Device reset
2	ENET_RX_CLK	AM10	2.5-V CMOS	RGMII receive clock
95	ENET_RX_D0	AK14	2.5-V CMOS	RGMII receive data bus
92	ENET_RX_D1	AL10	2.5-V CMOS	RGMII receive data bus
93	ENET_RX_D2	AJ14	2.5-V CMOS	RGMII receive data bus
91	ENET_RX_D3	AK12	2.5-V CMOS	RGMII receive data bus
94	ENET_RX_DV	AH14	2.5-V CMOS	RGMII receive data valid
11	ENET_TX_D0	AB14	2.5-V CMOS	RGMII transmit data bus
12	ENET_TX_D1	AD15	2.5-V CMOS	RGMII transmit data bus
14	ENET_TX_D2	AB15	2.5-V CMOS	RGMII transmit data bus
16	ENET_TX_D3	AB13	2.5-V CMOS	RGMII transmit data bus
9	ENET_TX_EN	AC14	2.5-V CMOS	RGMII transmit enable
55	ENET_XTAL_25MHZ	—	2.5-V CMOS	25-MHz RGMII transmit clock
29	MDI_P0	—	2.5-V CMOS	Media dependent interface
31	MDI_N0	—	2.5-V CMOS	Media dependent interface
33	MDI_P1	—	2.5-V CMOS	Media dependent interface
34	MDI_N1	—	2.5-V CMOS	Media dependent interface
39	MDI_P2	—	2.5-V CMOS	Media dependent interface
41	MDI_N2	—	2.5-V CMOS	Media dependent interface
42	MDI_P3	—	2.5-V CMOS	Media dependent interface
43	MDI_N3	—	2.5-V CMOS	Media dependent interface

HSMC

The development board supports two HSMC interfaces. Each physical interface provides four channels of 5.0 Gbps-capable transceivers. The HSMC port A interface supports both single-ended and differential signaling. The HSMC port B is a new DQS standard to support both single-ended signaling and external memory interfaces.

The HSMC port A interface supports a full SPI4.2 interface (17 LVDS channels), three input and output clocks, as well as JTAG and SMB signals. The LVDS channels can be used for CMOS signaling or LVDS.

The HSMC port B interface, other than supporting three input and output clocks as well as SMBus and JTAG signals, it also covers the new DQS standard to support daughtercards with external memory devices. For memory support, the VCCIO banks for the HSMC port B is adjustable between 1.2 V, 1.5 V, 1.8 V, and 2.5 V. When the DQS features are not used, these channels can be used for CMOS signaling.

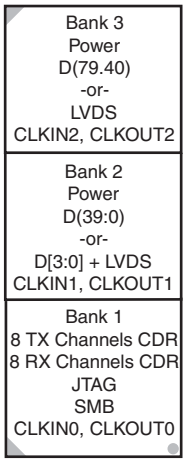
The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–8 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–8. HSMC Signal and Bank Diagram



The HSMC interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

☞ As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–22 lists the HSMC interface pin assignments, signal names, and functions.

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
HSMC Port A (J1)				
17	HSMA_TX_P3	P4	1.5-V PCML	Transceiver TX bit 3
18	HSMA_RX_P3	R2	1.5-V PCML	Transceiver RX bit 3
19	HSMA_TX_N3	P3	1.5-V PCML	Transceiver TX bit 3n
20	HSMA_RX_N3	R1	1.5-V PCML	Transceiver RX bit 3n
21	HSMA_TX_P2	T4	1.5-V PCML	Transceiver TX bit 2
22	HSMA_RX_P2	U2	1.5-V PCML	Transceiver RX bit 2
23	HSMA_TX_N2	T3	1.5-V PCML	Transceiver TX bit 2n
24	HSMA_RX_N2	U1	1.5-V PCML	Transceiver RX bit 2n
25	HSMA_TX_P1	V4	1.5-V PCML	Transceiver TX bit 1
26	HSMA_RX_P1	W2	1.5-V PCML	Transceiver RX bit 1
27	HSMA_TX_N1	V3	1.5-V PCML	Transceiver TX bit 1n
28	HSMA_RX_N1	W1	1.5-V PCML	Transceiver RX bit 1n
29	HSMA_TX_P0	Y4	1.5-V PCML	Transceiver TX bit 0
30	HSMA_RX_P0	AA2	1.5-V PCML	Transceiver RX bit 0
31	HSMA_TX_N0	Y3	1.5-V PCML	Transceiver TX bit 0n
32	HSMA_RX_N0	AA1	1.5-V PCML	Transceiver RX bit 0n
33	HSMA_SDA	K13	2.5-V CMOS	Management serial data
34	HSMA_SCL	E12	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AK5	2.5-V CMOS	JTAG clock signal
36	HSMA_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMA_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	JTAG_FPGA_TDO	AF11	2.5-V CMOS	JTAG data input
39	HSMA_CLK_OUT0	F10	2.5-V CMOS	Dedicated CMOS clock out
40	HSMA_CLK_IN0	G11	2.5-V CMOS	Dedicated CMOS clock in
41	HSMA_D0	L12	2.5-V CMOS	Dedicated CMOS I/O bit 0
42	HSMA_D1	F11	2.5-V CMOS	Dedicated CMOS I/O bit 1
43	HSMA_D2	F12	2.5-V CMOS	Dedicated CMOS I/O bit 2
44	HSMA_D3	K12	2.5-V CMOS	Dedicated CMOS I/O bit 3
47	HSMA_TX_D_P0	B4	LVDS or 2.5-V	LVDS TX bit 0 or CMOS bit 4

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
48	HSMA_RX_D_P0	P14	LVDS or 2.5-V	LVDS RX bit 0 or CMOS bit 5
49	HSMA_TX_D_N0	A3	LVDS or 2.5-V	LVDS TX bit 0n or CMOS bit 6
50	HSMA_RX_D_N0	N14	LVDS or 2.5-V	LVDS RX bit 0n or CMOS bit 7
53	HSMA_TX_D_P1	C9	LVDS or 2.5-V	LVDS TX bit 1 or CMOS bit 8
54	HSMA_RX_D_P1	M15	LVDS or 2.5-V	LVDS RX bit 1 or CMOS bit 9
55	HSMA_TX_D_N1	B9	LVDS or 2.5-V	LVDS TX bit 1n or CMOS bit 10
56	HSMA_RX_D_N1	M14	LVDS or 2.5-V	LVDS RX bit 1n or CMOS bit 11
59	HSMA_TX_D_P2	B5	LVDS or 2.5-V	LVDS TX bit 2 or CMOS bit 12
60	HSMA_RX_D_P2	M13	LVDS or 2.5-V	LVDS RX bit 2 or CMOS bit 13
61	HSMA_TX_D_N2	A5	LVDS or 2.5-V	LVDS TX bit 2n or CMOS bit 14
62	HSMA_RX_D_N2	L13	LVDS or 2.5-V	LVDS RX bit 2n or CMOS bit 15
65	HSMA_TX_D_P3	A12	LVDS or 2.5-V	LVDS TX bit 3 or CMOS bit 16
66	HSMA_RX_D_P3	N13	LVDS or 2.5-V	LVDS RX bit 3 or CMOS bit 17
67	HSMA_TX_D_N3	A11	LVDS or 2.5-V	LVDS TX bit 3n or CMOS bit 18
68	HSMA_RX_D_N3	N12	LVDS or 2.5-V	LVDS RX bit 3n or CMOS bit 19
71	HSMA_TX_D_P4	C6	LVDS or 2.5-V	LVDS TX bit 4 or CMOS bit 20
72	HSMA_RX_D_P4	M16	LVDS or 2.5-V	LVDS RX bit 4 or CMOS bit 21
73	HSMA_TX_D_N4	B6	LVDS or 2.5-V	LVDS TX bit 4n or CMOS bit 22
74	HSMA_RX_D_N4	L17	LVDS or 2.5-V	LVDS RX bit 4n or CMOS bit 23
77	HSMA_TX_D_P5	C13	LVDS or 2.5-V	LVDS TX bit 5 or CMOS bit 24
78	HSMA_RX_D_P5	B8	LVDS or 2.5-V	LVDS RX bit 5 or CMOS bit 25
79	HSMA_TX_D_N5	C12	LVDS or 2.5-V	LVDS TX bit 5n or CMOS bit 26
80	HSMA_RX_D_N5	A8	LVDS or 2.5-V	LVDS RX bit 5n or CMOS bit 27
83	HSMA_TX_D_P6	A7	LVDS or 2.5-V	LVDS TX bit 6 or CMOS bit 28
84	HSMA_RX_D_P6	J15	LVDS or 2.5-V	LVDS RX bit 6 or CMOS bit 29
85	HSMA_TX_D_N6	A6	LVDS or 2.5-V	LVDS TX bit 6n or CMOS bit 30
86	HSMA_RX_D_N6	K14	LVDS or 2.5-V	LVDS RX bit 6n or CMOS bit 31
89	HSMA_TX_D_P7	C8	LVDS or 2.5-V	LVDS TX bit 7 or CMOS bit 32
90	HSMA_RX_D_P7	H14	LVDS or 2.5-V	LVDS RX bit 7 or CMOS bit 33
91	HSMA_TX_D_N7	C7	LVDS or 2.5-V	LVDS TX bit 7n or CMOS bit 34
92	HSMA_RX_D_N7	G14	LVDS or 2.5-V	LVDS RX bit 7n or CMOS bit 35
95	HSMA_CLK_OUT_P1	C1	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMA_CLK_IN_P1	G18	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMA_CLK_OUT_N1	B1	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38
98	HSMA_CLK_IN_N1	F18	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMA_TX_D_P8	D11	LVDS or 2.5-V	LVDS TX bit 8 or CMOS bit 40
102	HSMA_RX_D_P8	E15	LVDS or 2.5-V	LVDS RX bit 8 or CMOS bit 41
103	HSMA_TX_D_N8	D10	LVDS or 2.5-V	LVDS TX bit 8n or CMOS bit 42
104	HSMA_RX_D_N8	D15	LVDS or 2.5-V	LVDS RX bit 8n or CMOS bit 43

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
107	HSMA_TX_D_P9	B10	LVDS or 2.5-V	LVDS TX bit 9 or CMOS bit 44
108	HSMA_RX_D_P9	F15	LVDS or 2.5-V	LVDS RX bit 9 or CMOS bit 45
109	HSMA_TX_D_N9	A10	LVDS or 2.5-V	LVDS TX bit 9n or CMOS bit 46
110	HSMA_RX_D_N9	G15	LVDS or 2.5-V	LVDS RX bit 9n or CMOS bit 47
113	HSMA_TX_D_P10	B13	LVDS or 2.5-V	LVDS TX bit 10 or CMOS bit 48
114	HSMA_RX_D_P10	E18	LVDS or 2.5-V	LVDS RX bit 10 or CMOS bit 49
115	HSMA_TX_D_N10	A13	LVDS or 2.5-V	LVDS TX bit 10n or CMOS bit 50
116	HSMA_RX_D_N10	E17	LVDS or 2.5-V	LVDS RX bit 10n or CMOS bit 51
119	HSMA_TX_D_P11	C11	LVDS or 2.5-V	LVDS TX bit 11 or CMOS bit 52
120	HSMA_RX_D_P11	G13	LVDS or 2.5-V	LVDS RX bit 11 or CMOS bit 53
121	HSMA_TX_D_N11	B11	LVDS or 2.5-V	LVDS TX bit 11n or CMOS bit 54
122	HSMA_RX_D_N11	H13	LVDS or 2.5-V	LVDS RX bit 11n or CMOS bit 55
125	HSMA_TX_D_P12	C14	LVDS or 2.5-V	LVDS TX bit 12 or CMOS bit 56
126	HSMA_RX_D_P12	E14	LVDS or 2.5-V	LVDS RX bit 12 or CMOS bit 57
127	HSMA_TX_D_N12	B14	LVDS or 2.5-V	LVDS TX bit 12n or CMOS bit 58
128	HSMA_RX_D_N12	D14	LVDS or 2.5-V	LVDS RX bit 12n or CMOS bit 59
131	HSMA_TX_D_P13	F13	LVDS or 2.5-V	LVDS TX bit 13 or CMOS bit 60
132	HSMA_RX_D_P13	C16	LVDS or 2.5-V	LVDS RX bit 13 or CMOS bit 61
133	HSMA_TX_D_N13	E13	LVDS or 2.5-V	LVDS TX bit 13n or CMOS bit 62
134	HSMA_RX_D_N13	B16	LVDS or 2.5-V	LVDS RX bit 13n or CMOS bit 63
137	HSMA_TX_D_P14	A17	LVDS or 2.5-V	LVDS TX bit 14 or CMOS bit 64
138	HSMA_RX_D_P14	D17	LVDS or 2.5-V	LVDS RX bit 14 or CMOS bit 65
139	HSMA_TX_D_N14	A16	LVDS or 2.5-V	LVDS TX bit 14n or CMOS bit 66
140	HSMA_RX_D_N14	D16	LVDS or 2.5-V	LVDS RX bit 14n or CMOS bit 67
143	HSMA_TX_D_P15	B15	LVDS or 2.5-V	LVDS TX bit 15 or CMOS bit 68
144	HSMA_RX_D_P15	L16	LVDS or 2.5-V	LVDS RX bit 15 or CMOS bit 69
145	HSMA_TX_D_N15	A15	LVDS or 2.5-V	LVDS TX bit 15n or CMOS bit 70
146	HSMA_RX_D_N15	L15	LVDS or 2.5-V	LVDS RX bit 15n or CMOS bit 71
149	HSMA_TX_D_P16	C18	LVDS or 2.5-V	LVDS TX bit 16 or CMOS bit 72
150	HSMA_RX_D_P16	F17	LVDS or 2.5-V	LVDS RX bit 16 or CMOS bit 73
151	HSMA_TX_D_N16	C17	LVDS or 2.5-V	LVDS TX bit 16n or CMOS bit 74
152	HSMA_RX_D_N16	F16	LVDS or 2.5-V	LVDS RX bit 16n or CMOS bit 75
155	HSMA_CLK_OUT_P2	B18	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76
156	HSMA_CLK_IN_P2	H17	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMA_CLK_OUT_N2	A18	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78
158	HSMA_CLK_IN_N2	H16	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
160	HSMA_PRSNTn	L11	2.5-V CMOS	HSMC port A presence detect
HSMC Port B (J2)				
17	HSMB_TX_P3	F4	1.5-V PCML	Transceiver TX bit 3

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
18	HSMB_RX_P3	G2	1.5-V PCML	Transceiver RX bit 3
19	HSMB_TX_N3	F3	1.5-V PCML	Transceiver TX bit 3n
20	HSMB_RX_N3	G1	1.5-V PCML	Transceiver RX bit 3n
21	HSMB_TX_P2	H4	1.5-V PCML	Transceiver TX bit 2
22	HSMB_RX_P2	J2	1.5-V PCML	Transceiver RX bit 2
23	HSMB_TX_N2	H3	1.5-V PCML	Transceiver TX bit 2n
24	HSMB_RX_N2	J1	1.5-V PCML	Transceiver RX bit 2n
25	HSMB_TX_P1	K4	1.5-V PCML	Transceiver TX bit 1
26	HSMB_RX_P1	L2	1.5-V PCML	Transceiver RX bit 1
27	HSMB_TX_N1	K3	1.5-V PCML	Transceiver TX bit 1n
28	HSMB_RX_N1	L1	1.5-V PCML	Transceiver RX bit 1n
29	HSMB_TX_P0	M4	1.5-V PCML	Transceiver TX bit 0
30	HSMB_RX_P0	N2	1.5-V PCML	Transceiver RX bit 0
31	HSMB_TX_N0	M3	1.5-V PCML	Transceiver TX bit 0n
32	HSMB_RX_N0	N1	1.5-V PCML	Transceiver RX bit 0n
33	HSMB_SDA	L20	2.5-V CMOS	Management serial data
34	HSMB_SCL	E27	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AK5	2.5-V CMOS	JTAG clock signal
36	HSMB_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMB_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	HSMB_JTAG_TDI	—	2.5-V CMOS	JTAG data input
39	HSMB_CLK_OUT0	D25	2.5-V CMOS	Dedicated CMOS clock out
40	HSMB_CLK_IN0	A22	2.5-V CMOS	Dedicated CMOS clock in
41	HSMB_WEn	B24	2.5-V CMOS	Write enable
42	HSMB_RASn	A23	2.5-V CMOS	Row address select
43	HSMB_ADDR_CMD0	L18	2.5-V CMOS	Memory address or command
44	HSMB_CASn	C21	2.5-V CMOS	Column address select
47	HSMB_DQ0	E22	2.5-V CMOS	Memory data bus
49	HSMB_DQ1	G20	2.5-V CMOS	Memory data bus
53	HSMB_DQ2	F20	2.5-V CMOS	Memory data bus
55	HSMB_DQ3	D24	2.5-V CMOS	Memory data bus
59	HSMB_DQ4	C26	2.5-V CMOS	Memory data bus
61	HSMB_DQ5	G21	2.5-V CMOS	Memory data bus
65	HSMB_DQ6	F21	2.5-V CMOS	Memory data bus
67	HSMB_DQ7	D27	2.5-V CMOS	Memory data bus
71	HSMB_DQ8	F23	2.5-V CMOS	Memory data bus
73	HSMB_DQ9	C29	2.5-V CMOS	Memory data bus
77	HSMB_DQ10	E24	2.5-V CMOS	Memory data bus
79	HSMB_DQ11	H21	2.5-V CMOS	Memory data bus

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
83	HSMB_DQ12	H22	2.5-V CMOS	Memory data bus
85	HSMB_DQ13	B28	2.5-V CMOS	Memory data bus
89	HSMB_DQ14	D26	2.5-V CMOS	Memory data bus
91	HSMB_DQ15	F22	2.5-V CMOS	Memory data bus
95	HSMB_CLK_OUT_P1	L22	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMB_CLK_IN_P1	K25	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMB_CLK_OUT_N1	K22	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38
98	HSMB_CLK_IN_N1	J25	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMB_DQ16	F27	2.5-V CMOS	Memory data bus
103	HSMB_DQ17	G23	2.5-V CMOS	Memory data bus
107	HSMB_DQ18	H23	2.5-V CMOS	Memory data bus
109	HSMB_DQ19	B31	2.5-V CMOS	Memory data bus
113	HSMB_DQ20	E28	2.5-V CMOS	Memory data bus
115	HSMB_DQ21	D29	2.5-V CMOS	Memory data bus
119	HSMB_DQ22	D30	2.5-V CMOS	Memory data bus
121	HSMB_DQ23	C32	2.5-V CMOS	Memory data bus
125	HSMB_DQ24	H26	2.5-V CMOS	Memory data bus
127	HSMB_DQ25	G25	2.5-V CMOS	Memory data bus
131	HSMB_DQ26	G28	2.5-V CMOS	Memory data bus
133	HSMB_DQ27	F25	2.5-V CMOS	Memory data bus
137	HSMB_DQ28	G29	2.5-V CMOS	Memory data bus
139	HSMB_DQ29	H24	2.5-V CMOS	Memory data bus
143	HSMB_DQ30	G24	2.5-V CMOS	Memory data bus
145	HSMB_DQ31	F30	2.5-V CMOS	Memory data bus
149	HSMB_C_P	M18	2.5-V CMOS	Memory OVLD
151	HSMB_C_N	E19	2.5-V CMOS	Memory ODT
155	HSMB_CLK_OUT_P2	F26	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76
156	HSMB_CLK_IN_P2	J20	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMB_CLK_OUT_N2	G26	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78
158	HSMB_CLK_IN_N2	K19	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
48	HSMB_DM0	C27	2.5-V CMOS	Data mask
50	HSMB_A0	E23	2.5-V CMOS	Memory address bus
54	HSMB_A1	B25	2.5-V CMOS	Memory address bus
56	HSMB_A2	A28	2.5-V CMOS	Memory address bus
60	HSMB_A3	A26	2.5-V CMOS	Memory address bus
62	HSMB_A4	D21	2.5-V CMOS	Memory address bus
72	HSMB_DM1	C28	2.5-V CMOS	Memory address bus
74	HSMB_A5	C23	2.5-V CMOS	Memory address bus
78	HSMB_A6	E29	2.5-V CMOS	Memory address bus

Table 2–22. HSMC Interface Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
80	HSMB_A7	D22	2.5-V CMOS	Memory address bus
84	HSMB_A8	D19	2.5-V CMOS	Memory address bus
86	HSMB_A9	B21	2.5-V CMOS	Memory address bus
102	HSMB_DM2	C31	2.5-V CMOS	Data mask
104	HSMB_A10	E20	2.5-V CMOS	Memory address bus
108	HSMB_A11	B23	2.5-V CMOS	Memory address bus
110	HSMB_A12	L25	2.5-V CMOS	Memory address bus
114	HSMB_A13	B19	2.5-V CMOS	Memory address bus
116	HSMB_A14	B20	2.5-V CMOS	Memory address bus
126	HSMB_DM3	H27	2.5-V CMOS	Data mask
128	HSMB_A15	A21	2.5-V CMOS	Memory address bus
132	HSMB_BA0	B26	2.5-V CMOS	Memory bank address bus
134	HSMB_BA1	A27	2.5-V CMOS	Memory bank address bus
138	HSMB_BA2	D20	2.5-V CMOS	Memory bank address bus
140	HSMB_BA3	M19	2.5-V CMOS	Memory bank address bus
68	HSMB_DQS_N0	M21	2.5-V CMOS	Memory data strobe
92	HSMB_DQS_N1	N23	2.5-V CMOS	Memory data strobe
122	HSMB_DQS_N2	K23	2.5-V CMOS	Memory data strobe
146	HSMB_DQS_N3	N24	2.5-V CMOS	Memory data strobe
66	HSMB_DQS_P0	N22	2.5-V CMOS	Memory data strobe
90	HSMB_DQS_P1	M23	2.5-V CMOS	Memory data strobe
120	HSMB_DQS_P2	L23	2.5-V CMOS	Memory data strobe
144	HSMB_DQS_P3	M24	2.5-V CMOS	Memory data strobe
150	HSMB_CKE	C22	2.5-V CMOS	Memory clock enable
152	HSMB_CSN	M25	2.5-V CMOS	Chip select
160	HSMB_PRSNTN	M20	2.5-V CMOS	HSMC port B presence detect

SDI Channel (Optional)

The development board is fully populated with the serial digital interface (SDI) channel. However, this interface shares a transceiver channel with the HSMC port A (transceiver channel 3) through a resistor-stuffing option. By default, the resistors are populated such that the HSMC port A transceiver is enabled.

☞ If you enable the SDI interface, the HSMC port A transceiver channel 3 will be disabled.

To enable the SDI interface, you must switch the placement of the following resistors listed in Table 2–23.

Table 2–23. Resistor Switching to Enable the SDI Channel

Resistor Old Placement	Resistor New Placement
R41	R45
R42	R46
R47	R50
R48	R51

The SDI video port consists of a LMH0303 cable driver (output) and a LMH0384 cable equalizer (input). The PHY devices from National Semiconductor interface to single-ended 75-Ω SMB connectors.

SDI Video Output

The cable driver supports operation at 270 Mb standard definition (SD), 1.5 Gb high definition (HD), and 2.97 Gb dual-link HD modes. Control signals are allowed for SD and HD modes selections, as well as device enable. The reference clock of the device is 148.5 MHz and matches the incoming signals to within 50 ppm using the UP and DN voltage control lines to the voltage-controlled crystal oscillator (VCXO).

Table 2–24 lists the supported output standards for the SD and HD input.

Table 2–24. Supported Output Standards for SD and HD Input

SD_HD Input	Supported Output Standards	Rise TIme
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

For more information about the application circuit of the cable driver, refer to the cable driver data sheet in www.national.com.

Table 2–25 summarizes the SDI video output interface pin assignments, signal names, and functions.

Table 2–25. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U50)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
1	SDI_A_TX_P	P4	1.5-V PCML	Serial data output P
2	SDI_A_TX_N	P3	1.5-V PCML	Serial data output N
4	SDI_A_TX_RSET	—	2.5-V	Output swing set resistor
6	SDI_A_TX_EN (1)	AM6	2.5-V	Output driver enable
10	SDI_A_TX_SD_HDN	AN5	2.5-V	High-definition select
11	SDI_A_TXDRV_N	—	2.5-V	Serial data
12	SDI_A_TXDRV_P	—	2.5-V	Serial data

Note to Table 2–6:

(1) The SDI_A_TX_EN pin has an internal pull up resistor to keep the output turned on by default.

SDI Video Input

The cable equalizer supports operation at 270 Mb SD, 1.5 Gb HD, and 2.97 Gb dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 2–26 lists the cable equalizer lengths.

Table 2–26. SDI Cable Equalizer Lengths

Data Rate (Mbps)	Cable Type	Maximum Cable Length (m)
270	Belden 1694A	400
1485		140
2970		120

Figure 2–9 shows the SDI cable equalizer, which is an excerpt from the LMH0384 cable equalizer data sheet. On this development board, the output is a single-ended output, with the negative channel driving a load local to the board.

Figure 2–9. SDI Cable Equalizer

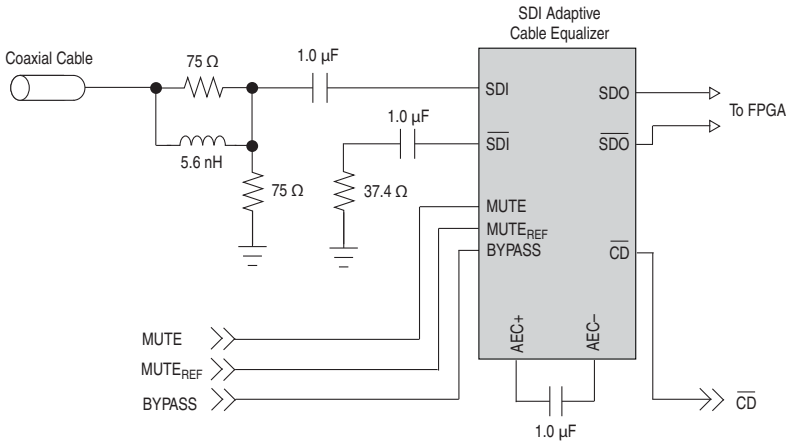


Table 2–27 summarizes the SDI video input interface pin assignments, signal names, and functions.

Table 2–27. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U47)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
2	SDI_A_IN_P1	—	2.5-V	Serial data
3	SDI_A_EQIN_N1	—	2.5-V	Serial data
7	SDI_A_RX_BYPASS	AM9	2.5-V	Equalizer bypass enable
10	SDI_A_RX_N	R1	1.5-V PCML	Serial data input N
11	SDI_A_RX_P	R2	1.5-V PCML	Serial data input P
14	SDI_A_RX_EN	AN4	2.5-V	Device enable

Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone V GT. The development board has the following memory interfaces:

- DDR3 SDRAM
- Synchronous flash

For more information about the memory interfaces, refer to the following documents:

- *Timing Analysis* section in the External Memory Interface Handbook.
- *DDR, DDR2, and DDR3 SDRAM Design Tutorials* section in the External Memory Interface Handbook.

DDR3 SDRAM

The development board supports seven 16Mx16x8 DDR3 SDRAM interfaces for very high-speed sequential memory access. The DDR3 SDRAM has two independent interfaces:

- DDR3A—40-bit data interface using a hard memory controller. This data bus consists of three ×16 devices and one of which only uses the first 8-bits of the ×8 device for ECC support.
- DDR3B—64-bit interface using a soft memory controller. This data bus consists of four ×16 devices.

DDR3A

The DDR3A SDRAM comprises of three ×16 devices with a single address and command bus. This interface connects to the vertical I/O banks on the bottom edge of the FPGA and utilizes the hard memory controller.

This memory interface runs at a target frequency of 400 MHz for a maximum theoretical bandwidth of over 32 Gbps.

Table 2–28 lists the DDR3A pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GT in terms of I/O setting and direction.

Table 2–28. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
DDR3 x16 (U26)				
N3	DDR3A_A0	AK18	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	AL18	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	AM18	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	AN18	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	AH17	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	AJ17	1.5-V SSTL Class I	Address bus

Table 2–28. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
R8	DDR3A_A6	AK17	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	AL17	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	AH16	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	AJ16	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	AL16	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	AM16	1.5-V SSTL Class I	Address bus
N7	DDR3A_A12	AM13	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	AN13	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	AN16	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AN17	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AP17	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AP15	1.5-V SSTL Class I	Row address select
K9	DDR3A_CKE	AP26	1.5-V SSTL Class I	Column address select
J7	DDR3A_CLK_P	AA18	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AA17	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	AA16	1.5-V SSTL Class I	Chip select
E7	DDR3A_DM0	AL21	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM1	AM24	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ0	AN19	1.5-V SSTL Class I	Data bus byte lane 0
F7	DDR3A_DQ1	AM19	1.5-V SSTL Class I	Data bus byte lane 0
F2	DDR3A_DQ2	AP20	1.5-V SSTL Class I	Data bus byte lane 0
F8	DDR3A_DQ3	AP21	1.5-V SSTL Class I	Data bus byte lane 0
H3	DDR3A_DQ4	AH19	1.5-V SSTL Class I	Data bus byte lane 0
H8	DDR3A_DQ5	AG19	1.5-V SSTL Class I	Data bus byte lane 0
G2	DDR3A_DQ6	AJ19	1.5-V SSTL Class I	Data bus byte lane 0
H7	DDR3A_DQ7	AM21	1.5-V SSTL Class I	Data bus byte lane 0
D7	DDR3A_DQ8	AM20	1.5-V SSTL Class I	Data bus byte lane 1
C3	DDR3A_DQ9	AL20	1.5-V SSTL Class I	Data bus byte lane 1
C8	DDR3A_DQ10	AN22	1.5-V SSTL Class I	Data bus byte lane 1
C2	DDR3A_DQ11	AN23	1.5-V SSTL Class I	Data bus byte lane 1
A7	DDR3A_DQ12	AP24	1.5-V SSTL Class I	Data bus byte lane 1
A2	DDR3A_DQ13	AP25	1.5-V SSTL Class I	Data bus byte lane 1
B8	DDR3A_DQ14	AN26	1.5-V SSTL Class I	Data bus byte lane 1
A3	DDR3A_DQ15	AN24	1.5-V SSTL Class I	Data bus byte lane 1
F3	DDR3A_DQS_P0	AB19	Differential 1.5-V SSTL Class I	Data strobe P byte lane 0
G3	DDR3A_DQS_N0	AC19	Differential 1.5-V SSTL Class I	Data strobe N byte lane 0

Table 2–28. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
C7	DDR3A_DQS_P1	AD19	Differential 1.5-V SSTL Class I	Data strobe P byte lane 1
B7	DDR3A_DQS_N1	AE19	Differential 1.5-V SSTL Class I	Data strobe N byte lane 1
K1	DDR3A_ODT	AN21	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AP14	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	AJ22	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	AN12	1.5-V SSTL Class I	Write enable
L8	DDR3A_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U27)				
N3	DDR3A_A0	AK18	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	AL18	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	AM18	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	AN18	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	AH17	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	AJ17	1.5-V SSTL Class I	Address bus
R8	DDR3A_A6	AK17	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	AL17	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	AH16	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	AJ16	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	AL16	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	AM16	1.5-V SSTL Class I	Address bus
N7	DDR3A_A12	AM13	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	AN13	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	AN16	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AN17	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AP17	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AP15	1.5-V SSTL Class I	Row address select
K9	DDR3A_CKE	AP26	1.5-V SSTL Class I	Column address select
J7	DDR3A_CLK_P	AA18	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AA17	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	AA16	1.5-V SSTL Class I	Chip select
E7	DDR3A_DM2	AM28	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3A_DM3	AL27	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ16	AP27	1.5-V SSTL Class I	Data bus byte lane 2
F7	DDR3A_DQ17	AN27	1.5-V SSTL Class I	Data bus byte lane 2
F2	DDR3A_DQ18	AK22	1.5-V SSTL Class I	Data bus byte lane 2

Table 2–28. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
F8	DDR3A_DQ19	AJ21	1.5-V SSTL Class I	Data bus byte lane 2
H3	DDR3A_DQ20	AH21	1.5-V SSTL Class I	Data bus byte lane 2
H8	DDR3A_DQ21	AH22	1.5-V SSTL Class I	Data bus byte lane 2
G2	DDR3A_DQ22	AP30	1.5-V SSTL Class I	Data bus byte lane 2
H7	DDR3A_DQ23	AN28	1.5-V SSTL Class I	Data bus byte lane 2
D7	DDR3A_DQ24	AL23	1.5-V SSTL Class I	Data bus byte lane 3
C3	DDR3A_DQ25	AK23	1.5-V SSTL Class I	Data bus byte lane 3
C8	DDR3A_DQ26	AL25	1.5-V SSTL Class I	Data bus byte lane 3
C2	DDR3A_DQ27	AM26	1.5-V SSTL Class I	Data bus byte lane 3
A7	DDR3A_DQ28	AK24	1.5-V SSTL Class I	Data bus byte lane 3
A2	DDR3A_DQ29	AJ24	1.5-V SSTL Class I	Data bus byte lane 3
B8	DDR3A_DQ30	AN31	1.5-V SSTL Class I	Data bus byte lane 3
A3	DDR3A_DQ31	AL28	1.5-V SSTL Class I	Data bus byte lane 3
F3	DDR3A_DQS_P2	AJ20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 2
G3	DDR3A_DQS_N2	AK20	Differential 1.5-V SSTL Class I	Data strobe N byte lane 2
C7	DDR3A_DQS_P3	Y20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 3
B7	DDR3A_DQS_N3	AA20	Differential 1.5-V SSTL Class I	Data strobe N byte lane 3
K1	DDR3A_ODT	AN21	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AP14	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	AJ22	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	AN12	1.5-V SSTL Class I	Write enable
L8	DDR3A_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U28)				
N3	DDR3A_A0	AK18	1.5-V SSTL Class I	Address bus
P7	DDR3A_A1	AL18	1.5-V SSTL Class I	Address bus
P3	DDR3A_A2	AM18	1.5-V SSTL Class I	Address bus
N2	DDR3A_A3	AN18	1.5-V SSTL Class I	Address bus
P8	DDR3A_A4	AH17	1.5-V SSTL Class I	Address bus
P2	DDR3A_A5	AJ17	1.5-V SSTL Class I	Address bus
R8	DDR3A_A6	AK17	1.5-V SSTL Class I	Address bus
R2	DDR3A_A7	AL17	1.5-V SSTL Class I	Address bus
T8	DDR3A_A8	AH16	1.5-V SSTL Class I	Address bus
R3	DDR3A_A9	AJ16	1.5-V SSTL Class I	Address bus
L7	DDR3A_A10	AL16	1.5-V SSTL Class I	Address bus
R7	DDR3A_A11	AM16	1.5-V SSTL Class I	Address bus

Table 2–28. DDR3A Device Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
N7	DDR3A_A12	AM13	1.5-V SSTL Class I	Address bus
T3	DDR3A_A13	AN13	1.5-V SSTL Class I	Address bus
M2	DDR3A_BA0	AN16	1.5-V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AN17	1.5-V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AP17	1.5-V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AP15	1.5-V SSTL Class I	Row address select
K9	DDR3A_CKE	AP26	1.5-V SSTL Class I	Column address select
J7	DDR3A_CLK_P	AA18	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AA17	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3A_CSN	AA16	1.5-V SSTL Class I	Chip select
E7	DDR3A_DM4	AL30	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3A_DQ32	AH23	1.5-V SSTL Class I	Data bus byte lane 4
F7	DDR3A_DQ33	AG23	1.5-V SSTL Class I	Data bus byte lane 4
F2	DDR3A_DQ34	AN32	1.5-V SSTL Class I	Data bus byte lane 4
F8	DDR3A_DQ35	AN29	1.5-V SSTL Class I	Data bus byte lane 4
H3	DDR3A_DQ36	AK25	1.5-V SSTL Class I	Data bus byte lane 4
H8	DDR3A_DQ37	AJ25	1.5-V SSTL Class I	Data bus byte lane 4
G2	DDR3A_DQ38	AK28	1.5-V SSTL Class I	Data bus byte lane 4
H7	DDR3A_DQ39	AM30	1.5-V SSTL Class I	Data bus byte lane 4
F3	DDR3A_DQS_P4	AC21	Differential 1.5-V SSTL Class I	Data strobe P byte lane 4
G3	DDR3A_DQS_N4	AD21	Differential 1.5-V SSTL Class I	Data strobe N byte lane 4
K1	DDR3A_ODT	AN21	1.5-V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AP14	1.5-V SSTL Class I	Row address select
T2	DDR3A_RESETN	AJ22	1.5-V SSTL Class I	Reset
L3	DDR3A_WEN	AN12	1.5-V SSTL Class I	Write enable
L8	DDR3A_ZQ03	—	1.5-V SSTL Class I	ZQ impedance calibration

DDR3B

The DDR3B SDRAM comprises of four ×16 devices with a single address and command bus. This interface connects to the horizontal I/O banks on the right edge of the FPGA and utilizes the soft memory controller.

This memory interface runs at a target frequency of 300 MHz for a maximum theoretical bandwidth of over 38.40 Gbps.

Table 2–28 lists the DDR3B pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GT in terms of I/O setting and direction.

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
DDR3 x16 (U30)				
N3	DDR3B_A0	H29	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	K28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	K34	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	L32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	R32	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	R33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	N32	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	G33	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	AE34	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	L27	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	V33	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	U33	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	T31	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	T30	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	J31	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N29	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	P27	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	N27	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	AF32	1.5-V SSTL Class I	Column address select
J7	DDR3B_CLK_P	R30	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	R29	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	V27	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM0	AE30	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM1	AE32	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ0	AF31	1.5-V SSTL Class I	Data bus byte lane 0
F7	DDR3B_DQ1	AD30	1.5-V SSTL Class I	Data bus byte lane 0
F2	DDR3B_DQ2	AJ32	1.5-V SSTL Class I	Data bus byte lane 0

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
F8	DDR3B_DQ3	AC31	1.5-V SSTL Class I	Data bus byte lane 0
H3	DDR3B_DQ4	AH32	1.5-V SSTL Class I	Data bus byte lane 0
H8	DDR3B_DQ5	Y28	1.5-V SSTL Class I	Data bus byte lane 0
G2	DDR3B_DQ6	AN34	1.5-V SSTL Class I	Data bus byte lane 0
H7	DDR3B_DQ7	Y27	1.5-V SSTL Class I	Data bus byte lane 0
D7	DDR3B_DQ8	AD32	1.5-V SSTL Class I	Data bus byte lane 1
C3	DDR3B_DQ9	AH33	1.5-V SSTL Class I	Data bus byte lane 1
C8	DDR3B_DQ10	AB31	1.5-V SSTL Class I	Data bus byte lane 1
C2	DDR3B_DQ11	AJ34	1.5-V SSTL Class I	Data bus byte lane 1
A7	DDR3B_DQ12	AA31	1.5-V SSTL Class I	Data bus byte lane 1
A2	DDR3B_DQ13	AK34	1.5-V SSTL Class I	Data bus byte lane 1
B8	DDR3B_DQ14	W31	1.5-V SSTL Class I	Data bus byte lane 1
A3	DDR3B_DQ15	AG33	1.5-V SSTL Class I	Data bus byte lane 1
F3	DDR3B_DQS_P0	Y29	Differential 1.5-V SSTL Class I	Data strobe P byte lane 0
G3	DDR3B_DQS_N0	Y30	Differential 1.5-V SSTL Class I	Data strobe N byte lane 0
C7	DDR3B_DQS_P1	W29	Differential 1.5-V SSTL Class I	Data strobe P byte lane 1
B7	DDR3B_DQS_N1	W30	Differential 1.5-V SSTL Class I	Data strobe N byte lane 1
K1	DDR3B_ODT	AA32	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	Y32	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	AG31	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	AM34	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U22)				
N3	DDR3B_A0	H29	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	K28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	K34	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	L32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	R32	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	R33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	N32	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	G33	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	AE34	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	L27	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	V33	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	U33	1.5-V SSTL Class I	Address bus

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
N7	DDR3B_A12	T31	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	T30	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	J31	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N29	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	P27	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	N27	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	AF32	1.5-V SSTL Class I	Column address select
J7	DDR3B_CLK_P	R30	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	R29	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	V27	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM2	AC34	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM3	W34	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ16	AD34	1.5-V SSTL Class I	Data bus byte lane 2
F7	DDR3B_DQ17	AC33	1.5-V SSTL Class I	Data bus byte lane 2
F2	DDR3B_DQ18	AG34	1.5-V SSTL Class I	Data bus byte lane 2
F8	DDR3B_DQ19	AB33	1.5-V SSTL Class I	Data bus byte lane 2
H3	DDR3B_DQ20	AE33	1.5-V SSTL Class I	Data bus byte lane 2
H8	DDR3B_DQ21	V32	1.5-V SSTL Class I	Data bus byte lane 2
G2	DDR3B_DQ22	AH34	1.5-V SSTL Class I	Data bus byte lane 2
H7	DDR3B_DQ23	W32	1.5-V SSTL Class I	Data bus byte lane 2
D7	DDR3B_DQ24	U29	1.5-V SSTL Class I	Data bus byte lane 3
C3	DDR3B_DQ25	V34	1.5-V SSTL Class I	Data bus byte lane 3
C8	DDR3B_DQ26	U34	1.5-V SSTL Class I	Data bus byte lane 3
C2	DDR3B_DQ27	AA33	1.5-V SSTL Class I	Data bus byte lane 3
A7	DDR3B_DQ28	R34	1.5-V SSTL Class I	Data bus byte lane 3
A2	DDR3B_DQ29	Y33	1.5-V SSTL Class I	Data bus byte lane 3
B8	DDR3B_DQ30	P34	1.5-V SSTL Class I	Data bus byte lane 3
A3	DDR3B_DQ31	U28	1.5-V SSTL Class I	Data bus byte lane 3
F3	DDR3B_DQS_P2	V24	Differential 1.5-V SSTL Class I	Data strobe P byte lane 2
G3	DDR3B_DQS_N2	V23	Differential 1.5-V SSTL Class I	Data strobe N byte lane 2
C7	DDR3B_DQS_P3	U24	Differential 1.5-V SSTL Class I	Data strobe P byte lane 3
B7	DDR3B_DQS_N3	U25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 3
K1	DDR3B_ODT	AA32	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	Y32	1.5-V SSTL Class I	Row address select

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
T2	DDR3B_RESETN	AG31	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	AM34	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U8)				
N3	DDR3B_A0	H29	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	K28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	K34	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	L32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	R32	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	R33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	N32	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	G33	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	AE34	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	L27	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	V33	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	U33	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	T31	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	T30	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	J31	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N29	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	P27	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	N27	1.5-V SSTL Class I	Row address select
K9	DDR3B_CKE	AF32	1.5-V SSTL Class I	Column address select
J7	DDR3B_CLK_P	R30	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	R29	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	V27	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM4	M33	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM5	K32	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ32	T32	1.5-V SSTL Class I	Data bus byte lane 4
F7	DDR3B_DQ33	N33	1.5-V SSTL Class I	Data bus byte lane 4
F2	DDR3B_DQ34	T33	1.5-V SSTL Class I	Data bus byte lane 4
F8	DDR3B_DQ35	L33	1.5-V SSTL Class I	Data bus byte lane 4
H3	DDR3B_DQ36	T28	1.5-V SSTL Class I	Data bus byte lane 4
H8	DDR3B_DQ37	J34	1.5-V SSTL Class I	Data bus byte lane 4
G2	DDR3B_DQ38	T27	1.5-V SSTL Class I	Data bus byte lane 4
H7	DDR3B_DQ39	M34	1.5-V SSTL Class I	Data bus byte lane 4
D7	DDR3B_DQ40	K33	1.5-V SSTL Class I	Data bus byte lane 5

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
C3	DDR3B_DQ41	N31	1.5-V SSTL Class I	Data bus byte lane 5
C8	DDR3B_DQ42	G34	1.5-V SSTL Class I	Data bus byte lane 5
C2	DDR3B_DQ43	R28	1.5-V SSTL Class I	Data bus byte lane 5
A7	DDR3B_DQ44	H33	1.5-V SSTL Class I	Data bus byte lane 5
A2	DDR3B_DQ45	P32	1.5-V SSTL Class I	Data bus byte lane 5
B8	DDR3B_DQ46	H34	1.5-V SSTL Class I	Data bus byte lane 5
A3	DDR3B_DQ47	R27	1.5-V SSTL Class I	Data bus byte lane 5
F3	DDR3B_DQS_P4	U23	Differential 1.5-V SSTL Class I	Data strobe P byte lane 4
G3	DDR3B_DQS_N4	T23	Differential 1.5-V SSTL Class I	Data strobe N byte lane 4
C7	DDR3B_DQS_P5	T25	Differential 1.5-V SSTL Class I	Data strobe P byte lane 5
B7	DDR3B_DQS_N5	R25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 5
K1	DDR3B_ODT	AA32	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	Y32	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	AG31	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	AM34	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ03	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U15)				
N3	DDR3B_A0	H29	1.5-V SSTL Class I	Address bus
P7	DDR3B_A1	K28	1.5-V SSTL Class I	Address bus
P3	DDR3B_A2	K34	1.5-V SSTL Class I	Address bus
N2	DDR3B_A3	L32	1.5-V SSTL Class I	Address bus
P8	DDR3B_A4	R32	1.5-V SSTL Class I	Address bus
P2	DDR3B_A5	R33	1.5-V SSTL Class I	Address bus
R8	DDR3B_A6	N32	1.5-V SSTL Class I	Address bus
R2	DDR3B_A7	G33	1.5-V SSTL Class I	Address bus
T8	DDR3B_A8	AE34	1.5-V SSTL Class I	Address bus
R3	DDR3B_A9	L27	1.5-V SSTL Class I	Address bus
L7	DDR3B_A10	V33	1.5-V SSTL Class I	Address bus
R7	DDR3B_A11	U33	1.5-V SSTL Class I	Address bus
N7	DDR3B_A12	T31	1.5-V SSTL Class I	Address bus
T3	DDR3B_A13	T30	1.5-V SSTL Class I	Address bus
M2	DDR3B_BA0	J31	1.5-V SSTL Class I	Bank address bus
N8	DDR3B_BA1	N29	1.5-V SSTL Class I	Bank address bus
M3	DDR3B_BA2	P27	1.5-V SSTL Class I	Bank address bus
K3	DDR3B_CASN	N27	1.5-V SSTL Class I	Row address select

Table 2–29. DDR3B Device Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 6)

Board Reference	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
K9	DDR3B_CKE	AF32	1.5-V SSTL Class I	Column address select
J7	DDR3B_CLK_P	R30	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	R29	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3B_CSN	V27	1.5-V SSTL Class I	Chip select
E7	DDR3B_DM6	L31	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3B_DM7	H28	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3B_DQ48	N28	1.5-V SSTL Class I	Data bus byte lane 6
F7	DDR3B_DQ49	L30	1.5-V SSTL Class I	Data bus byte lane 6
F2	DDR3B_DQ50	P30	1.5-V SSTL Class I	Data bus byte lane 6
F8	DDR3B_DQ51	K30	1.5-V SSTL Class I	Data bus byte lane 6
H3	DDR3B_DQ52	J32	1.5-V SSTL Class I	Data bus byte lane 6
H8	DDR3B_DQ53	H32	1.5-V SSTL Class I	Data bus byte lane 6
G2	DDR3B_DQ54	M31	1.5-V SSTL Class I	Data bus byte lane 6
H7	DDR3B_DQ55	H31	1.5-V SSTL Class I	Data bus byte lane 6
D7	DDR3B_DQ56	G30	1.5-V SSTL Class I	Data bus byte lane 7
C3	DDR3B_DQ57	K29	1.5-V SSTL Class I	Data bus byte lane 7
C8	DDR3B_DQ58	G31	1.5-V SSTL Class I	Data bus byte lane 7
C2	DDR3B_DQ59	M30	1.5-V SSTL Class I	Data bus byte lane 7
A7	DDR3B_DQ60	J30	1.5-V SSTL Class I	Data bus byte lane 7
A2	DDR3B_DQ61	M29	1.5-V SSTL Class I	Data bus byte lane 7
B8	DDR3B_DQ62	J29	1.5-V SSTL Class I	Data bus byte lane 7
A3	DDR3B_DQ63	L28	1.5-V SSTL Class I	Data bus byte lane 7
F3	DDR3B_DQS_P6	R23	Differential 1.5-V SSTL Class I	Data strobe P byte lane 6
G3	DDR3B_DQS_N6	R24	Differential 1.5-V SSTL Class I	Data strobe N byte lane 6
C7	DDR3B_DQS_P7	P24	Differential 1.5-V SSTL Class I	Data strobe P byte lane 7
B7	DDR3B_DQS_N7	P25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 7
K1	DDR3B_ODT	AA32	1.5-V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	Y32	1.5-V SSTL Class I	Row address select
T2	DDR3B_RESETN	AG31	1.5-V SSTL Class I	Reset
L3	DDR3B_WEN	AM34	1.5-V SSTL Class I	Write enable
L8	DDR3B_ZQ03	—	1.5-V SSTL Class I	ZQ impedance calibration

Flash

The development board supports a 1-GB CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, test application data, and user code space. This device is part of the shared FM bus that connects the flash memory and MAX V CPLD 5M2210 System Controller.

This 16-bit data interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word buffer while the erase time is 800 ms for a 128 K array block.

Table 2–30 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V GT in terms of I/O setting and direction.

Table 2–30. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U20)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
F6	FLASH_ADVN	AB34	2.5-V	Address valid
B4	FLASH_CEN	AA21	2.5-V	Chip enable
E6	FLASH_CLK	AE29	2.5-V	Clock
F8	FLASH_OEN	AG16	2.5-V	Output enable
F7	FLASH_RDYBSYN	AD20	2.5-V	Ready
D4	FLASH_RESETN	AB16	2.5-V	Reset
G8	FLASH_WEN	AM14	2.5-V	Write enable
C6	FLASH_WPN	—	2.5-V	Write protect
A1	FSM_A1	AK33	2.5-V	Address bus
B1	FSM_A2	AC27	2.5-V	Address bus
C1	FSM_A3	AB24	2.5-V	Address bus
D1	FSM_A4	AB23	2.5-V	Address bus
D2	FSM_A5	AC28	2.5-V	Address bus
A2	FSM_A6	Y24	2.5-V	Address bus
C2	FSM_A7	Y25	2.5-V	Address bus
A3	FSM_A8	AF27	2.5-V	Address bus
B3	FSM_A9	AF26	2.5-V	Address bus
C3	FSM_A10	AB28	2.5-V	Address bus
D3	FSM_A11	AE28	2.5-V	Address bus
C4	FSM_A12	AB29	2.5-V	Address bus
A5	FSM_A13	AF28	2.5-V	Address bus
B5	FSM_A14	AH28	2.5-V	Address bus
C5	FSM_A15	AB30	2.5-V	Address bus
D7	FSM_A16	AG29	2.5-V	Address bus
D8	FSM_A17	AA30	2.5-V	Address bus
A7	FSM_A18	AK30	2.5-V	Address bus
B7	FSM_A19	AJ30	2.5-V	Address bus
C7	FSM_A20	AG30	2.5-V	Address bus

Table 2–30. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U20)	Schematic Signal Name	Cyclone V GT Pin Number	I/O Standard	Description
C8	FSM_A21	AN33	2.5-V	Address bus
A8	FSM_A22	AF30	2.5-V	Address bus
G1	FSM_A23	AM33	2.5-V	Address bus
H8	FSM_A24	AK32	2.5-V	Address bus
B6	FSM_A25	AH31	2.5-V	Address bus
B8	FSM_A26	AD24	2.5-V	Address bus
F2	FSM_D0	AJ31	2.5-V	Data bus
E2	FSM_D1	AA23	2.5-V	Data bus
G3	FSM_D2	Y23	2.5-V	Data bus
E4	FSM_D3	Y22	2.5-V	Data bus
E5	FSM_D4	W24	2.5-V	Data bus
G5	FSM_D5	AC29	2.5-V	Data bus
G6	FSM_D6	AB25	2.5-V	Data bus
H7	FSM_D7	AA25	2.5-V	Data bus
E1	FSM_D8	AG28	2.5-V	Data bus
E3	FSM_D9	AH29	2.5-V	Data bus
F3	FSM_D10	AA27	2.5-V	Data bus
F4	FSM_D11	AA28	2.5-V	Data bus
F5	FSM_D12	AL32	2.5-V	Data bus
H5	FSM_D13	AC24	2.5-V	Data bus
G7	FSM_D14	AC23	2.5-V	Data bus
E7	FSM_D15	AL33	2.5-V	Data bus

Power Supply

You can power up the development board either from a laptop-style DC power input or from the PCI Express edge connector. The laptop supply must be a 19-V/6.32-A rated supply. The DC voltage is then stepped down to various power rails used by the board components. Table 2–31 outlines the allowable power inputs.

Table 2–31. Power Inputs

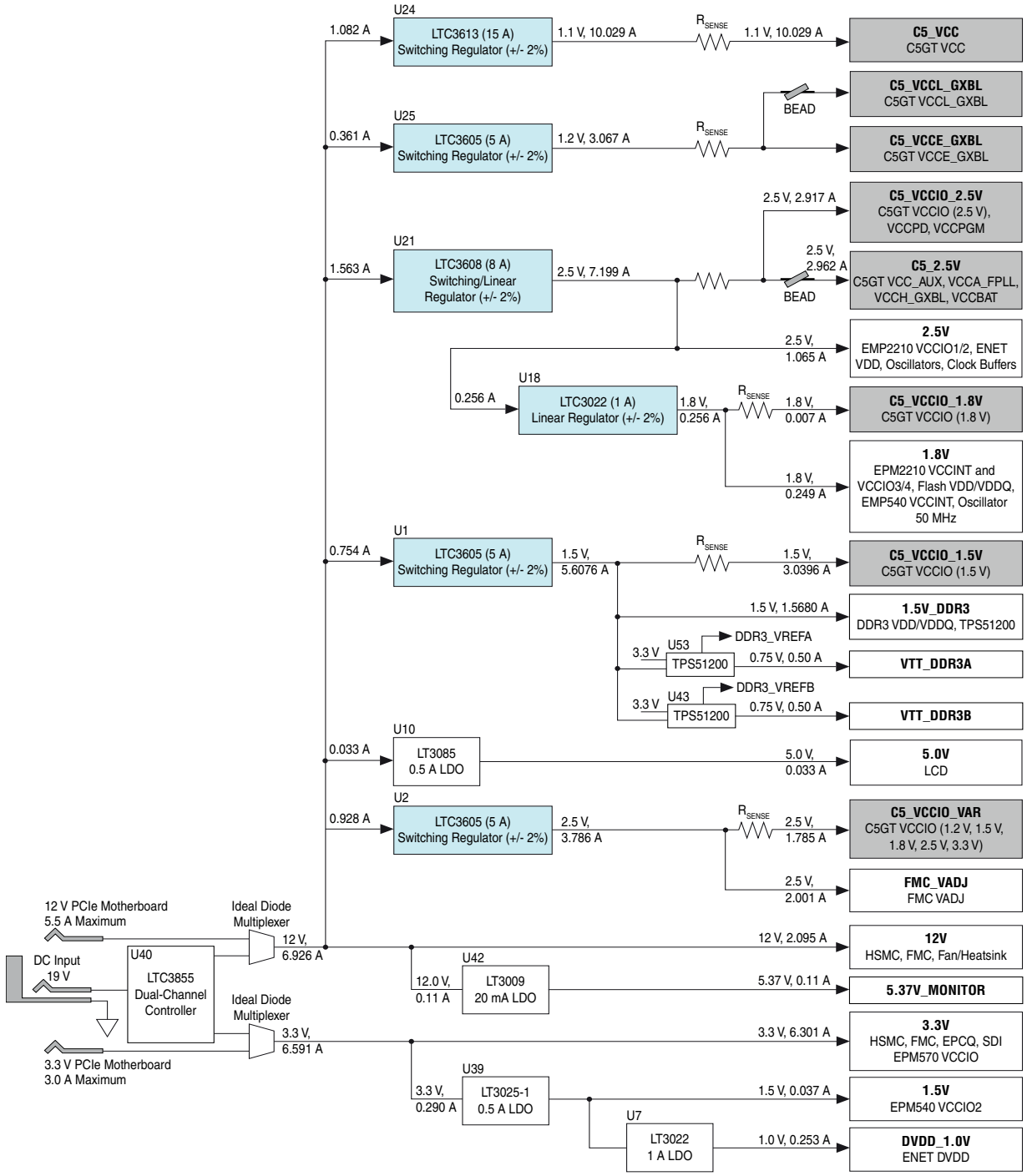
Power Source	Voltage (V)	Current (A)	Maximum Power (W)
Laptop-style DC input	19.0	6.32	120
25-W PCI Express edge connector	3.3	3.0	9
	12.0	2.1	16
75-W PCI Express edge connector	3.3	3.0	9
	12.0	5.5	66

An on-board multi-channel analog-to-digital converter (ADC) measures the current for several specific board rails.

Power Distribution System

Figure 2–10 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–10. Power Distribution System



Power Measurement

There are six power supply rails that have on-board current sense capabilities using 24-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure current. A SPI bus connects these ADC devices to the MAX V CPLD 5M2210 System Controller.

Figure 2–11 shows the block diagram for the power measurement circuitry.

Figure 2–11. Power Measurement Circuit

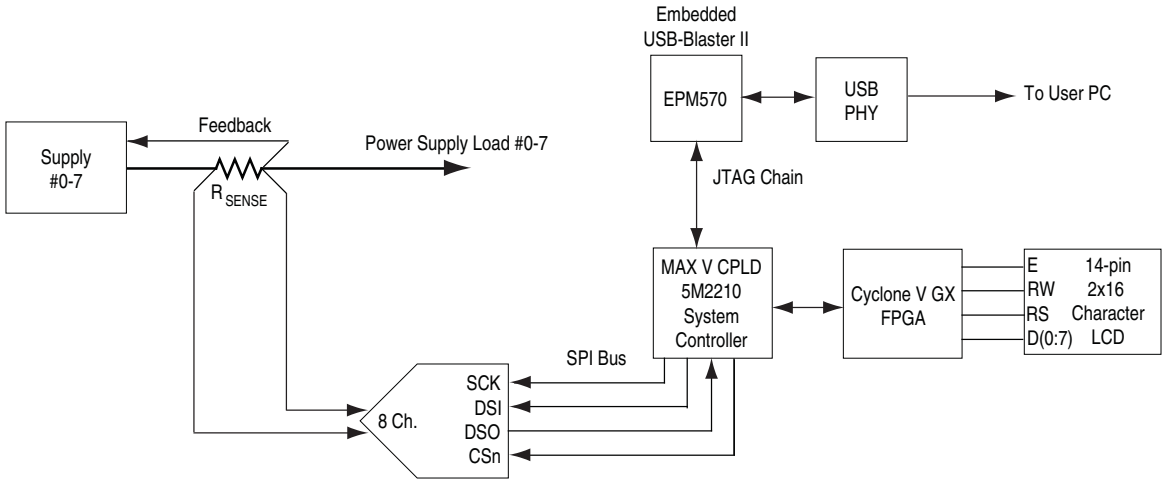


Table 2–32 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured while the device pin column specifies the devices attached to the rail.

Table 2–32. Power Measurement Rails

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	C5_VCC	1.1	VCC	FPGA core and periphery power
2	C5_VCCL_GXBL	1.2	VCCE_GXB	XCVR analog receive
	C5_VCCE_GXBL	1.2	VCCL_GXB	XCVR analog clock network
3	C5_VCCIO_2.5V C5_2.5V	2.5	VCCA_FPLL	PLL analog power
		2.5	VCC_AUX	Auxiliary
		2.5	VCCPD	I/O pre-drivers
		2.5	VCCPGM	Configuration I/O
		2.5	VCCH_GXBL	XCVR block level transmit buffers
		2.5	VCCIO_3A, VCCIO_8A	VCC I/O banks 3 and 8
4	A5A_VCCIO_1.8V	1.8	VCCIO_5A	VCCIO bank 5 (flash)
5	A5A_VCCIO_1.5V	1.5	VCCIO_3B, VCCIO_4A, VCCIO_5B, VCCIO_6A	VCCIO bank (DDR3)
6	A5A_VCCIO_VAR	2.5 (default)	VCCIO_7A	VCCIO bank (HSMB)

3. Board Components Reference

This chapter lists the component reference and manufacturing information of all the components on the Cyclone V GT FPGA development board.

Table 3–1 lists board component reference and manufacturing information.

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U13	FPGA, Cyclone V GT F1152, 150K LEs, lead free	Altera Corporation	5CGTFD9E5F35C7N	www.altera.com
U32	MAX V CPLD 5M2210 System Controller, 2210 LEs	Altera Corporation	5M2210ZF256C4N	www.altera.com
U49	MAX II CPLD, 570 LEs	Altera Corporation	EPM570T100	www.altera.com
U4	High-Speed USB peripheral controller	Cypress	CY7C68013A-56BAXC	www.cypress.com
D1–D4, D6–D18, D22–D30, D32	Green LED	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D34, D35, D44, D45	Yellow LED	Lumex Inc.	SML-LXT0805SYW-TR	www.lumex.com
D5	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D21	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com
SW3, SW4	Four-position DIP switch	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com
SW1	Eight-position DIP switch	C&K Components/ ITT Industries	TDA08H0SB1	www.ittcannon.com
S1–S7	Push button	Wurth Elektronik	434121043816	www.we-online.com
X1	25 MHz crystal oscillator, ±50 ppm, CMOS, 1.8 V	Epson	SG-310SDF 25.0000M-B3	www.eea.epson.com
X2	100 MHz clock oscillator, ±50 ppm, CMOS, 2.5 V	ECS, Inc	ECS-3525-1000-B-TR	www.ecsxtal.com
X3	148.50 MHz LVDS voltage controlled crystal oscillator, ±50 ppm, LVDS, 2.5 V	Silicon Labs	571FDB000159DG	www.silabs.com
X4	10-810 MHz programmable oscillator, ±50 ppm, 2.5 V	Silicon Labs	570FAB000433DG	www.silabs.com
X5	125 MHz crystal oscillator, ±50 ppm, LVDS, 2.5 V	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
X6	50 MHz clock oscillator, ±50 ppm, CMOS, 1.8 V	ECS, Inc	ECS-3518-500-B-xx	www.ecsxtal.com
J10	1×10 pin LCD socket strip	Samtec	SSW-110-01-G-S	www.samtec.com
B3	2×16 character LCD, 5×8 dot matrix	Newhaven Display International, Inc.	NHD-0216K3Z-NSW-BBW-V3	www.newhavendisplay.com

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U11	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAA1C000	www.marvell.com
J9	RJ-45 connector, 10/100/1000 Mbps	Halo Electronics, Inc.	HFJ11-1G02E	www.haloelectronics.com
J1, J2	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com
U50	3-Gbps HD/SD SDI cable driver with cable detect	National Semiconductor	LMH0303SQx	www.national.com
U47	3-Gbps HD/SD SDI adaptive cable equalizer	National Semiconductor	LMH0384SQ	www.national.com
U8, U15, U22, U26, U27, U28, U30	16M×16×8, 128-MB DDR3 SDRAM	Micron	MT41K128M16JT	www.micron.com
U19, U23	16M×8×8, 128-MB DDR3 SDRAM	Micron	MT41J128M8	www.micron.com
U20	1-Gb synchronous flash	Numonyx	PC28F00AP30BF	www.numonyx.com
U45	16-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

Compliance and Conformity Statements

Statement of China-RoHS Compliance

Table 3–2 lists hazardous substances included with the kit.

Table 3–2. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone V GT development board	X*	0	0	0	0	0
19 V power supply	0	0	0	0	0	0
Type-B mini-USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 3–2:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

CE EMI Conformity Caution

This development kit is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
August 2017	1.3	Added information about programming EPCQ
September 2014	1.2	Added "CE EMI Conformity Caution" on page 3–3.
June 2014	1.1	■ Corrected Table 2–22 pin numbers for HSMC Port A Board References 103 and 104. ■ Corrected Table 2–12 I/O standard for signal PCIE_REFCLK_P.
June 2013	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.

Visual Cue	Meaning
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.