P33C_CE110: PWM Configuration- Complementary PWM

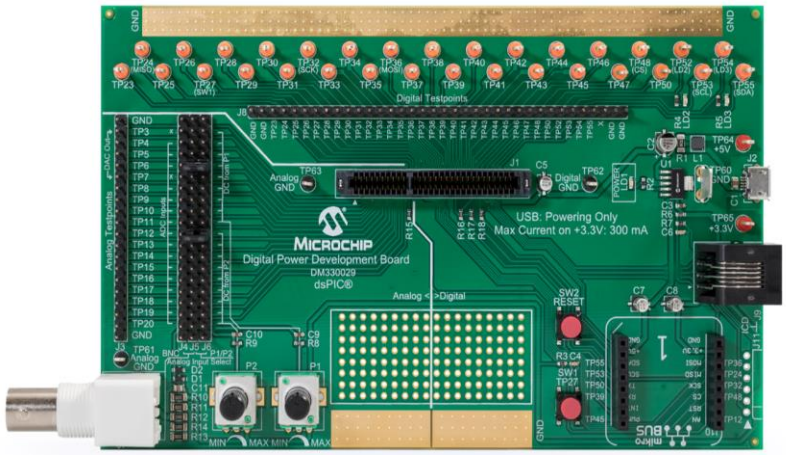
I. Introduction

This code example shows the basic configuration of the High Resolution PWM module and one PWM channel to generate a single, complementary PWM waveform for dsPIC33CK and dsPIC33CH devices.

II. Hardware

1. Digital Power Development Board (DM330029)

- https://www.microchip.com/DevelopmentTools/ProductDetails/PartNO/DM330029



2. dsPIC33CK256MP506 Digital Power Plug-In Module (MA330048)

- https://www.microchip.com/Developmenttools/ProductDetails/MA330048

3. dsPIC33CH512MP506 Digital Power Plug-in Module (MA330049)

- https://www.microchip.com/Developmenttools/ProductDetails/MA330049

III. Software Tools

1. MPLAB X IDE

- http://www.microchip.com/mplab/mplab-x-ide

2. XC16 Compilers

- http://www.microchip.com/mplab/compilers

IV. Code Example Description

1. Description

The High resolution PWM module used the PWM Generator (PG1) to generate a 400Khz, 250ps resolution, complementary PWM waveform output. The PWM waveform outputs can be monitored through TP45 (PWM1H) and TP47 (PWM1L) of DM330029 when using MA330048 and through TP35 (PWM1H) and TP38 (PWM1L) of DM330029 when using MA330049.

2. Pointers on configuring the PWM

- The APLL is used as clock input of the PWM by selecting AFPLLO for MCLKSEL bits of PCLKCON register and selecting MCLKSEL for CLKSEL bits of PG1CONL register. Note: APLL must provide a 500 MHz clock input to PWM in order to generate a High Resolution PWM

```
PCLKCONbits.MCLKSEL = 0b11;

pg->PGxCONL.bits.CLKSEL = 0b01;
```

- To allow self-triggering, Local EOC is selected for SOCS bits of PG1CONH register

```
pg->PGxCONH.bits.SOCS = 0;
```

- To operate the PWM output in complementary mode, the PMOD bits of PG1IOCONH are clear

```
pg->PGxIOCONH.bits.PMOD = 0b00;
```

- To produce a 400Khz, 50% Duty Cycle, high resolution PWM output, the value of PG1PER register is set to 10000 counts. The 10000 counts are the total number of 250ps Clock ticks in order to produce a 400Khz PWM frequency (1/400khz/250ps). The 50% Duty Cycle is achieved by setting the value of the PG1DC register to half of the PG1PER register.
  Note: the 250ps is recommended maximum PWM resolution provided by the device data sheet.

```
pg->PGxPER.value = PWM_PERIOD;  // PWM_PERIOD = (volatile
      uint16_t)((PWM_OUT_PERIOD/PWM_RESOLUTION))
      pg->PGxDC.value = (volatile uint16_t) (PWM_PERIOD*
                  PWM_DUTY_RATIO) ;
                  // PWM_DUTY_RATIO = 0.5
```

- To operate the PWM in high resolution mode, the HREN bit of PG1CONL is set. Note: when HREN = 0,PWM resolution is only 2ns so the output frequency of PG1 is only 50Khz (1/((10000)*2e-9))

```
pg->PGxCONL.bits.HREN = 1;
```

- To enable the PG1, set the ON bits of PG1CONL register.

```
pg->PGxCONL.bits.ON = 1;
```

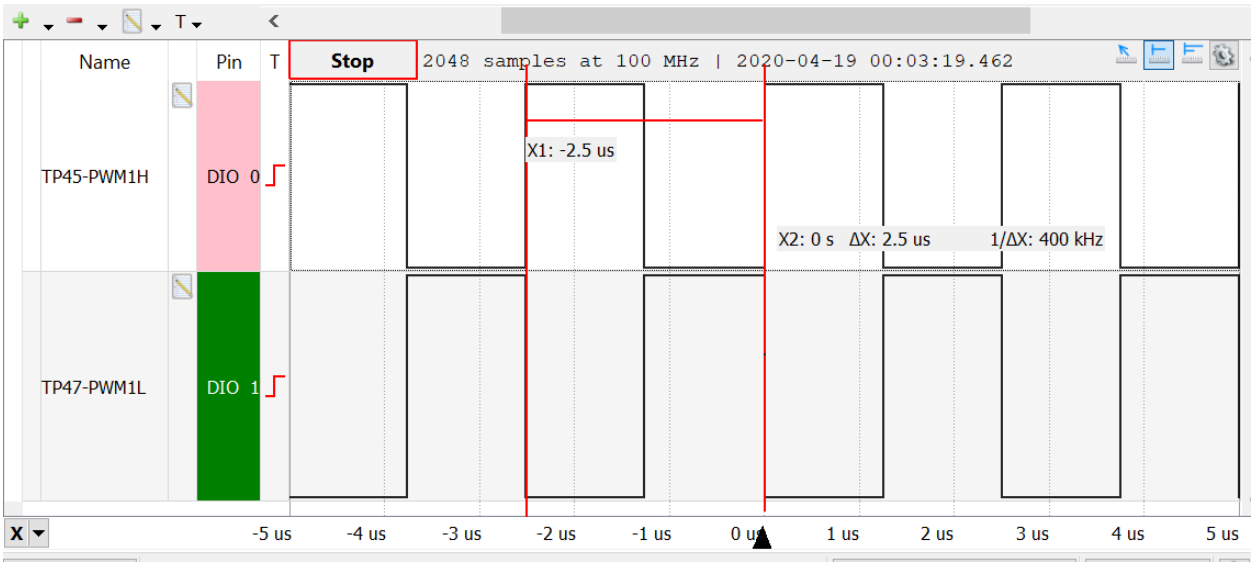
- To make available the complementary PWM outputs at PWM1H and PWM1L device pins, the PENH and PENL bits of PG1IOCONH registers are set.

```
pg->PGxIOCONH.bits.PENH = 1;
pg->PGxIOCONH.bits.PENL = 1;
```

NOTE: Refer to the device datasheet for more information. To complement the information in the data sheet, refer to "High-Resolution PWM with Fine Edge Placement" (DS70005320) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

V. Result

1. dsPIC33CK256MP506 device (TP45/TP47 – PWM1H/PWM1L)



2. dsPIC33CH512MP506 device (TP35/TP38 – PWM1H/PWM1L)