



# **DDR configuration tool for Microchip platforms**

Technical Note

CONFIDENTIAL

**TNxxxx**

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## TERMS and ABBREVIATIONS

HIF	Host Interface
ODT	On-Die Termination
PUB	PHY utility block
SoC	System on a Chip

## Requirements

The tools are developed using the `ruby` scripting language, which must be available.

The scripts may run under both `Linux` or `Windows`. The `Windows` environment may require installing the `WSL2` package to emulate `Linux`.

## Supported platforms

This tool is supported form the following target SoC platforms:

- `sparx5` (ARMv8 A53 dual-core)
- `lan966x` (ARMV7 A7 single-core)
- `lan969x` (ARMv8 A53 single-core)

## Introduction

This software package contain a set of tools that can create DDR configurations specific to a target platform and board design. A board design defines the physical DDR memory system, such that the DDR controller needs a carefully crafted configuration to ensure a stable and effective operation.

The DDR controller supported is the *Synopsis uMCTL2* DesignWare component, accompanied with a *Synopsis PHY Utility Block*.

The supported platforms all use DDR3 or DDR3 + DDR4.

## Workflow

The tool works by accepting a *configuration profile* as input, which can be transformed into a compact representation of the many configuration options the target, **specifically** generated for a given platform and board.

The output configuration may be represented in different formats, depending on the target platform.

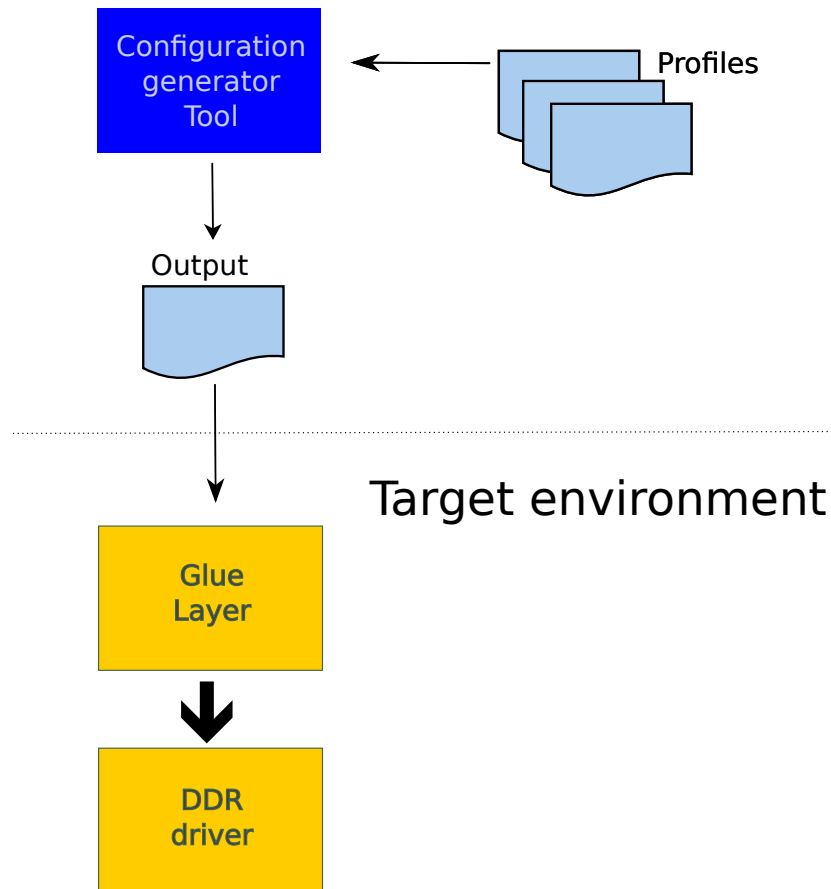
The different formats are:

<b>format</b>	<b>platform</b>	<b>comments</b>
source	lan966x	The configuration is output to "C" code, and compiled into the target firmware.
devicetree	lan969x, sparx5	The configuration is output to device-tree format, which is added to a target image (as a separate entity).
yaml	-none-	The configuration is stored in YAML format. The format can be used for documentation purposes as well as for comparing with other configurations.

The output representation is dictated by the target implementation of the actual target system DDR driver operating environment. Specifically, 'device tree' support may not be available on a given target (Example: lan966x ).

The workflow of working with the DDR configuration is illustrated below:

## Host environment



## Configuration parameters

At the top level, the following user-level parameters are available:

Keyword	Type	Description
platform	sparx5   lan966x   lan969x	The name of the target platform SoC
clock_speed	integer	The clock speed of the DDR data bus. See later.

Keyword	Type	Description
mem_size	integer	Total Memory Size (in Mbytes)
mem_type	DDR3   DDR4	The DDR memory type of the equipped DDR devices.
device_bus_width	x8   x16	Bus width of the equipped DDR devices. x8 support is experimental.
active_ranks	integer	The number of (active) ranks in the memory topology.
ecc_mode	0   4	The ECC mode to employ. ECC mode 0 implies ECC is disabled, mode 4 is "sec/ded over 1 beat"
mem_profile	string	The filename of a file defining DDR memory address generation. See later.
_2T_mode	boolean	Whether 2T timing should be used
board	string	The filename of file containing board specific tuning parameters. See later.

## Clock speed.

The *clock\_speed* affects a lot of the calculated parameters for the memory controller.

Whether or not the clock speed can be changed or not, depends on the target system (and the actual driver implementation).

The current state of the clock speed is described below.

Platform	Supported clocks	Notes
sparx5	2500   2000   1667   1250	NB: DDR4 will only work at 1667 Mhz
lan966x	1200	Fixed clock
lan969x	2400	Fixed clock

## Memory profile parameter *mem\_profile*

In order to define the way HIF addresses are used to select ranks, groups and DDR devices, a separate YAML file is used. This configuration file may be used by several configurations (board designs) using similar physical DDR topology.

The *mem\_profile* file defines the so-called "address map" registers (and sub-fields). An example is given below.

Note: The registers and sub-fields vary a little between platforms, so not all registers apply to all supported platforms. Refer to [1], section "2.11: Address Mapper".

#### *Address map definition example*

```
addrmap0:
  ADDRMAP_CS_BIT0: 31
addrmap1:
  ADDRMAP_BANK_B0: 24
  ADDRMAP_BANK_B1: 24
  ADDRMAP_BANK_B2: 24
addrmap2:
  ADDRMAP_COL_B2: 0
  ADDRMAP_COL_B3: 0
  ADDRMAP_COL_B4: 0
  ADDRMAP_COL_B5: 0
addrmap3:
  ADDRMAP_COL_B6: 0
  ADDRMAP_COL_B7: 0
  ADDRMAP_COL_B8: 0
  ADDRMAP_COL_B9: 0
addrmap4:
  ADDRMAP_COL_B10: 31
  ADDRMAP_COL_B11: 31
addrmap5:
  ADDRMAP_ROW_B0: 4
  ADDRMAP_ROW_B1: 4
  ADDRMAP_ROW_B2_10: 4
  ADDRMAP_ROW_B11: 4
addrmap6:
  ADDRMAP_ROW_B12: 4
  ADDRMAP_ROW_B13: 4
  ADDRMAP_ROW_B14: 4
  ADDRMAP_ROW_B15: 4
  LPDDR3_6GB_12GB: 0
addrmap7:
  ADDRMAP_ROW_B16: 15
  ADDRMAP_ROW_B17: 15
addrmap8:
  ADDRMAP_BG_B0: 63
  ADDRMAP_BG_B1: 63
```

## Memory profile parameter *board*

In order to control memory settings relating to **ODT** and general board tuning, this file can be used to define **all** parameters where a specific is needed which is different from the default or by this tool calculated value. As such, this file can be used to override specific parameters.

*Board file example (lan966x)*

```
dfitmg0:
- DFI_T_CTRL_DELAY: 4
- DFI_RDDATA_USE_DFI_PHY_CLK: 0
- DFI_T_RDDATA_EN: 3
- DFI_WRDATA_USE_DFI_PHY_CLK: 0
- DFI_TPHY_WRDATA: 1
- DFI_TPHY_WRLAT: 2
mr1:
- RTT_2: 1
```

All supported registers and sub-fields can be defined. See the full list of supported registers below.

## Generating a DDR configuration file

When generating a DDR configuration file, you will be using the `./scripts/gen_cfg.rb` script, and supplying the input profile file name as the first argument.

*cfg\_gen.rb argument syntax*

```
$ ./scripts/gen_cfg.rb --help
Usage: cfg_gen.rb [options] [config-file]
  -d, --debug                Enable debug messages
  -v, --verbose              Enable verbose messages
  -f, --format <format>     Use format (devicetree, yaml, source)
```

An example run could be:

*cfg\_gen.rb example run*

```
./scripts/gen_cfg.rb -f source configs/profiles/lan969x.yaml > config.c
```

And the output would be:



```
// SPDX-License-Identifier: (GPL-2.0+ OR MIT)
/*
 * Copyright (C) 2023 Microchip Technology Inc. and its subsidiaries.
 *
 */

#include <ddr_config.h>

const struct ddr_config lan969x_ddr_config = {
    .info = {
        .name = "lan969x 2023-02-27-14:45:24 d66calfcc1ec-dirty",
        .speed = 2400,
        .size = 0x40000000,
        .bus_width = 16,
    },
    .main = {
        .crcparctl1 = 0x00001000,
        .dbictl = 0x00000001,
        .dfimisc = 0x00000040,
        .dfitm0 = 0x038c820a,
        .dfitm1 = 0x00040201,
        .dfiupd0 = 0x40400003,
        .dfiupd1 = 0x004000ff,
        .ecccfg0 = 0x003f7f40,
        .init0 = 0x00020248,
        .init1 = 0x00e80000,
        .init3 = 0x0a340501,
        .init4 = 0x00180200,
        .init5 = 0x00110000,
        .init6 = 0x00000400,
        .init7 = 0x00000899,
        .mstr = 0x81040010,
        .pccfg = 0x00000000,
        .pwrctl = 0x00000000,
        .rfshctl0 = 0x00210010,
        .rfshctl3 = 0x00000000,
    },
    .timing = {
        .dramtm0 = 0x11132913,
        .dramtm1 = 0x0004051b,
        .dramtm12 = 0x1a000010,
        .dramtm2 = 0x0608050d,
        .dramtm3 = 0x0000400c,
        .dramtm4 = 0x08030409,
        .dramtm5 = 0x07070404,
        .dramtm8 = 0x05040c07,
        .dramtm9 = 0x0003040a,
        .odtcfg = 0x06000610,
        .rfshtmg = 0x006200d3,
    },
    .mapping = {
        .addrmap0 = 0x0000001f,
        .addrmap1 = 0x003f1818,
    }
};
```

```

        .addrmap2 = 0x00000000,
        .addrmap3 = 0x00000000,
        .addrmap4 = 0x00001f1f,
        .addrmap5 = 0x04040404,
        .addrmap6 = 0x04040404,
        .addrmap7 = 0x00000f0f,
        .addrmap8 = 0x00003f1a,
    },

    .phy = {
        .dcr = 0x0000040c,
        .dsgcr = 0x0064401b,
        .dtcr0 = 0x8000b0cf,
        .dtcr1 = 0x00010a37,
        .dxccr = 0x00c01884,
        .pgcr2 = 0x000147a2,
        .schcr1 = 0x00000000,
        .zq0pr = 0x0007bb00,
        .zq1pr = 0x0007bb00,
        .zq2pr = 0x00000000,
        .zqcr = 0x00058f00,
    },

    .phy_timing = {
        .dtpr0 = 0x0827100a,
        .dtpr1 = 0x28250119,
        .dtpr2 = 0x000701b1,
        .dtpr3 = 0x03000101,
        .dtpr4 = 0x01a50808,
        .dtpr5 = 0x00361009,
        .mr0 = 0x00000a34,
        .mr1 = 0x00000501,
        .mr2 = 0x00000018,
        .mr3 = 0x00000200,
        .mr4 = 0x00000800,
        .mr5 = 0x00000400,
        .mr6 = 0x00000899,
        .ptr0 = 0x4ae25710,
        .ptr1 = 0x74f4950e,
        .ptr2 = 0x00083def,
        .ptr3 = 0x1b192000,
        .ptr4 = 0x1003a000,
    },
};

```

Some platforms use the alternative `devicetree` format, but the procedure is the same as for `C` source.

You can also use the `yaml` format. It is especially useful for comparing alternate configurations using the `diff_cfg.rb` script. YAML configurations can also be output to `source` or `devicetree` configurations later with the `fmt_cfg.rb` script.

## Supported DDR configuration registers

The supported DDR configuration registers are a subset of the full UMCTL2 DDR controller registers. The registers supported in this tool have been identified to contain options that typically may need customization.

The configuration register set is currently different for the *lan966x* and the *lan969x/sparx5* driver, due to differences in the base IP version and IP configuration parameters.

register	lan966x	lan969x	sparx5
<b>ADDRMAP0</b>	yes	yes	yes
<b>ADDRMAP1</b>	yes	yes	yes
<b>ADDRMAP2</b>	yes	yes	yes
<b>ADDRMAP3</b>	yes	yes	yes
<b>ADDRMAP4</b>	yes	yes	yes
<b>ADDRMAP5</b>	yes	yes	yes
<b>ADDRMAP6</b>	yes	yes	yes
<b>ADDRMAP7</b>	<b>no</b>	yes	yes
<b>ADDRMAP8</b>	<b>no</b>	yes	yes
<b>CRCPARCTL1</b>	<b>no</b>	yes	yes
<b>DBICTL</b>	<b>no</b>	yes	yes
<b>DCR</b>	yes	yes	yes
<b>DFIMISC</b>	yes	yes	yes
<b>DFITMG0</b>	yes	yes	yes
<b>DFITMG1</b>	yes	yes	yes
<b>DFIUPD0</b>	yes	yes	yes
<b>DFIUPD1</b>	yes	yes	yes
<b>DRAMTMG0</b>	yes	yes	yes
<b>DRAMTMG1</b>	yes	yes	yes
<b>DRAMTMG12</b>	<b>no</b>	yes	yes
<b>DRAMTMG2</b>	yes	yes	yes

<b>DRAMTMG3</b>	yes	yes	yes
<b>DRAMTMG4</b>	yes	yes	yes
<b>DRAMTMG5</b>	yes	yes	yes
<b>DRAMTMG8</b>	yes	yes	yes
<b>DRAMTMG9</b>	<b>no</b>	yes	yes
<b>DSGCR</b>	yes	yes	yes
<b>DTCR</b>	yes	<b>no</b>	<b>no</b>
<b>DTCR0</b>	<b>no</b>	yes	yes
<b>DTCR1</b>	<b>no</b>	yes	yes
<b>DTPR0</b>	yes	yes	yes
<b>DTPR1</b>	yes	yes	yes
<b>DTPR2</b>	yes	yes	yes
<b>DTPR3</b>	<b>no</b>	yes	yes
<b>DTPR4</b>	<b>no</b>	yes	yes
<b>DTPR5</b>	<b>no</b>	yes	yes
<b>DXCCR</b>	yes	yes	yes
<b>ECCCFG0</b>	yes	yes	yes
<b>INIT0</b>	yes	yes	yes
<b>INIT1</b>	yes	yes	yes
<b>INIT3</b>	yes	yes	yes
<b>INIT4</b>	yes	yes	yes
<b>INIT5</b>	yes	yes	yes
<b>INIT6</b>	<b>no</b>	yes	yes
<b>INIT7</b>	<b>no</b>	yes	yes
<b>MR0</b>	yes	yes	yes
<b>MR1</b>	yes	yes	yes
<b>MR2</b>	yes	yes	yes

<b>MR3</b>	yes	yes	yes
<b>MR4</b>	<b>no</b>	yes	yes
<b>MR5</b>	<b>no</b>	yes	yes
<b>MR6</b>	<b>no</b>	yes	yes
<b>MSTR</b>	yes	yes	yes
<b>ODTCFG</b>	yes	yes	yes
<b>PCCFG</b>	yes	yes	yes
<b>PGCR2</b>	yes	yes	yes
<b>PTR0</b>	yes	yes	yes
<b>PTR1</b>	yes	yes	yes
<b>PTR2</b>	yes	yes	yes
<b>PTR3</b>	yes	yes	yes
<b>PTR4</b>	yes	yes	yes
<b>PWRCTL</b>	yes	yes	yes
<b>RFSHCTL0</b>	yes	yes	yes
<b>RFSHCTL3</b>	yes	yes	yes
<b>RFSHTMG</b>	yes	yes	yes
<b>SCHCR1</b>	<b>no</b>	yes	yes
<b>ZQ0CR0</b>	yes	<b>no</b>	<b>no</b>
<b>ZQ0CR1</b>	yes	<b>no</b>	<b>no</b>
<b>ZQ0PR</b>	<b>no</b>	yes	yes
<b>ZQ1CR0</b>	yes	<b>no</b>	<b>no</b>
<b>ZQ1CR1</b>	yes	<b>no</b>	<b>no</b>
<b>ZQ1PR</b>	<b>no</b>	yes	yes
<b>ZQ2PR</b>	<b>no</b>	yes	yes
<b>ZQCR</b>	<b>no</b>	yes	yes

Register fields below are given including start and end bits. The value following in parenthesis is the default value.

## ADDRMAP0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_CS_BIT0	bit 4..0 (0)	bit 4..0 (0)	bit 4..0 (0)

## ADDRMAP1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_BANK_B2	bit 5..16 (0)	bit 5..16 (0)	bit 5..16 (0)
ADDRMAP_BANK_B1	bit 5..8 (0)	bit 5..8 (0)	bit 5..8 (0)
ADDRMAP_BANK_B0	bit 5..0 (0)	bit 5..0 (0)	bit 5..0 (0)

## ADDRMAP2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_COL_B5	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)
ADDRMAP_COL_B4	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
ADDRMAP_COL_B3	bit 4..8 (0)	bit 4..8 (0)	bit 3..8 (0)
ADDRMAP_COL_B2	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

## ADDRMAP3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_COL_B9	bit 4..24 (0)	bit 4..24 (0)	bit 4..24 (0)
ADDRMAP_COL_B8	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
ADDRMAP_COL_B7	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
ADDRMAP_COL_B6	bit 4..0 (0)	bit 4..0 (0)	bit 3..0 (0)

## ADDRMAP4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>ADDRMAP_COL_B11</b>	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
<b>ADDRMAP_COL_B10</b>	bit 4..0 (0)	bit 4..0 (0)	bit 4..0 (0)

## ADDRMAP5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>ADDRMAP_ROW_B11</b>	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)
<b>ADDRMAP_ROW_B2_10</b>	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
<b>ADDRMAP_ROW_B1</b>	bit 3..8 (0)	bit 3..8 (0)	bit 3..8 (0)
<b>ADDRMAP_ROW_B0</b>	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

## ADDRMAP6

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>ADDRMAP_ROW_B15</b>	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)
<b>ADDRMAP_ROW_B14</b>	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
<b>ADDRMAP_ROW_B13</b>	bit 3..8 (0)	bit 3..8 (0)	bit 3..8 (0)
<b>ADDRMAP_ROW_B12</b>	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)
<b>LPDDR3_6GB_12GB</b>			bit 31 (0)

## ADDRMAP7

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>ADDRMAP_ROW_B16</b>		bit 3..0 (0)	bit 3..0 (0)
<b>ADDRMAP_ROW_B17</b>		bit 3..8 (0)	bit 3..8 (0)

## ADDRMAP8

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_BG_B0		bit 5..0 (0)	bit 5..0 (0)
ADDRMAP_BG_B1		bit 5..8 (0)	bit 5..8 (0)

## CRCPARCTL1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
PARITY_ENABLE		bit 0 (0)	bit 0 (0)
CRC_ENABLE		bit 4 (0)	bit 4 (0)
CRC_INC_DM		bit 7 (0)	bit 7 (0)
CAPARITY_DISABLE_BEFORE_SR		bit 12 (1)	bit 12 (1)

## DBICTL

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
DM_EN		bit 0 (1)	bit 0 (1)
WR_DBI_EN		bit 1 (0)	bit 1 (0)
RD_DBI_EN		bit 2 (0)	bit 2 (0)

## DCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
UDIMM	bit 29 (0)	bit 29 (0)	bit 29 (0)
DDR2T	bit 28 (0)	bit 28 (0)	bit 28 (0)
NOSRA	bit 27 (0)	bit 27 (0)	bit 27 (0)
BYTEMASK	bit 7..10 (1)	bit 7..10 (1)	bit 7..10 (1)
MPRDQ	bit 7 (0)	bit 7 (0)	bit 7 (0)
PDQ	bit 2..4 (0)	bit 2..4 (0)	bit 2..4 (0)
DDR8BNK	bit 3 (1)	bit 3 (1)	bit 3 (1)



<b>DDRMD</b>	bit 2..0 (3)	bit 2..0 (3)	bit 2..0 (3)
<b>DDRTYPE</b>		bit 1..8 (0)	bit 1..8 (0)
<b>RESERVED_26_18</b>		bit 8..18 (0)	bit 8..18 (0)
<b>UBG</b>		bit 30 (0)	bit 30 (0)
<b>RESERVED_31</b>		bit 31 (0)	bit 31 (0)

## DFIMISC

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DFI_FREQUENCY</b>	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
<b>DFI_INIT_START</b>	bit 5 (0)	bit 5 (0)	bit 5 (0)
<b>CTL_IDLE_EN</b>	bit 4 (0)	bit 4 (0)	bit 4 (0)
<b>DFI_INIT_COMPLETE_EN</b>	bit 0 (1)	bit 0 (1)	bit 0 (1)
<b>PHY_DBI_MODE</b>		bit 1 (0)	bit 1 (0)
<b>DIS_DYN_ADR_TRI</b>		bit 6 (1)	

## DFITMG0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DFI_T_CTRL_DELAY</b>	bit 4..24 (7)	bit 4..24 (7)	bit 4..24 (7)
<b>DFI_RDDATA_USE_DFI_PHY_CLK</b>	bit 23 (0)	bit 23 (0)	bit 23 (0)
<b>DFI_T_RDDATA_EN</b>	bit 6..16 (2)	bit 6..16 (2)	bit 6..16 (2)
<b>DFI_WRDATA_USE_DFI_PHY_CLK</b>	bit 15 (0)	bit 15 (0)	bit 15 (0)
<b>DFI_TPHY_WRDATA</b>	bit 5..8 (0)	bit 5..8 (0)	bit 5..8 (0)
<b>DFI_TPHY_WRLAT</b>	bit 5..0 (2)	bit 5..0 (2)	bit 5..0 (2)

## DFITMG1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
-------	---------	---------	--------

<b>DFI_T_PARIN_LAT</b>	bit 1..24 (0)	bit 1..24 (0)	bit 1..24 (0)
<b>DFI_T_WRDATA_DELAY</b>	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
<b>DFI_T_DRAM_CLK_DISABLE</b>	bit 4..8 (4)	bit 4..8 (4)	bit 4..8 (4)
<b>DFI_T_DRAM_CLK_ENABLE</b>	bit 4..0 (4)	bit 4..0 (4)	bit 4..0 (4)
<b>DFI_T_CMD_LAT</b>		bit 3..28 (0)	bit 3..28 (0)

## DFIUPD0

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>DIS_AUTO_CTRLUPD</b>	bit 31 (0)	bit 31 (0)	bit 31 (0)
<b>DIS_AUTO_CTRLUPD_SRX</b>	bit 30 (0)	bit 30 (0)	bit 30 (0)
<b>CTRLUPD_PRE_SRX</b>	bit 29 (0)	bit 29 (0)	bit 29 (0)
<b>DFI_T_CTRLUP_MAX</b>	bit 9..16 (64)	bit 9..16 (64)	bit 9..16 (64)
<b>DFI_T_CTRLUP_MIN</b>	bit 9..0 (3)	bit 9..0 (3)	bit 9..0 (3)

## DFIUPD1

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>DFI_T_CTRLUPD_INTERVAL_MIN_X1024</b>	bit 7..16 (1)	bit 7..16 (1)	bit 7..16 (1)
<b>DFI_T_CTRLUPD_INTERVAL_MAX_X1024</b>	bit 7..0 (1)	bit 7..0 (1)	bit 7..0 (1)

## DRAMTMGO

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>WR2PRE</b>	bit 6..24 (15)	bit 6..24 (15)	bit 6..24 (15)
<b>T_FAW</b>	bit 5..16 (16)	bit 5..16 (16)	bit 5..16 (16)
<b>T_RAS_MAX</b>	bit 6..8 (27)	bit 6..8 (27)	bit 6..8 (27)
<b>T_RAS_MIN</b>	bit 5..0 (15)	bit 5..0 (15)	bit 5..0 (15)

## DRAMTMG1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_XP</b>	bit 4..16 (8)	bit 4..16 (8)	bit 4..16 (8)
<b>RD2PRE</b>	bit 5..8 (4)	bit 5..8 (4)	bit 5..8 (4)
<b>T_RC</b>	bit 6..0 (20)	bit 6..0 (20)	bit 6..0 (20)

## DRAMTMG12

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_MRD_PDA</b>		bit 4..0 (16)	bit 4..0 (16)
<b>T_WR_MPR</b>		bit 5..24 (26)	

## DRAMTMG2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RD2WR</b>	bit 5..8 (6)	bit 5..8 (6)	bit 5..8 (6)
<b>WR2RD</b>	bit 5..0 (13)	bit 5..0 (13)	bit 5..0 (13)
<b>READ_LATENCY</b>		bit 5..16 (5)	bit 5..16 (5)
<b>WRITE_LATENCY</b>		bit 5..24 (3)	bit 5..24 (3)

## DRAMTMG3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_MRD</b>	bit 5..12 (4)	bit 5..12 (4)	bit 5..12 (4)
<b>T_MOD</b>	bit 9..0 (12)	bit 9..0 (12)	bit 9..0 (12)
<b>T_MRW</b>			bit 9..20 (5)

## DRAMTMG4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_RCD</b>	bit 4..24 (5)	bit 4..24 (5)	bit 4..24 (5)
<b>T_CCD</b>	bit 3..16 (4)	bit 3..16 (4)	bit 3..16 (4)
<b>T_RRD</b>	bit 3..8 (4)	bit 3..8 (4)	bit 3..8 (4)
<b>T_RP</b>	bit 4..0 (5)	bit 4..0 (5)	bit 4..0 (5)

## DRAMTMG5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_CKSRX</b>	bit 3..24 (5)	bit 3..24 (5)	bit 3..24 (5)
<b>T_CKSRE</b>	bit 6..16 (5)	bit 7..16 (5)	bit 3..16 (5)
<b>T_CKESR</b>	bit 5..8 (4)	bit 7..8 (4)	bit 5..8 (4)
<b>T_CKE</b>	bit 4..0 (3)	bit 4..0 (3)	bit 4..0 (3)

## DRAMTMG8

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_XS_DLL_X32</b>	bit 6..8 (68)	bit 6..8 (68)	bit 6..8 (68)
<b>T_XS_X32</b>	bit 6..0 (5)	bit 6..0 (5)	bit 6..0 (5)
<b>T_XS_ABORT_X32</b>		bit 6..16 (3)	bit 6..16 (3)
<b>T_XS_FAST_X32</b>		bit 6..24 (3)	bit 6..24 (3)

## DRAMTMG9

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>WR2RD_S</b>		bit 5..0 (13)	bit 5..0 (13)
<b>T_RRD_S</b>		bit 3..8 (4)	bit 3..8 (4)
<b>T_CCD_S</b>		bit 2..16 (4)	bit 2..16 (4)
<b>DDR4_WR_PREAMBLE</b>		bit 30 (0)	bit 30 (0)

## DSGCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>CKEOE</b>	bit 31 (1)		
<b>RSTOE</b>	bit 30 (1)	bit 21 (1)	bit 21 (1)
<b>ODTOE</b>	bit 29 (1)		
<b>CKOE</b>	bit 28 (1)		
<b>ODTPDD</b>	bit 3..24 (0)		
<b>CKEPDD</b>	bit 3..20 (0)		
<b>SDRMODE</b>	bit 19 (0)	bit 1..19 (0)	bit 1..19 (0)
<b>RRMODE</b>	bit 18 (0)		
<b>ATOAE</b>	bit 17 (0)	bit 17 (0)	bit 17 (0)
<b>DTOOE</b>	bit 16 (0)	bit 16 (0)	bit 16 (0)
<b>DTOIOM</b>	bit 15 (0)	bit 15 (0)	bit 15 (0)
<b>DTOPDR</b>	bit 14 (1)	bit 14 (1)	bit 14 (1)
<b>DTOPDD</b>	bit 13 (1)		
<b>DTOODT</b>	bit 12 (0)	bit 12 (0)	bit 12 (0)
<b>PUAD</b>	bit 3..8 (4)	bit 3..8 (0)	bit 3..8 (0)
<b>BRRMODE</b>	bit 7 (0)		
<b>DQSGX</b>	bit 6 (0)	bit 1..6 (0)	bit 1..6 (0)
<b>CUAEN</b>	bit 5 (0)	bit 5 (0)	bit 5 (0)
<b>LPPLLPD</b>	bit 4 (1)	bit 4 (1)	bit 4 (1)
<b>LPIOPD</b>	bit 3 (1)	bit 3 (1)	bit 3 (1)
<b>ZUEN</b>	bit 2 (1)		
<b>BDisEN</b>	bit 1 (1)	bit 1 (1)	bit 1 (1)
<b>PUREN</b>	bit 0 (1)	bit 0 (1)	bit 0 (1)
<b>CTLZUEN</b>		bit 2 (0)	bit 2 (0)

<b>RESERVED_13</b>		bit 13 (0)	bit 13 (0)
<b>WRRMODE</b>		bit 18 (1)	bit 18 (1)
<b>RRRMODE</b>		bit 22 (1)	bit 22 (1)
<b>PHYZUEN</b>		bit 23 (0)	bit 23 (0)
<b>LPACIOPD</b>		bit 24 (0)	
<b>RESERVED_31_25</b>		bit 6..25 (0)	
<b>RESERVED_31_24</b>			bit 7..24 (0)

## DTCR

Applies to: lan966x

Field	lan966x	lan969x	sparx5
<b>RFSHDT</b>	bit 3..28 (9)		
<b>RANKEN</b>	bit 3..24 (15)		
<b>DTEXD</b>	bit 22 (0)		
<b>DTDSTP</b>	bit 21 (0)		
<b>DTDEN</b>	bit 20 (0)		
<b>DTDBS</b>	bit 3..16 (0)		
<b>DTWDQMO</b>	bit 14 (0)		
<b>DTBDC</b>	bit 13 (1)		
<b>DTWBDDM</b>	bit 12 (1)		
<b>DTWDQM</b>	bit 3..8 (5)		
<b>DTCMPD</b>	bit 7 (1)		
<b>DTMPR</b>	bit 6 (0)		
<b>DTRANK</b>	bit 1..4 (0)		
<b>DTRPTN</b>	bit 3..0 (7)		

## DTCR0

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DTRPTN</b>		bit 3..0 (7)	bit 3..0 (7)
<b>RESERVED_5_4</b>		bit 1..4 (0)	bit 1..4 (0)
<b>DTMPR</b>		bit 6 (0)	bit 6 (0)
<b>DTCMPD</b>		bit 7 (1)	bit 7 (1)
<b>RESERVED_10_8</b>		bit 2..8 (0)	bit 2..8 (0)
<b>DTDBS4</b>		bit 11 (0)	bit 11 (0)
<b>DTWBDDM</b>		bit 12 (1)	bit 12 (1)
<b>DTBDC</b>		bit 13 (1)	bit 13 (1)
<b>DTRDBITR</b>		bit 1..14 (2)	bit 1..14 (2)
<b>DTDBS</b>		bit 3..16 (0)	bit 3..16 (0)
<b>DTDEN</b>		bit 20 (0)	bit 20 (0)
<b>DTDSTP</b>		bit 21 (0)	bit 21 (0)
<b>DTEXD</b>		bit 22 (0)	bit 22 (0)
<b>RESERVED_23</b>		bit 23 (0)	
<b>DTDRS</b>		bit 1..24 (0)	bit 1..24 (0)
<b>RESERVED_27_26</b>		bit 1..26 (0)	bit 1..26 (0)
<b>RFSHDT</b>		bit 3..28 (8)	bit 3..28 (8)
<b>DTEXG</b>			bit 23 (0)

## DTCR1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>BSTEN</b>		bit 0 (1)	bit 0 (1)
<b>RDLVLEN</b>		bit 1 (1)	bit 1 (1)
<b>RDPRMBL_TRN</b>		bit 2 (1)	bit 2 (1)
<b>RESERVED_3</b>		bit 3 (0)	bit 3 (0)
<b>RDLVLGS</b>		bit 2..4 (3)	bit 2..4 (3)

<b>RESERVED_7</b>		bit 7 (0)	bit 7 (0)
<b>RDLVLGDIFF</b>		bit 2..8 (2)	bit 2..8 (2)
<b>WLVDPRD</b>		bit 11 (1)	
<b>DTRANK</b>		bit 1..12 (0)	bit 1..12 (0)
<b>RESERVED_15_14</b>		bit 1..14 (0)	bit 1..14 (0)
<b>RANKEN</b>		bit 1..16 (3)	bit 1..16 (3)
<b>RANKEN_RSVD</b>		bit 13..18 (0)	bit 13..18 (0)
<b>RESERVED_11</b>			bit 11 (0)

## DTPRO

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TRC</b>	bit 5..26 (50)		
<b>TRRD</b>	bit 3..22 (7)	bit 5..24 (7)	bit 5..24 (7)
<b>TRAS</b>	bit 5..16 (36)	bit 6..16 (36)	bit 6..16 (36)
<b>TRCD</b>	bit 3..12 (14)		
<b>TRP</b>	bit 3..8 (14)	bit 6..8 (14)	bit 6..8 (14)
<b>TWTR</b>	bit 3..4 (8)		
<b>TRTP</b>	bit 3..0 (8)	bit 3..0 (8)	bit 3..0 (8)
<b>RESERVED_7_4</b>		bit 3..4 (0)	bit 3..4 (0)
<b>RESERVED_15</b>		bit 15 (0)	bit 15 (0)
<b>RESERVED_23</b>		bit 23 (0)	bit 23 (0)
<b>RESERVED_31_30</b>		bit 1..30 (0)	bit 1..30 (0)

## DTPR1

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TAON_OFF_D</b>	bit 1..30 (0)		



<b>TWLO</b>	bit 3..26 (8)		
<b>TWLMRD</b>	bit 5..20 (40)	bit 5..24 (40)	bit 5..24 (40)
<b>TRFC</b>	bit 8..11 (374)		
<b>TFAW</b>	bit 5..5 (38)	bit 7..16 (38)	bit 7..16 (38)
<b>TMOD</b>	bit 2..2 (4)	bit 2..8 (4)	bit 2..8 (4)
<b>TMRD</b>	bit 1..0 (2)	bit 4..0 (6)	bit 4..0 (6)
<b>RESERVED_7_5</b>		bit 2..5 (0)	bit 2..5 (0)
<b>RESERVED_15_11</b>		bit 4..11 (0)	bit 4..11 (0)
<b>RESERVED_31_30</b>		bit 1..30 (0)	bit 1..30 (0)

## DTPR2

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TCCD</b>	bit 31 (0)		
<b>TRTW</b>	bit 30 (0)	bit 28 (0)	bit 28 (0)
<b>TRTODT</b>	bit 29 (0)	bit 24 (0)	bit 24 (0)
<b>TDLLK</b>	bit 9..19 (512)		
<b>TCKE</b>	bit 3..15 (6)	bit 3..16 (6)	bit 3..16 (6)
<b>TXP</b>	bit 4..10 (26)		
<b>TXS</b>	bit 9..0 (512)	bit 9..0 (512)	bit 9..0 (512)
<b>RESERVED_15_10</b>		bit 5..10 (0)	bit 5..10 (0)
<b>RESERVED_23_20</b>		bit 3..20 (0)	bit 3..20 (0)
<b>RESERVED_27_25</b>		bit 2..25 (0)	bit 2..25 (0)
<b>RESERVED_31_29</b>		bit 2..29 (0)	bit 2..29 (0)

## DTPR3

Applies to: lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
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<b>TDQSCK</b>		bit 2..0 (1)	bit 2..0 (1)
<b>RESERVED_7_3</b>		bit 4..3 (0)	bit 4..3 (0)
<b>TDQSCKMAX</b>		bit 2..8 (1)	bit 2..8 (1)
<b>RESERVED_15_11</b>		bit 4..11 (0)	bit 4..11 (0)
<b>TDLLK</b>		bit 9..16 (384)	bit 9..16 (384)
<b>TCCD</b>		bit 2..26 (0)	bit 2..26 (0)
<b>TOFDX</b>		bit 2..29 (0)	bit 2..29 (0)

## DTPR4

Applies to: lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TXP</b>		bit 4..0 (26)	bit 4..0 (26)
<b>RESERVED_7_5</b>		bit 2..5 (0)	bit 2..5 (0)
<b>TWLO</b>		bit 3..8 (8)	bit 3..8 (8)
<b>RESERVED_15_12</b>		bit 3..12 (0)	bit 3..12 (0)
<b>TRFC</b>		bit 9..16 (374)	bit 9..16 (374)
<b>RESERVED_27_26</b>		bit 1..26 (0)	bit 1..26 (0)
<b>TAOND_TAOFD</b>		bit 1..28 (0)	bit 1..28 (0)
<b>RESERVED_31_30</b>		bit 1..30 (0)	bit 1..30 (0)

## DTPR5

Applies to: lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TWTR</b>		bit 4..0 (8)	bit 4..0 (8)
<b>RESERVED_7_5</b>		bit 2..5 (0)	bit 2..5 (0)
<b>TRCD</b>		bit 6..8 (14)	bit 6..8 (14)
<b>RESERVED_15</b>		bit 15 (0)	bit 15 (0)
<b>TRC</b>		bit 7..16 (50)	bit 7..16 (50)

<b>RESERVED_31_24</b>		bit 7..24 (0)	bit 7..24 (0)
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## DXCCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DDPDRCDO</b>	bit 3..28 (4)		
<b>DDPDDCDO</b>	bit 3..24 (4)		
<b>DYNDXPDR</b>	bit 23 (0)		
<b>DYNDXPDD</b>	bit 22 (0)		
<b>UDQIOM</b>	bit 21 (0)	bit 21 (0)	bit 21 (0)
<b>UDQPDR</b>	bit 20 (1)		
<b>UDQPDD</b>	bit 19 (1)		
<b>UDQODT</b>	bit 18 (0)		
<b>MSBUDQ</b>	bit 2..15 (0)	bit 2..15 (0)	bit 2..15 (0)
<b>DQSNRES</b>	bit 3..9 (12)	bit 3..9 (12)	bit 3..9 (12)
<b>DQSRES</b>	bit 3..5 (4)	bit 3..5 (4)	bit 3..5 (4)
<b>DXPDR</b>	bit 4 (0)		
<b>DXPDD</b>	bit 3 (0)		
<b>MDLEN</b>	bit 2 (1)	bit 2 (1)	bit 2 (1)
<b>DXIOM</b>	bit 1 (0)	bit 1 (0)	bit 1 (0)
<b>DXODT</b>	bit 0 (0)	bit 0 (0)	bit 0 (0)
<b>DQSGLB</b>		bit 1..3 (0)	bit 1..3 (0)
<b>DXSR</b>		bit 1..13 (0)	bit 1..13 (0)
<b>RESERVED_19_18</b>		bit 1..18 (0)	
<b>QSCNTENCTL</b>		bit 20 (0)	
<b>QSCNTEN</b>		bit 22 (1)	bit 22 (1)
<b>DXDCCBYP</b>		bit 23 (1)	bit 23 (1)
<b>RESERVED_28_24</b>		bit 4..24 (0)	bit 4..24 (0)

<b>RKLOOP</b>		bit 29 (1)	bit 29 (1)
<b>X4DQSM</b>		bit 30 (0)	bit 30 (0)
<b>X4MODE</b>		bit 31 (0)	bit 31 (0)
<b>RESERVED_20_18</b>			bit 2..18 (0)

## ECCCFG0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>ECC_REGION_MAP_GRANU</b>	bit 1..30 (0)	bit 1..30 (0)	
<b>ECC_REGION_MAP_OTHER</b>	bit 29 (0)	bit 29 (0)	
<b>ECC_AP_ERR_THRESHOLD</b>	bit 24 (0)	bit 24 (0)	
<b>BLK_CHANNEL_IDLE_TIME_X32</b>	bit 5..16 (63)	bit 5..16 (63)	
<b>ECC_REGION_MAP</b>	bit 6..8 (127)	bit 6..8 (127)	
<b>ECC_REGION_REMAP_EN</b>	bit 7 (0)	bit 7 (0)	
<b>ECC_AP_EN</b>	bit 6 (1)	bit 6 (1)	
<b>DIS_SCRUB</b>	bit 4 (0)	bit 4 (0)	bit 4 (0)
<b>ECC_MODE</b>	bit 2..0 (0)	bit 2..0 (0)	bit 2..0 (0)

## INIT0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>SKIP_DRAM_INIT</b>	bit 1..30 (0)	bit 1..30 (0)	bit 1..30 (0)
<b>POST_CKE_X1024</b>	bit 9..16 (2)	bit 9..16 (2)	bit 9..16 (2)
<b>PRE_CKE_X1024</b>	bit 11..0 (78)	bit 11..0 (78)	bit 11..0 (78)

## INIT1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
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<b>DRAM_RSTN_X1024</b>	bit 8..16 (0)	bit 8..16 (0)	bit 8..16 (0)
<b>PRE_OCD_X32</b>	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

## INIT3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>MR</b>	bit 15..16 (0)	bit 15..16 (0)	bit 15..16 (0)
<b>EMR</b>	bit 15..0 (1296)	bit 15..0 (1296)	bit 15..0 (1296)

## INIT4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>EMR2</b>	bit 15..16 (0)	bit 15..16 (0)	bit 15..16 (0)
<b>EMR3</b>	bit 15..0 (0)	bit 15..0 (0)	bit 15..0 (0)

## INIT5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DEV_ZQINIT_X32</b>	bit 7..16 (16)	bit 7..16 (16)	bit 7..16 (16)
<b>MAX_AUTO_INIT_X1024</b>			bit 9..0 (4)

## INIT6

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>MR5</b>		bit 15..0 (0)	bit 15..0 (0)
<b>MR4</b>		bit 15..16 (0)	bit 15..16 (0)

## INIT7

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
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<b>MR6</b>		bit 15..0 (0)	bit 15..0 (0)
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## MR0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RSVD_15_13</b>	bit 2..13 (0)	bit 2..13 (0)	bit 2..13 (0)
<b>PD</b>	bit 12 (0)	bit 12 (0)	bit 12 (0)
<b>WR</b>	bit 2..9 (5)	bit 2..9 (5)	bit 2..9 (5)
<b>DR</b>	bit 8 (0)	bit 8 (0)	bit 8 (0)
<b>TM</b>	bit 7 (0)	bit 7 (0)	bit 7 (0)
<b>CL_6_4</b>	bit 2..4 (5)	bit 2..4 (5)	bit 2..4 (5)
<b>BT</b>	bit 3 (0)	bit 3 (0)	bit 3 (0)
<b>CL_2</b>	bit 2 (0)	bit 2 (0)	bit 2 (0)
<b>BL</b>	bit 1..0 (2)	bit 1..0 (2)	bit 1..0 (2)
<b>RESERVED_31_16</b>		bit 15..16 (0)	bit 15..16 (0)

## MR1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RSVD_15_13</b>	bit 2..13 (0)	bit 2..13 (0)	bit 2..13 (0)
<b>QOFF</b>	bit 12 (0)	bit 12 (0)	bit 12 (0)
<b>TDQS</b>	bit 11 (0)	bit 11 (0)	bit 11 (0)
<b>RSVD_10</b>	bit 10 (0)	bit 10 (0)	bit 10 (0)
<b>RTT_9</b>	bit 9 (0)	bit 9 (0)	bit 9 (0)
<b>DE_RSVD_8</b>	bit 8 (0)		
<b>LEVEL</b>	bit 7 (0)	bit 7 (0)	bit 7 (0)
<b>RTT_6</b>	bit 6 (0)	bit 6 (0)	bit 6 (0)
<b>DIC_5</b>	bit 5 (0)	bit 5 (0)	bit 5 (0)

<b>AL</b>	bit 1..3 (0)	bit 1..3 (0)	bit 1..3 (0)
<b>RTT_2</b>	bit 2 (0)	bit 2 (0)	bit 2 (0)
<b>DIC_1</b>	bit 1 (0)	bit 1 (0)	bit 1 (0)
<b>DE</b>	bit 0 (0)	bit 0 (0)	bit 0 (0)
<b>RSVD_8</b>		bit 8 (0)	bit 8 (0)
<b>RESERVED_31_16</b>		bit 15..16 (0)	bit 15..16 (0)

## MR2

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>RSVD_15_11</b>	bit 4..11 (0)	bit 4..11 (0)	bit 4..11 (0)
<b>RTT_WR</b>	bit 1..9 (0)	bit 1..9 (0)	bit 1..9 (0)
<b>RSVD_8</b>	bit 8 (0)	bit 8 (0)	bit 8 (0)
<b>SRT</b>	bit 7 (0)	bit 7 (0)	bit 7 (0)
<b>ASR</b>	bit 6 (0)	bit 6 (0)	bit 6 (0)
<b>CWL</b>	bit 2..3 (0)	bit 2..3 (0)	bit 2..3 (0)
<b>PASR</b>	bit 2..0 (0)	bit 2..0 (0)	bit 2..0 (0)
<b>RESERVED_31_16</b>		bit 15..16 (0)	bit 15..16 (0)

## MR3

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>RSVD_15_3</b>	bit 12..3 (0)	bit 12..3 (0)	bit 12..3 (0)
<b>MPR</b>	bit 2 (0)	bit 2 (0)	bit 2 (0)
<b>MPRLOC</b>	bit 1..0 (0)	bit 1..0 (0)	bit 1..0 (0)
<b>RESERVED_31_16</b>		bit 15..16 (0)	bit 15..16 (0)

## MR4

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RSVD_15_0		bit 15..0 (0)	bit 15..0 (0)
RESERVED_31_16		bit 15..16 (0)	bit 15..16 (0)

## MR5

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RSVD_15_0		bit 15..0 (1024)	bit 15..0 (1024)
RESERVED_31_16		bit 15..16 (0)	bit 15..16 (0)

## MR6

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RSVD_15_0		bit 15..0 (1024)	bit 15..0 (1024)
RESERVED_31_16		bit 15..16 (0)	bit 15..16 (0)

## MSTR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ACTIVE_RANKS	bit 1..24 (3)	bit 1..24 (3)	bit 1..24 (3)
BURST_RDWR	bit 3..16 (4)	bit 3..16 (4)	bit 3..16 (4)
DLL_OFF_MODE	bit 15 (0)	bit 15 (0)	bit 15 (0)
DATA_BUS_WIDTH	bit 1..12 (0)	bit 1..12 (0)	bit 1..12 (0)
EN_2T_TIMING_MODE	bit 10 (0)	bit 10 (0)	bit 10 (0)
BURSTCHOP	bit 9 (0)	bit 9 (0)	bit 9 (0)
DDR3	bit 0 (1)	bit 0 (1)	bit 0 (1)
DDR4		bit 4 (0)	bit 4 (0)
GEARDOWN_MODE		bit 11 (0)	bit 11 (0)
DEVICE_CONFIG		bit 1..30 (0)	bit 1..30 (0)



<b>LPDDR2</b>			bit 2 (0)
<b>LPDDR3</b>			bit 3 (0)

## ODTCFG

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>WR_ODT_HOLD</b>	bit 3..24 (4)	bit 3..24 (4)	bit 3..24 (4)
<b>WR_ODT_DELAY</b>	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
<b>RD_ODT_HOLD</b>	bit 3..8 (4)	bit 3..8 (4)	bit 3..8 (4)
<b>RD_ODT_DELAY</b>	bit 4..2 (0)	bit 4..2 (0)	bit 4..2 (0)

## PCCFG

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>BL_EXP_MODE</b>	bit 8 (0)	bit 8 (0)	bit 8 (0)
<b>PAGEMATCH_LIMIT</b>	bit 4 (0)	bit 4 (0)	bit 4 (0)
<b>GO2CRITICAL_EN</b>	bit 0 (0)	bit 0 (0)	bit 0 (0)

## PGCR2

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>DYNACPDD</b>	bit 31 (0)		
<b>LPMSTRC0</b>	bit 30 (0)		
<b>ACPDDC</b>	bit 29 (0)		
<b>SHRAC</b>	bit 28 (0)		
<b>DTPMXTMR</b>	bit 7..20 (15)	bit 7..20 (0)	bit 7..20 (0)
<b>FXDLAT</b>	bit 19 (0)	bit 19 (0)	bit 19 (0)
<b>NOBUB</b>	bit 18 (0)		
<b>TREFPRD</b>	bit 17..0 (74880)	bit 17..0 (74880)	bit 17..0 (74880)

<b>CSNCIDMUX</b>		bit 18 (0)	bit 18 (0)
<b>FXDLATINCR</b>		bit 28 (0)	bit 28 (0)
<b>RFSHMODE</b>		bit 1..29 (0)	bit 1..29 (0)
<b>RESERVED_31</b>		bit 31 (0)	bit 31 (0)

## PTR0

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TPLLPD</b>	bit 10..21 (534)	bit 10..21 (534)	bit 10..21 (534)
<b>TPLLGS</b>	bit 14..6 (2134)	bit 14..6 (2134)	bit 14..6 (2134)
<b>TPHYRST</b>	bit 5..0 (16)	bit 5..0 (16)	bit 5..0 (16)

## PTR1

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TPLLLOCK</b>	bit 15..16 (53334)	bit 16..15 (53334)	bit 16..15 (53334)
<b>TPLLIRST</b>	bit 12..0 (4800)	bit 12..0 (4800)	bit 12..0 (4800)
<b>RESERVED_14_13</b>		bit 1..13 (0)	bit 1..13 (0)

## PTR2

Applies to: lan966x lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>TWLDLYS</b>	bit 4..15 (16)	bit 4..15 (16)	bit 4..15 (16)
<b>TCALH</b>	bit 4..10 (15)	bit 4..10 (15)	bit 4..10 (15)
<b>TCALS</b>	bit 4..5 (15)	bit 4..5 (15)	bit 4..5 (15)
<b>TCALON</b>	bit 4..0 (15)	bit 4..0 (15)	bit 4..0 (15)
<b>RESERVED_31_20</b>		bit 11..20 (0)	bit 11..20 (0)

## PTR3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>TDINIT1</b>	bit 9..20 (384)	bit 9..20 (384)	bit 9..20 (384)
<b>TDINIT0</b>	bit 19..0 (533334)	bit 19..0 (533334)	bit 19..0 (533334)
<b>RESERVED_31_30</b>		bit 1..30 (0)	bit 1..30 (0)

## PTR4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>TDINIT3</b>	bit 9..18 (683)	bit 10..18 (800)	bit 10..18 (800)
<b>TDINIT2</b>	bit 17..0 (213334)	bit 17..0 (213334)	bit 17..0 (213334)
<b>RESERVED_31_29</b>		bit 2..29 (0)	bit 2..29 (0)

## PWRCTL

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>DIS_CAM_DRAIN_SELFREF</b>	bit 7 (0)	bit 7 (0)	bit 7 (0)
<b>SELFREF_SW</b>	bit 5 (0)	bit 5 (0)	bit 5 (0)
<b>EN_DFI_DRAM_CLK_DISABLE</b>	bit 3 (0)	bit 3 (0)	bit 3 (0)
<b>POWERDOWN_EN</b>	bit 1 (0)	bit 1 (0)	bit 1 (0)
<b>SELFREF_EN</b>	bit 0 (0)	bit 0 (0)	bit 0 (0)
<b>MPSM_EN</b>		bit 4 (0)	bit 4 (0)
<b>DEEPPOWERDOWN_EN</b>			bit 2 (0)

## RFSHCTL0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>REFRESH_MARGIN</b>	bit 3..20 (2)	bit 3..20 (2)	bit 3..20 (2)
<b>REFRESH_TO_X1_X32</b>	bit 4..12 (16)	bit 4..12 (16)	
<b>REFRESH_BURST</b>	bit 5..4 (0)	bit 5..4 (0)	bit 4..4 (0)

<b>PER_BANK_REFRESH</b>			bit 2 (0)
<b>REFRESH_TO_X32</b>			bit 4..12 (16)

## RFSHCTL3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>REFRESH_UPDATE_LEVEL</b>	bit 1 (0)	bit 1 (0)	bit 1 (0)
<b>DIS_AUTO_REFRESH</b>	bit 0 (0)	bit 0 (0)	bit 0 (0)
<b>REFRESH_MODE</b>		bit 2..4 (0)	bit 2..4 (0)

## RFSHTMG

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>T_RFC_NOM_X1_X32</b>	bit 11..16 (98)	bit 11..16 (98)	
<b>T_RFC_MIN</b>	bit 9..0 (140)	bit 9..0 (140)	bit 9..0 (140)
<b>LPDDR3_TREFBW_EN</b>			bit 15 (0)
<b>T_RFC_NOM_X32</b>			bit 11..16 (98)

## SCHCR1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RESERVED_1_0</b>		bit 1..0 (0)	bit 1..0 (0)
<b>ALLRANK</b>		bit 2 (0)	bit 2 (0)
<b>RESERVED_3</b>		bit 3 (0)	bit 3 (0)
<b>SCBK</b>		bit 1..4 (0)	bit 1..4 (0)
<b>SCBG</b>		bit 1..6 (0)	bit 1..6 (0)
<b>SCADDR</b>		bit 19..8 (0)	bit 19..8 (0)
<b>SCRNK</b>		bit 3..28 (0)	bit 3..28 (0)

## ZQ0CR0

Applies to: lan966x

Field	lan966x	lan969x	sparx5
<b>ZQ0_ZQPD</b>	bit 31 (0)		
<b>ZQ0_ZCALEN</b>	bit 30 (1)		
<b>ZQ0_ZCALBYP</b>	bit 29 (0)		
<b>ZQ0_ZDEN</b>	bit 28 (0)		
<b>ZQ0_ZDATA</b>	bit 27..0 (330)		

## ZQ0CR1

Applies to: lan966x

Field	lan966x	lan969x	sparx5
<b>ZQ0_DFIPU1</b>	bit 17 (0)		
<b>ZQ0_DFIPU0</b>	bit 16 (0)		
<b>ZQ0_DFICCU</b>	bit 14 (0)		
<b>ZQ0_DFICU1</b>	bit 13 (0)		
<b>ZQ0_DFICU0</b>	bit 12 (1)		
<b>ZQ0_ZPROG</b>	bit 7..0 (123)		

## ZQ0PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RESERVED_7_0</b>		bit 7..0 (0)	
<b>ZPROG_ASYM_DRV_PU</b>		bit 3..8 (11)	bit 3..8 (11)
<b>ZPROG_ASYM_DRV_PD</b>		bit 3..12 (11)	bit 3..12 (11)
<b>ZPROG_PU_ODT_ONLY</b>		bit 3..16 (7)	bit 3..16 (7)
<b>PU_DRV_ADJUST</b>		bit 1..20 (0)	bit 1..20 (0)
<b>PD_DRV_ADJUST</b>		bit 1..22 (0)	bit 1..22 (0)

<b>RESERVED_27_24</b>		bit 3..24 (0)	
<b>PU_ODT_ONLY</b>		bit 28 (0)	
<b>ZSEGBYP</b>		bit 29 (0)	
<b>ODT_ZDEN</b>		bit 30 (0)	
<b>DRV_ZDEN</b>		bit 31 (0)	
<b>ZQDIV</b>			bit 7..0 (123)
<b>ZCTRL_UPPER</b>			bit 3..24 (0)
<b>RESERVED_31_28</b>			bit 3..28 (0)

## ZQ1CR0

Applies to: lan966x

Field	lan966x	lan969x	sparx5
<b>ZQ1_ZQPD</b>	bit 31 (0)		
<b>ZQ1_ZCALEN</b>	bit 30 (1)		
<b>ZQ1_ZCALBYP</b>	bit 29 (0)		
<b>ZQ1_ZDEN</b>	bit 28 (0)		
<b>ZQ1_ZDATA</b>	bit 27..0 (330)		

## ZQ1CR1

Applies to: lan966x

Field	lan966x	lan969x	sparx5
<b>ZQ1_DFIPU1</b>	bit 17 (0)		
<b>ZQ1_DFIPU0</b>	bit 16 (0)		
<b>ZQ1_DFICCU</b>	bit 14 (0)		
<b>ZQ1_DFICU1</b>	bit 13 (0)		
<b>ZQ1_DFICU0</b>	bit 12 (1)		
<b>ZQ1_ZPROG</b>	bit 7..0 (123)		

## ZQ1PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RESERVED_7_0</b>		bit 7..0 (0)	
<b>ZPROG_ASYM_DRV_PU</b>		bit 3..8 (11)	bit 3..8 (11)
<b>ZPROG_ASYM_DRV_PD</b>		bit 3..12 (11)	bit 3..12 (11)
<b>ZPROG_PU_ODT_ONLY</b>		bit 3..16 (7)	bit 3..16 (7)
<b>PU_DRV_ADJUST</b>		bit 1..20 (0)	bit 1..20 (0)
<b>PD_DRV_ADJUST</b>		bit 1..22 (0)	bit 1..22 (0)
<b>RESERVED_27_24</b>		bit 3..24 (0)	
<b>PU_ODT_ONLY</b>		bit 28 (0)	
<b>ZSEGBYP</b>		bit 29 (0)	
<b>ODT_ZDEN</b>		bit 30 (0)	
<b>DRV_ZDEN</b>		bit 31 (0)	
<b>ZQDIV</b>			bit 7..0 (123)
<b>ZCTRL_UPPER</b>			bit 3..24 (0)
<b>RESERVED_31_28</b>			bit 3..28 (0)

## ZQ2PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
<b>RESERVED_7_0</b>		bit 7..0 (0)	
<b>ZPROG_ASYM_DRV_PU</b>		bit 3..8 (0)	bit 3..8 (11)
<b>ZPROG_ASYM_DRV_PD</b>		bit 3..12 (0)	bit 3..12 (11)
<b>ZPROG_PU_ODT_ONLY</b>		bit 3..16 (0)	bit 3..16 (7)
<b>PU_DRV_ADJUST</b>		bit 1..20 (0)	bit 1..20 (0)
<b>PD_DRV_ADJUST</b>		bit 1..22 (0)	bit 1..22 (0)
<b>RESERVED_27_24</b>		bit 3..24 (0)	

<b>PU_ODT_ONLY</b>		bit 28 (0)	
<b>ZSEGBYP</b>		bit 29 (0)	
<b>ODT_ZDEN</b>		bit 30 (0)	
<b>DRV_ZDEN</b>		bit 31 (0)	
<b>ZQDIV</b>			bit 7..0 (123)
<b>ZCTRL_UPPER</b>			bit 3..24 (0)
<b>RESERVED_31_28</b>			bit 3..28 (0)

## ZQCR

Applies to: lan969x sparx5

<b>Field</b>	<b>lan966x</b>	<b>lan969x</b>	<b>sparx5</b>
<b>RESERVED_0</b>		bit 0 (0)	bit 0 (0)
<b>TERM_OFF</b>		bit 1 (0)	bit 1 (0)
<b>ZQPD</b>		bit 2 (0)	bit 2 (0)
<b>RESERVED_7_3</b>		bit 4..3 (0)	bit 4..3 (0)
<b>PGWAIT</b>		bit 2..8 (5)	bit 2..8 (5)
<b>ZCALT</b>		bit 2..11 (1)	bit 2..11 (1)
<b>AVGMAX</b>		bit 1..14 (2)	bit 1..14 (2)
<b>AVGEN</b>		bit 16 (1)	bit 16 (1)
<b>IODLMT</b>		bit 7..17 (2)	bit 6..17 (2)
<b>RESERVED_26_25</b>		bit 1..25 (0)	
<b>FORCE_ZCAL_VT_UPDATE</b>		bit 27 (0)	bit 27 (0)
<b>RESERVED_31_28</b>		bit 3..28 (0)	
<b>ASYM_DRV_EN</b>			bit 24 (0)
<b>PU_ODT_ONLY</b>			bit 25 (0)
<b>DIS_NON_LIN_COMP</b>			bit 26 (1)
<b>ZCTRL_UPPER</b>			bit 3..28 (0)



## References

- [1] DesignWare Cores Enhanced Universal DDR Memory Controller (uMCTL2) Databook