DDR configuration tool for Microchip platforms

Technical Note

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TERMS and ABBREVIATIONS

```
HIF                Host Interface
ODT                On-Die Termination
PUB                PHY utility block
SoC                System on a Chip
```

Requirements

The tools are developed using the `ruby` scripting language, which must be available.

The scripts may run under both `Linux` or `Windows`. The `Windows` environment may require installing the `WSL2` package to emulate `Linux`.

Supported platforms

This tool is supported form the following target SoC platforms:

- sparx5 (ARMv8 A53 dual-core)
- lan966x (ARMV7 A7 single-core)
- lan969x (ARMv8 A53 single-core)

Introduction

This software package contain a set of tools that can create DDR configurations specific to a target platform and board design. A board design defines the physical DDR memory system, such that the DDR controller needs a carefully crafted configuration to ensure a stable and effective operation.

The DDR controller supported is the *Synopsis uMCTL2* DesignWare component, accompanied with a *Synopsis PHY Utility Block*.

The supported platforms all use DDR3 or DDR3 + DDR4.

Workflow

The tool works by accepting a *configuration profile* as input, which can be transformed into a compact representation of the many configuration options the target, **specifically** generated for a given platform and board.

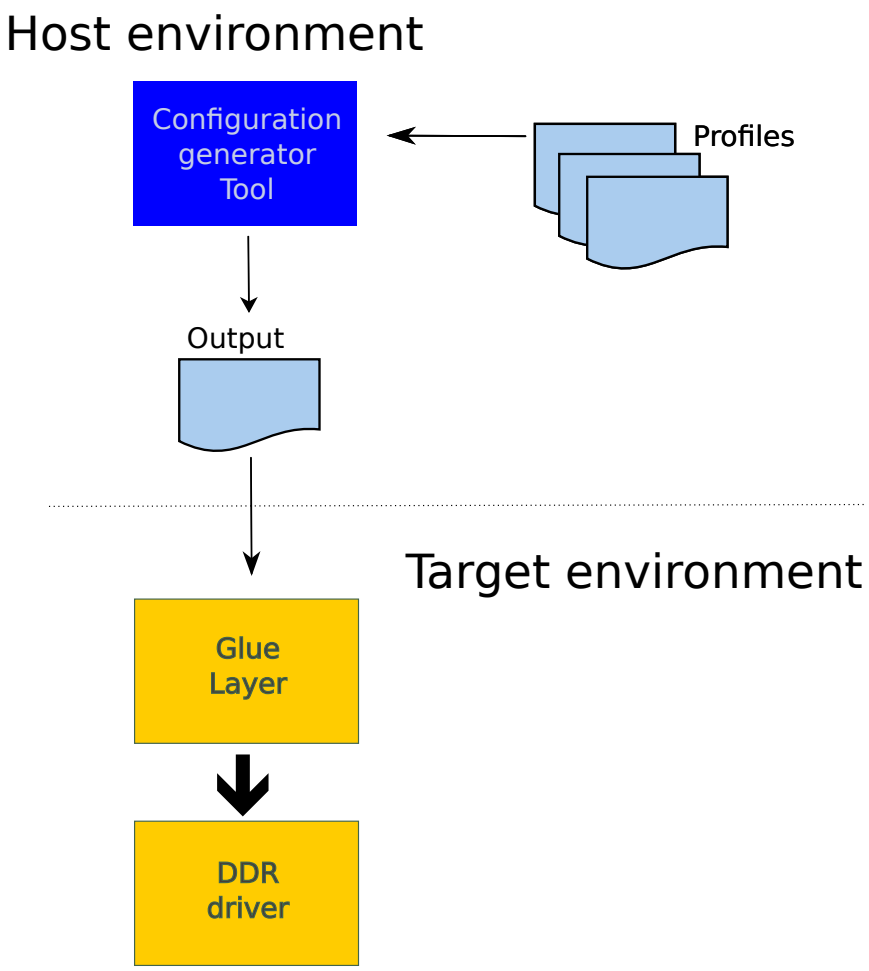
The output configuration may be represented in different formats, depending on the target platform.

The different formats are:

format	platform	comments
source	lan966x	The configuration is output to "C" code, and compiled into the target firmware.
devicetree	lan969x, sparx5	The configuration is output to device-tree format, which is added to a a target image (as a separate entity).
yaml	-none-	The configuration is stored in YAML format. The format can be used for documentation purposes as well as for comparing with other configurations.

The output representation is dictated by the target implementation of the actual target system DDR driver operating environment. Specifically, 'device tree' support may not be available on a given target (Example: `lan966x`).

The workflow of working with the DDR configuration is illustrated below:



Configuration parameters

At the top level, the following user-level parameters are available:

Keyword	Type	Description
`platform`	`sparx5 | lan966x | lan969x`	The name of the target platform SoC
`clock_speed`	`integer`	The clock speed of the DDR data bus. See later.

Keyword	Type	Description
mem_size	integer	Total Memory Size (in Mbytes)
mem_type	DDR3 | DDR4	The DDR memory type of the equipped DDR devices.
device_bus_width	x8 | x16	Bus width of the equipped DDR devices. x8 support is experimental.
enable_half_bus	boolean	Configures the memory topology to use only half of the SoC data bus width
enable_quarter_bus	boolean	Configures the memory topology to use only 1/4 of the SoC data bus width
active_ranks	integer	The number of (active) ranks in the memory topology.
ecc_mode	0 | 4	The ECC mode to employ. ECC mode 0 implies ECC is disabled, mode 4 is "sec/ded over 1 beat"
mem_profile	string	The filename of a file defining DDR memory address generation. See later.
_2T_mode	boolean	Whether 2T timing should be used
board	string	The filename of file containing board specific tuning parameters. See later.

Bus width

The bus width of the SoC differs between different platforms. Below is an overview of the (maximum) bus width supported per platform.

Platform	Bus Width
sparx5	32
lan966x	16
lan969x	16

The effective bus width can optionally be reduced with the `enable_half_bus` or the `enable_quarter_bus` parameter. The effective bus width must be at least 8 bits, such that `enable_quarter_bus` is only supported on `sparx5`.

The `device_bus_width` parameter describe the bus width of the individual DDR chips - of which there may be several. For example, a `sparx5` 32-bit topology with ECC will require 5 chips of `x8` width to naturally match the 32 bits data plus the ECC bits. Using `enable_half_bus` you could use 3 chips of `x16` width, but you would be leaving half of the ECC memory device unused - while having a simpler physical board layout.

Clock speed.

The *clock_speed* affects a lot of the calculated parameters for the memory controller.

Whether or not the clock speed can be changed or not, depends on the target system (and the actual driver implementation).

The current state of the clock speed is described below.

Platform	Supported clocks	Notes
`sparx5`	`2500 | 2000 | 1667 | 1250`	NB: DDR4 will only work at 1667 Mhz
`lan966x`	`1200`	Fixed clock
`lan969x`	`2400 | 2133| 1866 | 1600`	Default should be 2400 Mhz

Memory profile parameter *mem_profile*

In order to define the way HIF addresses are used to select ranks, groups and DDR devices, a separate YAML file is used. This configuration file may be used by several configurations (board designs) using similar physical DDR topology.

The *mem_profile* file defines the so-called "address map" registers (and sub-fields). An example is given below.

Note: The registers and sub-fields vary a little between platforms, so not all registers apply to all supported platforms. Refer to [1], section "2.11: Address Mapper".

Address map definition example

```
addrmap0:
  ADDRMAP_CS_BIT0: 31
addrmap1:
  ADDRMAP_BANK_B0: 24
  ADDRMAP_BANK_B1: 24
  ADDRMAP_BANK_B2: 24
addrmap2:
  ADDRMAP_COL_B2: 0
  ADDRMAP_COL_B3: 0
  ADDRMAP_COL_B4: 0
  ADDRMAP_COL_B5: 0
addrmap3:
  ADDRMAP_COL_B6: 0
  ADDRMAP_COL_B7: 0
  ADDRMAP_COL_B8: 0
  ADDRMAP_COL_B9: 0
addrmap4:
  ADDRMAP_COL_B10: 31
  ADDRMAP_COL_B11: 31
addrmap5:
  ADDRMAP_ROW_B0: 4
  ADDRMAP_ROW_B1: 4
  ADDRMAP_ROW_B2_10: 4
  ADDRMAP_ROW_B11: 4
addrmap6:
  ADDRMAP_ROW_B12: 4
  ADDRMAP_ROW_B13: 4
  ADDRMAP_ROW_B14: 4
  ADDRMAP_ROW_B15: 4
  LPDDR3_6GB_12GB: 0
addrmap7:
  ADDRMAP_ROW_B16: 15
  ADDRMAP_ROW_B17: 15
addrmap8:
  ADDRMAP_BG_B0: 63
  ADDRMAP_BG_B1: 63
```

Memory profile parameter *board*

In order to control memory settings relating to `ODT` and general board tuning, this file can be used to define **all** parameters where a specific is needed which is different from the default or by this tool calculated value. As such, this file can be used to override specific parameters.

Board file example (lan966x)

```
dfitmg0:
  - DFI_T_CTRL_DELAY: 4
  - DFI_RDDATA_USE_DFI_PHY_CLK: 0
  - DFI_T_RDDATA_EN: 3
  - DFI_WRDATA_USE_DFI_PHY_CLK: 0
  - DFI_TPHY_WRDATA: 1
  - DFI_TPHY_WRLAT: 2
mr1:
  - RTT_2: 1
```

All supported registers and sub-fields can be defined. See the full list of supported registers below.

Generating a DDR configuration file

When generating a DDR configuration file, you will be using the *./scripts/gen_cfg.rb* script, and supplying the input profile file name as the first argument.

cfg_gen.rb argument syntax

```
$ ./scripts/gen_cfg.rb --help
Usage: cfg_gen.rb [options] [config-file]
    -d, --debug                      Enable debug messages
    -v, --verbose                    Enable verbose messages
    -f, --format <format>            Use format (devicetree, yaml, source)
```

An example run could be:

cfg_gen.rb example run

```
./scripts/gen_cfg.rb -f source configs/profiles/lan969x.yaml > config.c
```

And the output would be:

```
// SPDX-License-Identifier: (GPL-2.0+ OR MIT)
/*
 * Copyright (C) 2023 Microchip Technology Inc. and its subsidiaries.
 *
 */

#include <ddr_config.h>

const struct ddr_config lan969x_ddr_config = {
        .info = {
                .name = "lan969x 2023-02-27-14:45:24 d66ca1fcc1ec-dirty",
                .speed = 2400,
                .size = 0x40000000,
                .bus_width = 16,
        },
        .main = {
                .crcparctl1 = 0x00001000,
                .dbictl = 0x00000001,
                .dfimisc = 0x00000040,
                .dfitmg0 = 0x038c820a,
                .dfitmg1 = 0x00040201,
                .dfiupd0 = 0x40400003,
                .dfiupd1 = 0x004000ff,
                .ecccfg0 = 0x003f7f40,
                .init0 = 0x00020248,
                .init1 = 0x00e80000,
                .init3 = 0x0a340501,
                .init4 = 0x00180200,
                .init5 = 0x00110000,
                .init6 = 0x00000400,
                .init7 = 0x00000899,
                .mstr = 0x81040010,
                .pccfg = 0x00000000,
                .pwrctl = 0x00000000,
                .rfshctl0 = 0x00210010,
                .rfshctl3 = 0x00000000,
        },

        .timing = {
                .dramtmg0 = 0x11132913,
                .dramtmg1 = 0x0004051b,
                .dramtmg12 = 0x1a000010,
                .dramtmg2 = 0x0608050d,
                .dramtmg3 = 0x0000400c,
                .dramtmg4 = 0x08030409,
                .dramtmg5 = 0x07070404,
                .dramtmg8 = 0x05040c07,
                .dramtmg9 = 0x0003040a,
                .odtcfg = 0x06000610,
                .rfshtmg = 0x006200d3,
        },

        .mapping = {
                .addrmap0 = 0x0000001f,
                .addrmap1 = 0x003f1818,
```

```
                .addrmap2 = 0x00000000,
                .addrmap3 = 0x00000000,
                .addrmap4 = 0x00001f1f,
                .addrmap5 = 0x04040404,
                .addrmap6 = 0x04040404,
                .addrmap7 = 0x00000f0f,
                .addrmap8 = 0x00003f1a,
        },

        .phy = {
                .dcr = 0x0000040c,
                .dsgcr = 0x0064401b,
                .dtcr0 = 0x8000b0cf,
                .dtcr1 = 0x00010a37,
                .dxccr = 0x00c01884,
                .pgcr2 = 0x000147a2,
                .schcr1 = 0x00000000,
                .zq0pr = 0x0007bb00,
                .zq1pr = 0x0007bb00,
                .zq2pr = 0x00000000,
                .zqcr = 0x00058f00,
        },

        .phy_timing = {
                .dtpr0 = 0x0827100a,
                .dtpr1 = 0x28250119,
                .dtpr2 = 0x000701b1,
                .dtpr3 = 0x03000101,
                .dtpr4 = 0x01a50808,
                .dtpr5 = 0x00361009,
                .ptr0 = 0x4ae25710,
                .ptr1 = 0x74f4950e,
                .ptr2 = 0x00083def,
                .ptr3 = 0x1b192000,
                .ptr4 = 0x1003a000,
        },

};
```

Some platforms use the alternative `devicetree` format, but the procedure is the same as for `C` source.

You can also use the `yaml` format. It is especially useful for comparing alternate configurations using the *diff_cfg.rb* script. YAML configurations can also be output to `source` or `devicetree` configurations later with the *fmt_cfg.rb* script.

Supported DDR configuration registers

The supported DDR configuration registers are a subset of the full UMCTL2 DDR controller registers. The registers supported in this tool have been identified to contain options that typically may need customization.

The configuration register set is currently different for the *lan966x* and the *lan969x*/*sparx5* driver, due to differences in the base IP version and IP configuration parameters.

register	lan966x	lan969x	sparx5
ADDRMAP0	yes	yes	yes
ADDRMAP1	yes	yes	yes
ADDRMAP2	yes	yes	yes
ADDRMAP3	yes	yes	yes
ADDRMAP4	yes	yes	yes
ADDRMAP5	yes	yes	yes
ADDRMAP6	yes	yes	yes
ADDRMAP7	**no**	yes	yes
ADDRMAP8	**no**	yes	yes
CRCPARCTL1	**no**	yes	yes
DBICTL	**no**	yes	yes
DCR	yes	yes	yes
DFIMISC	yes	yes	yes
DFITMG0	yes	yes	yes
DFITMG1	yes	yes	yes
DFIUPD0	yes	yes	yes
DFIUPD1	yes	yes	yes
DRAMTMG0	yes	yes	yes
DRAMTMG1	yes	yes	yes
DRAMTMG12	**no**	yes	yes
DRAMTMG2	yes	yes	yes
DRAMTMG3	yes	yes	yes
DRAMTMG4	yes	yes	yes
DRAMTMG5	yes	yes	yes

DRAMTMG8	yes	yes	yes
DRAMTMG9	**no**	yes	yes
DSGCR	yes	yes	yes
DTCR	yes	**no**	**no**
DTCR0	**no**	yes	yes
DTCR1	**no**	yes	yes
DTPR0	yes	yes	yes
DTPR1	yes	yes	yes
DTPR2	yes	yes	yes
DTPR3	**no**	yes	yes
DTPR4	**no**	yes	yes
DTPR5	**no**	yes	yes
DXCCR	yes	yes	yes
ECCCFG0	yes	yes	yes
INIT0	yes	yes	yes
INIT1	yes	yes	yes
INIT3	yes	yes	yes
INIT4	yes	yes	yes
INIT5	yes	yes	yes
INIT6	**no**	yes	yes
INIT7	**no**	yes	yes
MSTR	yes	yes	yes
ODTCFG	yes	yes	yes
PCCFG	yes	yes	yes
PGCR2	yes	yes	yes
PTR0	yes	yes	yes
PTR1	yes	yes	yes

PTR2	yes	yes	yes
PTR3	yes	yes	yes
PTR4	yes	yes	yes
PWRCTL	yes	yes	yes
RFSHCTL0	yes	yes	yes
RFSHCTL3	yes	yes	yes
RFSHTMG	yes	yes	yes
SBRCTL	**no**	**no**	yes
SCHCR1	**no**	yes	yes
ZQ0CR0	yes	**no**	**no**
ZQ0CR1	yes	**no**	**no**
ZQ0PR	**no**	yes	yes
ZQ1CR0	yes	**no**	**no**
ZQ1CR1	yes	**no**	**no**
ZQ1PR	**no**	yes	yes
ZQ2PR	**no**	yes	yes
ZQCR	**no**	yes	yes

Register fields below are given including start and end bits. The value following in parenthesis is the default value.

ADDRMAP0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_CS_BIT0	bit 4..0 (0)	bit 4..0 (0)	bit 4..0 (0)

ADDRMAP1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_BANK_B2	bit 5..16 (0)	bit 5..16 (0)	bit 5..16 (0)

ADDRMAP_BANK_B1	bit 5..8 (0)	bit 5..8 (0)	bit 5..8 (0)
ADDRMAP_BANK_B0	bit 5..0 (0)	bit 5..0 (0)	bit 5..0 (0)

ADDRMAP2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_COL_B5	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)
ADDRMAP_COL_B4	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
ADDRMAP_COL_B3	bit 4..8 (0)	bit 4..8 (0)	bit 3..8 (0)
ADDRMAP_COL_B2	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

ADDRMAP3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_COL_B9	bit 4..24 (0)	bit 4..24 (0)	bit 4..24 (0)
ADDRMAP_COL_B8	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
ADDRMAP_COL_B7	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
ADDRMAP_COL_B6	bit 4..0 (0)	bit 4..0 (0)	bit 3..0 (0)

ADDRMAP4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_COL_B11	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
ADDRMAP_COL_B10	bit 4..0 (0)	bit 4..0 (0)	bit 4..0 (0)

ADDRMAP5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_ROW_B11	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)

ADDRMAP_ROW_B2_10	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
ADDRMAP_ROW_B1	bit 3..8 (0)	bit 3..8 (0)	bit 3..8 (0)
ADDRMAP_ROW_B0	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

ADDRMAP6

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_ROW_B15	bit 3..24 (0)	bit 3..24 (0)	bit 3..24 (0)
ADDRMAP_ROW_B14	bit 3..16 (0)	bit 3..16 (0)	bit 3..16 (0)
ADDRMAP_ROW_B13	bit 3..8 (0)	bit 3..8 (0)	bit 3..8 (0)
ADDRMAP_ROW_B12	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)
LPDDR3_6GB_12GB			bit 31 (0)

ADDRMAP7

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_ROW_B16		bit 3..0 (0)	bit 3..0 (0)
ADDRMAP_ROW_B17		bit 3..8 (0)	bit 3..8 (0)

ADDRMAP8

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
ADDRMAP_BG_B0		bit 5..0 (0)	bit 5..0 (0)
ADDRMAP_BG_B1		bit 5..8 (0)	bit 5..8 (0)

CRCPARCTL1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
PARITY_ENABLE		bit 0 (0)	bit 0 (0)

CRC_ENABLE		bit 4 (0)	bit 4 (0)
CRC_INC_DM		bit 7 (0)	bit 7 (0)
CAPARITY_DISABLE_BEFORE_SR		bit 12 (1)	bit 12 (1)

DBICTL

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
DM_EN		bit 0 (1)	bit 0 (1)
WR_DBI_EN		bit 1 (0)	bit 1 (0)
RD_DBI_EN		bit 2 (0)	bit 2 (0)

DCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
UDIMM	bit 29 (0)	bit 29 (0)	bit 29 (0)
DDR2T	bit 28 (0)	bit 28 (0)	bit 28 (0)
NOSRA	bit 27 (0)	bit 27 (0)	bit 27 (0)
BYTEMASK	bit 7..10 (1)	bit 7..10 (1)	bit 7..10 (1)
MPRDQ	bit 7 (0)	bit 7 (0)	bit 7 (0)
PDQ	bit 2..4 (0)	bit 2..4 (0)	bit 2..4 (0)
DDR8BNK	bit 3 (1)	bit 3 (1)	bit 3 (1)
DDRMD	bit 2..0 (3)	bit 2..0 (3)	bit 2..0 (3)
DDRTYPE		bit 1..8 (0)	bit 1..8 (0)
RESERVED_26_18		bit 8..18 (0)	bit 8..18 (0)
UBG		bit 30 (0)	bit 30 (0)
RESERVED_31		bit 31 (0)	bit 31 (0)

DFIMISC

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DFI_FREQUENCY	bit 4..8 (0)	bit 4..8 (0)	bit 4..8 (0)
DFI_INIT_START	bit 5 (0)	bit 5 (0)	bit 5 (0)
CTL_IDLE_EN	bit 4 (0)	bit 4 (0)	bit 4 (0)
DFI_INIT_COMPLETE_EN	bit 0 (1)	bit 0 (1)	bit 0 (1)
PHY_DBI_MODE		bit 1 (0)	bit 1 (0)
DIS_DYN_ADR_TRI		bit 6 (1)	

DFITMG0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DFI_T_CTRL_DELAY	bit 4..24 (7)	bit 4..24 (7)	bit 4..24 (7)
DFI_RDDATA_USE_DFI_PHY_CLK	bit 23 (0)	bit 23 (0)	bit 23 (0)
DFI_T_RDDATA_EN	bit 6..16 (2)	bit 6..16 (2)	bit 6..16 (2)
DFI_WRDATA_USE_DFI_PHY_CLK	bit 15 (0)	bit 15 (0)	bit 15 (0)
DFI_TPHY_WRDATA	bit 5..8 (0)	bit 5..8 (0)	bit 5..8 (0)
DFI_TPHY_WRLAT	bit 5..0 (2)	bit 5..0 (2)	bit 5..0 (2)

DFITMG1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DFI_T_PARIN_LAT	bit 1..24 (0)	bit 1..24 (0)	bit 1..24 (0)
DFI_T_WRDATA_DELAY	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
DFI_T_DRAM_CLK_DISABLE	bit 4..8 (4)	bit 4..8 (4)	bit 4..8 (4)
DFI_T_DRAM_CLK_ENABLE	bit 4..0 (4)	bit 4..0 (4)	bit 4..0 (4)
DFI_T_CMD_LAT		bit 3..28 (0)	bit 3..28 (0)

DFIUPD0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DIS_AUTO_CTRLUPD	bit 31 (0)	bit 31 (0)	bit 31 (0)
DIS_AUTO_CTRLUPD_SRX	bit 30 (0)	bit 30 (0)	bit 30 (0)
CTRLUPD_PRE_SRX	bit 29 (0)	bit 29 (0)	bit 29 (0)
DFI_T_CTRLUP_MAX	bit 9..16 (64)	bit 9..16 (64)	bit 9..16 (64)
DFI_T_CTRLUP_MIN	bit 9..0 (3)	bit 9..0 (3)	bit 9..0 (3)

DFIUPD1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DFI_T_CTRLUPD_INTERVAL_MIN_X1024	bit 7..16 (1)	bit 7..16 (1)	bit 7..16 (1)
DFI_T_CTRLUPD_INTERVAL_MAX_X1024	bit 7..0 (1)	bit 7..0 (1)	bit 7..0 (1)

DRAMTMG0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
WR2PRE	bit 6..24 (15)	bit 6..24 (15)	bit 6..24 (15)
T_FAW	bit 5..16 (16)	bit 5..16 (16)	bit 5..16 (16)
T_RAS_MAX	bit 6..8 (27)	bit 6..8 (27)	bit 6..8 (27)
T_RAS_MIN	bit 5..0 (15)	bit 5..0 (15)	bit 5..0 (15)

DRAMTMG1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_XP	bit 4..16 (8)	bit 4..16 (8)	bit 4..16 (8)
RD2PRE	bit 5..8 (4)	bit 5..8 (4)	bit 5..8 (4)
T_RC	bit 6..0 (20)	bit 6..0 (20)	bit 6..0 (20)

DRAMTMG12

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
T_MRD_PDA		bit 4..0 (16)	bit 4..0 (16)
T_WR_MPR		bit 5..24 (26)	

DRAMTMG2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
RD2WR	bit 5..8 (6)	bit 5..8 (6)	bit 5..8 (6)
WR2RD	bit 5..0 (13)	bit 5..0 (13)	bit 5..0 (13)
READ_LATENCY		bit 5..16 (5)	bit 5..16 (5)
WRITE_LATENCY		bit 5..24 (3)	bit 5..24 (3)

DRAMTMG3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_MRD	bit 5..12 (4)	bit 5..12 (4)	bit 5..12 (4)
T_MOD	bit 9..0 (12)	bit 9..0 (12)	bit 9..0 (12)
T_MRW			bit 9..20 (5)

DRAMTMG4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_RCD	bit 4..24 (5)	bit 4..24 (5)	bit 4..24 (5)
T_CCD	bit 3..16 (4)	bit 3..16 (4)	bit 3..16 (4)
T_RRD	bit 3..8 (4)	bit 3..8 (4)	bit 3..8 (4)
T_RP	bit 4..0 (5)	bit 4..0 (5)	bit 4..0 (5)

DRAMTMG5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_CKSRX	bit 3..24 (5)	bit 3..24 (5)	bit 3..24 (5)
T_CKSRE	bit 6..16 (5)	bit 7..16 (5)	bit 3..16 (5)
T_CKESR	bit 5..8 (4)	bit 7..8 (4)	bit 5..8 (4)
T_CKE	bit 4..0 (3)	bit 4..0 (3)	bit 4..0 (3)

DRAMTMG8

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_XS_DLL_X32	bit 6..8 (68)	bit 6..8 (68)	bit 6..8 (68)
T_XS_X32	bit 6..0 (5)	bit 6..0 (5)	bit 6..0 (5)
T_XS_ABORT_X32		bit 6..16 (3)	bit 6..16 (3)
T_XS_FAST_X32		bit 6..24 (3)	bit 6..24 (3)

DRAMTMG9

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
WR2RD_S		bit 5..0 (13)	bit 5..0 (13)
T_RRD_S		bit 3..8 (4)	bit 3..8 (4)
T_CCD_S		bit 2..16 (4)	bit 2..16 (4)
DDR4_WR_PREAMBLE		bit 30 (0)	bit 30 (0)

DSGCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
CKEOE	bit 31 (1)		
RSTOE	bit 30 (1)	bit 21 (1)	bit 21 (1)

ODTOE	bit 29 (1)		
CKOE	bit 28 (1)		
ODTPDD	bit 3..24 (0)		
CKEPDD	bit 3..20 (0)		
SDRMODE	bit 19 (0)	bit 1..19 (0)	bit 1..19 (0)
RRMODE	bit 18 (0)		
ATOAE	bit 17 (0)	bit 17 (0)	bit 17 (0)
DTOOE	bit 16 (0)	bit 16 (0)	bit 16 (0)
DTOIOM	bit 15 (0)	bit 15 (0)	bit 15 (0)
DTOPDR	bit 14 (1)	bit 14 (1)	bit 14 (1)
DTOPDD	bit 13 (1)		
DTOODT	bit 12 (0)	bit 12 (0)	bit 12 (0)
PUAD	bit 3..8 (4)	bit 3..8 (0)	bit 3..8 (0)
BRRMODE	bit 7 (0)		
DQSGX	bit 6 (0)	bit 1..6 (0)	bit 1..6 (0)
CUAEN	bit 5 (0)	bit 5 (0)	bit 5 (0)
LPPLLPD	bit 4 (1)	bit 4 (1)	bit 4 (1)
LPIOPD	bit 3 (1)	bit 3 (1)	bit 3 (1)
ZUEN	bit 2 (1)		
BDISEN	bit 1 (1)	bit 1 (1)	bit 1 (1)
PUREN	bit 0 (1)	bit 0 (1)	bit 0 (1)
CTLZUEN		bit 2 (0)	bit 2 (0)
RESERVED_13		bit 13 (0)	bit 13 (0)
WRRMODE		bit 18 (1)	bit 18 (1)
RRRMODE		bit 22 (1)	bit 22 (1)
PHYZUEN		bit 23 (0)	bit 23 (0)
LPACIOPD		bit 24 (0)	

RESERVED_31_25		bit 6..25 (0)	
RESERVED_31_24			bit 7..24 (0)

DTCR

Applies to: lan966x

Field	lan966x	lan969x	sparx5
RFSHDT	bit 3..28 (9)		
RANKEN	bit 3..24 (15)		
DTEXD	bit 22 (0)		
DTDSTP	bit 21 (0)		
DTDEN	bit 20 (0)		
DTDBS	bit 3..16 (0)		
DTWDQMO	bit 14 (0)		
DTBDC	bit 13 (1)		
DTWBDDM	bit 12 (1)		
DTWDQM	bit 3..8 (5)		
DTCMPD	bit 7 (1)		
DTMPR	bit 6 (0)		
DTRANK	bit 1..4 (0)		
DTRPTN	bit 3..0 (7)		

DTCR0

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
DTRPTN		bit 3..0 (7)	bit 3..0 (7)
RESERVED_5_4		bit 1..4 (0)	bit 1..4 (0)
DTMPR		bit 6 (0)	bit 6 (0)
DTCMPD		bit 7 (1)	bit 7 (1)

RESERVED_10_8		bit 2..8 (0)	bit 2..8 (0)
DTDBS4		bit 11 (0)	bit 11 (0)
DTWBDDM		bit 12 (1)	bit 12 (1)
DTBDC		bit 13 (1)	bit 13 (1)
DTRDBITR		bit 1..14 (2)	bit 1..14 (2)
DTDBS		bit 3..16 (0)	bit 3..16 (0)
DTDEN		bit 20 (0)	bit 20 (0)
DTDSTP		bit 21 (0)	bit 21 (0)
DTEXD		bit 22 (0)	bit 22 (0)
RESERVED_23		bit 23 (0)	
DTDRS		bit 1..24 (0)	bit 1..24 (0)
RESERVED_27_26		bit 1..26 (0)	bit 1..26 (0)
RFSHDT		bit 3..28 (8)	bit 3..28 (8)
DTEXG			bit 23 (0)

DTCR1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
BSTEN		bit 0 (1)	bit 0 (1)
RDLVLEN		bit 1 (1)	bit 1 (1)
RDPRMBL_TRN		bit 2 (1)	bit 2 (1)
RESERVED_3		bit 3 (0)	bit 3 (0)
RDLVLGS		bit 2..4 (3)	bit 2..4 (3)
RESERVED_7		bit 7 (0)	bit 7 (0)
RDLVLGDIFF		bit 2..8 (2)	bit 2..8 (2)
WLVLDPRD		bit 11 (1)	
DTRANK		bit 1..12 (0)	bit 1..12 (0)
RESERVED_15_14		bit 1..14 (0)	bit 1..14 (0)

RANKEN		bit 1..16 (3)	bit 1..16 (3)
RANKEN_RSVD		bit 13..18 (0)	bit 13..18 (0)
RESERVED_11			bit 11 (0)

DTPR0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TRC	bit 5..26 (50)		
TRRD	bit 3..22 (7)	bit 5..24 (7)	bit 5..24 (7)
TRAS	bit 5..16 (36)	bit 6..16 (36)	bit 6..16 (36)
TRCD	bit 3..12 (14)		
TRP	bit 3..8 (14)	bit 6..8 (14)	bit 6..8 (14)
TWTR	bit 3..4 (8)		
TRTP	bit 3..0 (8)	bit 3..0 (8)	bit 3..0 (8)
RESERVED_7_4		bit 3..4 (0)	bit 3..4 (0)
RESERVED_15		bit 15 (0)	bit 15 (0)
RESERVED_23		bit 23 (0)	bit 23 (0)
RESERVED_31_30		bit 1..30 (0)	bit 1..30 (0)

DTPR1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TAON_OFF_D	bit 1..30 (0)		
TWLO	bit 3..26 (8)		
TWLMRD	bit 5..20 (40)	bit 5..24 (40)	bit 5..24 (40)
TRFC	bit 8..11 (374)		
TFAW	bit 5..5 (38)	bit 7..16 (38)	bit 7..16 (38)
TMOD	bit 2..2 (4)	bit 2..8 (4)	bit 2..8 (4)

TMRD	bit 1..0 (2)	bit 4..0 (6)	bit 4..0 (6)
RESERVED_7_5		bit 2..5 (0)	bit 2..5 (0)
RESERVED_15_11		bit 4..11 (0)	bit 4..11 (0)
RESERVED_31_30		bit 1..30 (0)	bit 1..30 (0)

DTPR2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TCCD	bit 31 (0)		
TRTW	bit 30 (0)	bit 28 (0)	bit 28 (0)
TRTODT	bit 29 (0)	bit 24 (0)	bit 24 (0)
TDLLK	bit 9..19 (512)		
TCKE	bit 3..15 (6)	bit 3..16 (6)	bit 3..16 (6)
TXP	bit 4..10 (26)		
TXS	bit 9..0 (512)	bit 9..0 (512)	bit 9..0 (512)
RESERVED_15_10		bit 5..10 (0)	bit 5..10 (0)
RESERVED_23_20		bit 3..20 (0)	bit 3..20 (0)
RESERVED_27_25		bit 2..25 (0)	bit 2..25 (0)
RESERVED_31_29		bit 2..29 (0)	bit 2..29 (0)

DTPR3

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
TDQSCK		bit 2..0 (1)	bit 2..0 (1)
RESERVED_7_3		bit 4..3 (0)	bit 4..3 (0)
TDQSCKMAX		bit 2..8 (1)	bit 2..8 (1)
RESERVED_15_11		bit 4..11 (0)	bit 4..11 (0)
TDLLK		bit 9..16 (384)	bit 9..16 (384)

TCCD		bit 2..26 (0)	bit 2..26 (0)
TOFDX		bit 2..29 (0)	bit 2..29 (0)

DTPR4

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
TXP		bit 4..0 (26)	bit 4..0 (26)
RESERVED_7_5		bit 2..5 (0)	bit 2..5 (0)
TWLO		bit 3..8 (8)	bit 3..8 (8)
RESERVED_15_12		bit 3..12 (0)	bit 3..12 (0)
TRFC		bit 9..16 (374)	bit 9..16 (374)
RESERVED_27_26		bit 1..26 (0)	bit 1..26 (0)
TAOND_TAOFD		bit 1..28 (0)	bit 1..28 (0)
RESERVED_31_30		bit 1..30 (0)	bit 1..30 (0)

DTPR5

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
TWTR		bit 4..0 (8)	bit 4..0 (8)
RESERVED_7_5		bit 2..5 (0)	bit 2..5 (0)
TRCD		bit 6..8 (14)	bit 6..8 (14)
RESERVED_15		bit 15 (0)	bit 15 (0)
TRC		bit 7..16 (50)	bit 7..16 (50)
RESERVED_31_24		bit 7..24 (0)	bit 7..24 (0)

DXCCR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DDPDRCDO	bit 3..28 (4)		

DDPDDCDO	bit 3..24 (4)		
DYNDXPDR	bit 23 (0)		
DYNDXPDD	bit 22 (0)		
UDQIOM	bit 21 (0)	bit 21 (0)	bit 21 (0)
UDQPDR	bit 20 (1)		
UDQPDD	bit 19 (1)		
UDQODT	bit 18 (0)		
MSBUDQ	bit 2..15 (0)	bit 2..15 (0)	bit 2..15 (0)
DQSNRES	bit 3..9 (12)	bit 3..9 (12)	bit 3..9 (12)
DQSRES	bit 3..5 (4)	bit 3..5 (4)	bit 3..5 (4)
DXPDR	bit 4 (0)		
DXPDD	bit 3 (0)		
MDLEN	bit 2 (1)	bit 2 (1)	bit 2 (1)
DXIOM	bit 1 (0)	bit 1 (0)	bit 1 (0)
DXODT	bit 0 (0)	bit 0 (0)	bit 0 (0)
DQSGLB		bit 1..3 (0)	bit 1..3 (0)
DXSR		bit 1..13 (0)	bit 1..13 (0)
RESERVED_19_18		bit 1..18 (0)	
QSCNTENCTL		bit 20 (0)	
QSCNTEN		bit 22 (1)	bit 22 (1)
DXDCCBYP		bit 23 (1)	bit 23 (1)
RESERVED_28_24		bit 4..24 (0)	bit 4..24 (0)
RKLOOP		bit 29 (1)	bit 29 (1)
X4DQSMD		bit 30 (0)	bit 30 (0)
X4MODE		bit 31 (0)	bit 31 (0)
RESERVED_20_18			bit 2..18 (0)

ECCCFG0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
ECC_REGION_MAP_GRANU	bit 1..30 (0)	bit 1..30 (0)	
ECC_REGION_MAP_OTHER	bit 29 (0)	bit 29 (0)	
ECC_AP_ERR_THRESHOLD	bit 24 (0)	bit 24 (0)	
BLK_CHANNEL_IDLE_TIME_X32	bit 5..16 (63)	bit 5..16 (63)	
ECC_REGION_MAP	bit 6..8 (127)	bit 6..8 (127)	
ECC_REGION_REMAP_EN	bit 7 (0)	bit 7 (0)	
ECC_AP_EN	bit 6 (1)	bit 6 (1)	
DIS_SCRUB	bit 4 (0)	bit 4 (0)	bit 4 (0)
ECC_MODE	bit 2..0 (0)	bit 2..0 (0)	bit 2..0 (0)

INIT0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
SKIP_DRAM_INIT	bit 1..30 (0)	bit 1..30 (0)	bit 1..30 (0)
POST_CKE_X1024	bit 9..16 (2)	bit 9..16 (2)	bit 9..16 (2)
PRE_CKE_X1024	bit 11..0 (78)	bit 11..0 (78)	bit 11..0 (78)

INIT1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DRAM_RSTN_X1024	bit 8..16 (0)	bit 8..16 (0)	bit 8..16 (0)
PRE_OCD_X32	bit 3..0 (0)	bit 3..0 (0)	bit 3..0 (0)

INIT3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
MR	bit 15..16 (0)	bit 15..16 (0)	bit 15..16 (0)
EMR	bit 15..0 (1296)	bit 15..0 (1296)	bit 15..0 (1296)

INIT4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
EMR2	bit 15..16 (0)	bit 15..16 (0)	bit 15..16 (0)
EMR3	bit 15..0 (0)	bit 15..0 (0)	bit 15..0 (0)

INIT5

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DEV_ZQINIT_X32	bit 7..16 (16)	bit 7..16 (16)	bit 7..16 (16)
MAX_AUTO_INIT_X1024			bit 9..0 (4)

INIT6

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
MR5		bit 15..0 (0)	bit 15..0 (0)
MR4		bit 15..16 (0)	bit 15..16 (0)

INIT7

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
MR6		bit 15..0 (0)	bit 15..0 (0)

MSTR

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5

ACTIVE_RANKS	bit 1..24 (3)	bit 1..24 (3)	bit 1..24 (3)
BURST_RDWR	bit 3..16 (4)	bit 3..16 (4)	bit 3..16 (4)
DLL_OFF_MODE	bit 15 (0)	bit 15 (0)	bit 15 (0)
DATA_BUS_WIDTH	bit 1..12 (0)	bit 1..12 (0)	bit 1..12 (0)
EN_2T_TIMING_MODE	bit 10 (0)	bit 10 (0)	bit 10 (0)
BURSTCHOP	bit 9 (0)	bit 9 (0)	bit 9 (0)
DDR3	bit 0 (1)	bit 0 (1)	bit 0 (1)
DDR4		bit 4 (0)	bit 4 (0)
GEARDOWN_MODE		bit 11 (0)	bit 11 (0)
DEVICE_CONFIG		bit 1..30 (0)	bit 1..30 (0)
LPDDR2			bit 2 (0)
LPDDR3			bit 3 (0)

ODTCFG

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
WR_ODT_HOLD	bit 3..24 (4)	bit 3..24 (4)	bit 3..24 (4)
WR_ODT_DELAY	bit 4..16 (0)	bit 4..16 (0)	bit 4..16 (0)
RD_ODT_HOLD	bit 3..8 (4)	bit 3..8 (4)	bit 3..8 (4)
RD_ODT_DELAY	bit 4..2 (0)	bit 4..2 (0)	bit 4..2 (0)

PCCFG

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
BL_EXP_MODE	bit 8 (0)	bit 8 (0)	bit 8 (0)
PAGEMATCH_LIMIT	bit 4 (0)	bit 4 (0)	bit 4 (0)
GO2CRITICAL_EN	bit 0 (0)	bit 0 (0)	bit 0 (0)

PGCR2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DYNACPDD	bit 31 (0)		
LPMSTRC0	bit 30 (0)		
ACPDDC	bit 29 (0)		
SHRAC	bit 28 (0)		
DTPMXTMR	bit 7..20 (15)	bit 7..20 (0)	bit 7..20 (0)
FXDLAT	bit 19 (0)	bit 19 (0)	bit 19 (0)
NOBUB	bit 18 (0)		
TREFPRD	bit 17..0 (74880)	bit 17..0 (74880)	bit 17..0 (74880)
CSNCIDMUX		bit 18 (0)	bit 18 (0)
FXDLATINCR		bit 28 (0)	bit 28 (0)
RFSHMODE		bit 1..29 (0)	bit 1..29 (0)
RESERVED_31		bit 31 (0)	bit 31 (0)

PTR0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TPLLPD	bit 10..21 (534)	bit 10..21 (534)	bit 10..21 (534)
TPLLGS	bit 14..6 (2134)	bit 14..6 (2134)	bit 14..6 (2134)
TPHYRST	bit 5..0 (16)	bit 5..0 (16)	bit 5..0 (16)

PTR1

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TPLLLOCK	bit 15..16 (53334)	bit 16..15 (53334)	bit 16..15 (53334)
TPLLRST	bit 12..0 (4800)	bit 12..0 (4800)	bit 12..0 (4800)

RESERVED_14_13		bit 1..13 (0)	bit 1..13 (0)

PTR2

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TWLDLYS	bit 4..15 (16)	bit 4..15 (16)	bit 4..15 (16)
TCALH	bit 4..10 (15)	bit 4..10 (15)	bit 4..10 (15)
TCALS	bit 4..5 (15)	bit 4..5 (15)	bit 4..5 (15)
TCALON	bit 4..0 (15)	bit 4..0 (15)	bit 4..0 (15)
RESERVED_31_20		bit 11..20 (0)	bit 11..20 (0)

PTR3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TDINIT1	bit 9..20 (384)	bit 9..20 (384)	bit 9..20 (384)
TDINIT0	bit 19..0 (533334)	bit 19..0 (533334)	bit 19..0 (533334)
RESERVED_31_30		bit 1..30 (0)	bit 1..30 (0)

PTR4

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
TDINIT3	bit 9..18 (683)	bit 10..18 (800)	bit 10..18 (800)
TDINIT2	bit 17..0 (213334)	bit 17..0 (213334)	bit 17..0 (213334)
RESERVED_31_29		bit 2..29 (0)	bit 2..29 (0)

PWRCTL

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
DIS_CAM_DRAIN_SELFREF	bit 7 (0)	bit 7 (0)	bit 7 (0)

SELFREF_SW	bit 5 (0)	bit 5 (0)	bit 5 (0)
EN_DFI_DRAM_CLK_DISABLE	bit 3 (0)	bit 3 (0)	bit 3 (0)
POWERDOWN_EN	bit 1 (0)	bit 1 (0)	bit 1 (0)
SELFREF_EN	bit 0 (0)	bit 0 (0)	bit 0 (0)
MPSM_EN		bit 4 (0)	bit 4 (0)
DEEPPOWERDOWN_EN			bit 2 (0)

RFSHCTL0

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
REFRESH_MARGIN	bit 3..20 (2)	bit 3..20 (2)	bit 3..20 (2)
REFRESH_TO_X1_X32	bit 4..12 (16)	bit 4..12 (16)	
REFRESH_BURST	bit 5..4 (0)	bit 5..4 (0)	bit 4..4 (0)
PER_BANK_REFRESH			bit 2 (0)
REFRESH_TO_X32			bit 4..12 (16)

RFSHCTL3

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
REFRESH_UPDATE_LEVEL	bit 1 (0)	bit 1 (0)	bit 1 (0)
DIS_AUTO_REFRESH	bit 0 (0)	bit 0 (0)	bit 0 (0)
REFRESH_MODE		bit 2..4 (0)	bit 2..4 (0)

RFSHTMG

Applies to: lan966x lan969x sparx5

Field	lan966x	lan969x	sparx5
T_RFC_NOM_X1_X32	bit 11..16 (98)	bit 11..16 (98)	
T_RFC_MIN	bit 9..0 (140)	bit 9..0 (140)	bit 9..0 (140)
LPDDR3_TREFBW_EN			bit 15 (0)

T_RFC_NOM_X32			bit 11..16 (98)

SBRCTL

Applies to:

sparx5

Field	lan966x	lan969x	sparx5
SCRUB_INTERVAL	bit 12..8 (255)	bit 12..8 (255)	bit 12..8 (255)
SCRUB_BURST	bit 2..4 (1)	bit 2..4 (1)	bit 2..4 (1)
SCRUB_MODE	bit 2 (0)	bit 2 (0)	bit 2 (0)
SCRUB_DURING_LOWPOWER	bit 1 (0)	bit 1 (0)	bit 1 (0)
SCRUB_EN	bit 0 (0)	bit 0 (0)	bit 0 (0)

SCHCR1

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RESERVED_1_0		bit 1..0 (0)	bit 1..0 (0)
ALLRANK		bit 2 (0)	bit 2 (0)
RESERVED_3		bit 3 (0)	bit 3 (0)
SCBK		bit 1..4 (0)	bit 1..4 (0)
SCBG		bit 1..6 (0)	bit 1..6 (0)
SCADDR		bit 19..8 (0)	bit 19..8 (0)
SCRNK		bit 3..28 (0)	bit 3..28 (0)

ZQ0CR0

Applies to: lan966x

Field	lan966x	lan969x	sparx5
ZQ0_ZQPD	bit 31 (0)		
ZQ0_ZCALEN	bit 30 (1)		

ZQ0_ZCALBYP	bit 29 (0)		
ZQ0_ZDEN	bit 28 (0)		
ZQ0_ZDATA	bit 27..0 (330)		

ZQ0CR1

Applies to: lan966x

Field	lan966x	lan969x	sparx5
ZQ0_DFIPU1	bit 17 (0)		
ZQ0_DFIPU0	bit 16 (0)		
ZQ0_DFICCU	bit 14 (0)		
ZQ0_DFICU1	bit 13 (0)		
ZQ0_DFICU0	bit 12 (1)		
ZQ0_ZPROG	bit 7..0 (123)		

ZQ0PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RESERVED_7_0		bit 7..0 (0)	
ZPROG_ASYM_DRV_PU		bit 3..8 (11)	bit 3..8 (11)
ZPROG_ASYM_DRV_PD		bit 3..12 (11)	bit 3..12 (11)
ZPROG_PU_ODT_ONLY		bit 3..16 (7)	bit 3..16 (7)
PU_DRV_ADJUST		bit 1..20 (0)	bit 1..20 (0)
PD_DRV_ADJUST		bit 1..22 (0)	bit 1..22 (0)
RESERVED_27_24		bit 3..24 (0)	
PU_ODT_ONLY		bit 28 (0)	
ZSEGBYP		bit 29 (0)	
ODT_ZDEN		bit 30 (0)	
DRV_ZDEN		bit 31 (0)	

ZQDIV			bit 7..0 (123)
ZCTRL_UPPER			bit 3..24 (0)
RESERVED_31_28			bit 3..28 (0)

ZQ1CR0

Applies to: lan966x

Field	lan966x	lan969x	sparx5
ZQ1_ZQPD	bit 31 (0)		
ZQ1_ZCALEN	bit 30 (1)		
ZQ1_ZCALBYP	bit 29 (0)		
ZQ1_ZDEN	bit 28 (0)		
ZQ1_ZDATA	bit 27..0 (330)		

ZQ1CR1

Applies to: lan966x

Field	lan966x	lan969x	sparx5
ZQ1_DFIPU1	bit 17 (0)		
ZQ1_DFIPU0	bit 16 (0)		
ZQ1_DFICCU	bit 14 (0)		
ZQ1_DFICU1	bit 13 (0)		
ZQ1_DFICU0	bit 12 (1)		
ZQ1_ZPROG	bit 7..0 (123)		

ZQ1PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RESERVED_7_0		bit 7..0 (0)	
ZPROG_ASYM_DRV_PU		bit 3..8 (11)	bit 3..8 (11)
ZPROG_ASYM_DRV_PD		bit 3..12 (11)	bit 3..12 (11)

ZPROG_PU_ODT_ONLY		bit 3..16 (7)	bit 3..16 (7)
PU_DRV_ADJUST		bit 1..20 (0)	bit 1..20 (0)
PD_DRV_ADJUST		bit 1..22 (0)	bit 1..22 (0)
RESERVED_27_24		bit 3..24 (0)	
PU_ODT_ONLY		bit 28 (0)	
ZSEGBYP		bit 29 (0)	
ODT_ZDEN		bit 30 (0)	
DRV_ZDEN		bit 31 (0)	
ZQDIV			bit 7..0 (123)
ZCTRL_UPPER			bit 3..24 (0)
RESERVED_31_28			bit 3..28 (0)

ZQ2PR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RESERVED_7_0		bit 7..0 (0)	
ZPROG_ASYM_DRV_PU		bit 3..8 (0)	bit 3..8 (11)
ZPROG_ASYM_DRV_PD		bit 3..12 (0)	bit 3..12 (11)
ZPROG_PU_ODT_ONLY		bit 3..16 (0)	bit 3..16 (7)
PU_DRV_ADJUST		bit 1..20 (0)	bit 1..20 (0)
PD_DRV_ADJUST		bit 1..22 (0)	bit 1..22 (0)
RESERVED_27_24		bit 3..24 (0)	
PU_ODT_ONLY		bit 28 (0)	
ZSEGBYP		bit 29 (0)	
ODT_ZDEN		bit 30 (0)	
DRV_ZDEN		bit 31 (0)	
ZQDIV			bit 7..0 (123)
ZCTRL_UPPER			bit 3..24 (0)

RESERVED_31_28			bit 3..28 (0)

ZQCR

Applies to: lan969x sparx5

Field	lan966x	lan969x	sparx5
RESERVED_0		bit 0 (0)	bit 0 (0)
TERM_OFF		bit 1 (0)	bit 1 (0)
ZQPD		bit 2 (0)	bit 2 (0)
RESERVED_7_3		bit 4..3 (0)	bit 4..3 (0)
PGWAIT		bit 2..8 (5)	bit 2..8 (5)
ZCALT		bit 2..11 (1)	bit 2..11 (1)
AVGMAX		bit 1..14 (2)	bit 1..14 (2)
AVGEN		bit 16 (1)	bit 16 (1)
IODLMT		bit 7..17 (2)	bit 6..17 (2)
RESERVED_26_25		bit 1..25 (0)	
FORCE_ZCAL_VT_UPDATE		bit 27 (0)	bit 27 (0)
RESERVED_31_28		bit 3..28 (0)	
ASYM_DRV_EN			bit 24 (0)
PU_ODT_ONLY			bit 25 (0)
DIS_NON_LIN_COMP			bit 26 (1)
ZCTRL_UPPER			bit 3..28 (0)

Register documentation reference

Register	lan966x	lan969x	sparx5
ADDRMAP0	Address Map Register 0	Address Map Register 0	Address Map Register 0
ADDRMAP1	Address Map Register 1	Address Map Register 1	Address Map Register 1

ADDRMAP2	Address Map Register 2	Address Map Register 2	Address Map Register 2
ADDRMAP3	Address Map Register 3	Address Map Register 3	Address Map Register 3
ADDRMAP4	Address Map Register 4	Address Map Register 4	Address Map Register 4
ADDRMAP5	Address Map Register 5	Address Map Register 5	Address Map Register 5
ADDRMAP6	Address Map Register 6	Address Map Register 6	Address Map Register 6
ADDRMAP7	-	Address Map Register 7	Address Map Register 7
ADDRMAP8	-	Address Map Register 8	Address Map Register 8
CRCPARCTL1	-	CRC Parity Control Register 1	CRC Parity Control Register1
DBICTL	-	DM/DBI Control Register	DM/DBI Control Register
DCR	DRAM Configuration Register	DRAM Configuration Register	DRAM Configuration Register
DFIMISC	DFI Miscellaneous Control Register	DFI Miscellaneous Control Register	DFI Miscellaneous Control Register
DFITMG0	DFI Timing Register 0	DFI Timing Register 0	DFI Timing Register 0
DFITMG1	DFI Timing Register 1	DFI Timing Register 1	DFI Timing Register 1
DFIUPD0	DFI Update Register 0	DFI Update Register 0	DFI Update Register 0
DFIUPD1	DFI Update Register 1	DFI Update Register 1	DFI Update Register 1
DRAMTMG0	SDRAM Timing Register 0	SDRAM Timing Register 0	SDRAM Timing Register 0
DRAMTMG1	SDRAM Timing Register 1	SDRAM Timing Register 1	SDRAM Timing Register 1
DRAMTMG12	-	SDRAM Timing Register 12	SDRAM Timing Register 12

DRAMTMG2	SDRAM Timing Register 2	SDRAM Timing Register 2	SDRAM Timing Register 2
DRAMTMG3	SDRAM Timing Register 3	SDRAM Timing Register 3	SDRAM Timing Register 3
DRAMTMG4	SDRAM Timing Register 4	SDRAM Timing Register 4	SDRAM Timing Register 4
DRAMTMG5	SDRAM Timing Register 5	SDRAM Timing Register 5	SDRAM Timing Register 5
DRAMTMG8	SDRAM Timing Register 8	SDRAM Timing Register 8	SDRAM Timing Register 8
DRAMTMG9	-	SDRAM Timing Register 9	SDRAM Timing Register 9
DSGCR	DDR System General Configuration Register	DDR System General Configuration Register	DDR System General Configuration Register
DTCR	Data Training Configuration Register	-	-
DTCR0	-	Data Training Configuration Register 0	Data Training Configuration Register 0
DTCR1	-	Data Training Configuration Register 1	Data Training Configuration Register 1
DTPR0	DRAM Timing Parameters Register 0	DRAM Timing Parameters Register 0	DRAM Timing Parameters Register 0
DTPR1	DRAM Timing Parameters Register 1	DRAM Timing Parameters Register 1	DRAM Timing Parameters Register 1
DTPR2	DRAM Timing Parameters Register 2	DRAM Timing Parameters Register 2	DRAM Timing Parameters Register 2
DTPR3	-	DRAM Timing Parameters Register 3	DRAM Timing Parameters Register 3
DTPR4	-	DRAM Timing Parameters Register 4	DRAM Timing Parameters Register 4

DTPR5	-	DRAM Timing Parameters Register 5	DRAM Timing Parameters Register 5
DXCCR	DATX8 Common Configuration Register	DATX8 Common Configuration Register	DATX8 Common Configuration Register
ECCCFG0	ECC Configuration Register 0	ECC Configuration Register 0	ECC Configuration Register 0
INIT0	SDRAM Initialization Register 0	SDRAM Initialization Register 0	SDRAM Initialization Register 0
INIT1	SDRAM Initialization Register 1	SDRAM Initialization Register 1	SDRAM Initialization Register 1
INIT3	SDRAM Initialization Register 3	SDRAM Initialization Register 3	SDRAM Initialization Register 3
INIT4	SDRAM Initialization Register 4	SDRAM Initialization Register 4	SDRAM Initialization Register 4
INIT5	SDRAM Initialization Register 5	SDRAM Initialization Register 5	SDRAM Initialization Register 5
INIT6	-	SDRAM Initialization Register 6	SDRAM Initialization Register 6
INIT7	-	SDRAM Initialization Register 7	SDRAM Initialization Register 7
MSTR	Master Register0	Master Register 0	Master Register0
ODTCFG	ODT Configuration Register	ODT Configuration Register	ODT Configuration Register
PCCFG	Port Common Configuration Register	Port Common Configuration Register	Port Common Configuration Register
PGCR2	PHY General Configuration Register 2	PHY General Configuration Register 2	PHY General Configuration Register 2

PTR0	PHY Timing Register 0	PHY Timing Register 0	PHY Timing Register 0
PTR1	PHY Timing Register 1	PHY Timing Register 1	PHY Timing Register 1
PTR2	PHY Timing Register 2	PHY Timing Register 2	PHY Timing Register 2
PTR3	PHY Timing Register 3	PHY Timing Register 3	PHY Timing Register 3
PTR4	PHY Timing Register 4	PHY Timing Register 4	PHY Timing Register 4
PWRCTL	Low Power Control Register	Low Power Control Register	Low Power Control Register
RFSHCTL0	Refresh Control Register 0	Refresh Control Register 0	Refresh Control Register 0
RFSHCTL3	Refresh Control Register 3	Refresh Control Register 3	Refresh Control Register 3
RFSHTMG	Refresh Timing Register	Refresh Timing Register	Refresh Timing Register
SBRCTL	Scrubber Control Register	Scrubber Control Register	Scrubber Control Register
SCHCR1	-	Scheduler Command Register 1	Scheduler Command Register 1
ZQ0CR0	ZQ n Impedance Control Register 0	-	-
ZQ0CR1	ZQ n Impedance Control Register 1	-	-
ZQ0PR	-	ZQ n Impedance Control Program Register	ZQ n Impedance Control Program Register
ZQ1CR0	ZQ n Impedance Control Register 0	-	-
ZQ1CR1	ZQ n Impedance Control Register 1	-	-
ZQ1PR	-	ZQ n Impedance Control Program Register	ZQ n Impedance Control Program Register

ZQ2PR	-	ZQ n Impedance Control Program Register	ZQ n Impedance Control Program Register
ZQCR	-	ZQ Impedance Control Register	ZQ Impedance Control Register

Register fields documentation reference

ADDRMAP0 fields

Field	lan966x	lan969x	sparx5
ADDRMAP_CS_BIT0	Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 29, and 31 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 0 is set to 0. Programming Mode: Static		

ADDRMAP1 fields

Field	lan966x	lan969x	sparx5
ADDRMAP_BANK_B2	Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31, and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Programming Mode: Static		Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31 and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Programming Mode: Static

ADDRMAP_BANK_B1	Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Programming Mode: Static	Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32 and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Programming Mode: Static
ADDRMAP_BANK_B0	Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32, and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Programming Mode: Static	Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Programming Mode: Static

ADDRMAP2 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_COL_B5	- Full bus width mode - Selects the HIF address bit used as column address bit 5 - Half bus width mode - Selects the HIF address bit used as column address bit 6 - Quarter bus width mode - Selects the HIF address bit used as column address bit 7 Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 5. - Half bus width mode: Selects the HIF address bit used as column address bit 6. - Quarter bus width mode: Selects the HIF address bit used as column address bit 7 . Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static
ADDRMAP_COL_B4	- Full bus width mode - Selects the HIF address bit used as column address bit 4 - Half bus width mode - Selects the HIF address bit used as column address bit 5 - Quarter bus width mode - Selects the HIF address bit used as column address bit 6 Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 4. - Half bus width mode: Selects the HIF address bit used as column address bit 5. - Quarter bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

ADDRMAP_COL_B3	- Full bus width mode - Selects the HIF address bit used as column address bit 3 - Half bus width mode - Selects the HIF address bit used as column address bit 4 - Quarter bus width mode - Selects the HIF address bit used as column address bit 5 Valid Range: 0 to 7, x. x indicates a valid value in the inline ECC configuration. Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), if MEMC_BURST_LENGTH is 16, number of column address is 10 and work on half bus width mode, column bit 8, column bit 7 and column bit 3 must map to the highest 3 valid HIF address bits. This register need be set to x. (x = the highest valid HIF address bit - internal base - 2) Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 3. - Half bus width mode: Selects the HIF address bit used as column address bit 4. - Quarter bus width mode: Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7 Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0. Programming Mode: Static

ADDRMAP_COL_B2	- Full bus width mode - Selects the HIF address bit used as column address bit 2 - Half bus width mode - Selects the HIF address bit used as column address bit 3 - Quarter bus width mode - Selects the HIF address bit used as column address bit 4 Valid Range: 0 to 7 Internal Base: 2 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless: - In Half or Quarter bus width (MSTR.data_bus_width!=00) and - PCCFG.bl_exp_mode==1 and either - In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or - In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0 If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless: - In Half or Quarter bus width (MSTR.data_bus_width!=00) and - PCCFG.bl_exp_mode==1 and - In DDR4 and ADDRMAP8.addrmap_bg_b0==0 Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3. Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 2. - Half bus width mode: Selects the HIF address bit used as column address bit 3. - Quarter bus width mode: Selects the HIF address bit used as column address bit 4. Valid Range: 0 to 7 Internal Base: 2 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless: - in Half or Quarter bus width (MSTR.data_bus_width!=00) and - PCCFG.bl_exp_mode==1 and either - In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or - In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0 If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless: - in Half or Quarter bus width (MSTR.data_bus_width!=00) and - PCCFG.bl_exp_mode==1 and - In DDR4 and ADDRMAP8.addrmap_bg_b0==0 Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3. Programming Mode: Static

ADDRMAP3 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_COL_B9	- Full bus width mode - Selects the HIF address bit used as column address bit 9 - Half bus width mode - Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) - Quarter bus width mode - Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set	- Full bus width mode: Selects the HIF address bit used as column address bit 9. - Half bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). - Quarter bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, x, and 31. x indicate a valid value in inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second

	to 31 and then this column address bit is set to 0. Programming Mode: Static	highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) if it is unused, set to 31. Programming Mode: Static

ADDRMAP_COL_B8	- Full bus width mode - Selects the HIF address bit used as column address bit 8 - Half bus width mode - Selects the HIF address bit used as column address bit 9 - Quarter bus width mode - Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 8 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 8. - Half bus width mode: Selects the HIF address bit used as column address bit 9. - Quarter bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, x, and 31. x indicate a valid value in inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 8 is the third highest column address bit, it must map to the third highest valid

		HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) if it is unused, set to 31. Programming Mode: Static
ADDRMAP_COL_B7	- Full bus width mode - Selects the HIF address bit used as column address bit 7 - Half bus width mode - Selects the HIF address bit used as column address bit 8 - Quarter bus width mode - Selects the HIF address bit used as column address bit 9 Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 7. - Half bus width mode: Selects the HIF address bit used as column address bit 8. - Quarter bus width mode: Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, x, and 31. x indicate a valid value in inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) if it is unused, set to 31. Programming Mode: Static

ADDRMAP_COL_B6	- Full bus width mode - Selects the HIF address bit used as column address bit 6. - Half bus width mode - Selects the HIF address bit used as column address bit 7. - Quarter bus width mode - Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, x and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), if MEMC_BURST_LENGTH is 8, number of column address is 10 and work on half bus width mode, column bit 8, column bit 7 and column bit 6 must map to the highest 3 valid HIF address bits. This register need be set to x. (x = the highest valid HIF address bit - internal base - 2) Programming Mode: Static	- Full bus width mode: Selects the HIF address bit used as column address bit 6. - Half bus width mode: Selects the HIF address bit used as column address bit 7. - Quarter bus width mode: Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, and 15 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

ADDRMAP4 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_COL_B11	- Full bus width mode - Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) - Half bus width mode - UNUSED. See later in this description for value you need to set to make it unused - Quarter bus width mode - UNUSED. See later in this description for value you need to set to make it unused Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 11 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 11 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 11 is the third highest column address bit, it must map to	- Full bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). - Half bus width mode: Unused. To make it unused, this should be tied to 4’hF. - Quarter bus width mode: Unused. To make it unused, this must be tied to 4’hF. Valid Range: 0 to 7, x, and 31. x indicate a valid value in inline ECC configuration. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 11 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 11 is the second highest column address bit, it must map to the second

	the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static	highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 11 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) if it is unused, set to 31. Programming Mode: Static

ADDRMAP_COL_B10	- Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) - Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) - Quarter bus width mode: UNUSED. See later in this description for value you need to set to make it unused Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 10 is the third highest column	- Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). - Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). - Quarter bus width mode: UNUSED. To make it unused, this must be tied to 4’hF. Valid Range: 0 to 7, x, and 31. x indicate a valid value in inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and ECC is enabled (ECCCFG0.ecc_mode>0), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest

	address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static	column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 10 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) if it is unused, set to 31. Programming Mode: Static

ADDRMAP5 fields

Field	lan966x	lan969x	sparx5
ADDRMAP_ROW_B11	Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 11, and 15 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 11 is set to 0. Programming Mode: Static		

ADDRMAP_ROW_B2_10	Selects the HIF address bits used as row address bits 2 to 10. Valid Range: 0 to 11, and 15 Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) and so on, increasing to 16 (for row address bit 10) The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When set to 15, the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11. Programming Mode: Static	Selects the HIF address bits used as row address bits 2 to 10. Valid Range: 0 to 11, and 15 Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) etc increasing to 16 (for row address bit 10) The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When value 15 is used the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11. Programming Mode: Static
ADDRMAP_ROW_B1	Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 11 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static	
ADDRMAP_ROW_B0	Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 11 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static	

ADDRMAP6 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_ROW_B15	Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 11, and 15 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 15 is set to 0. Programming Mode: Static	
ADDRMAP_ROW_B14	Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 11, and 15 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 14 is set to 0. Programming Mode: Static	
ADDRMAP_ROW_B13	Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 11, and 15 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 13 is set to 0. Programming Mode: Static	
ADDRMAP_ROW_B12	Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 11, and 15 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 12 is set to 0. Programming Mode: Static	
LPDDR3_6GB_12GB		Set this to 1 if there is an LPDDR3 SDRAM 6Gb or 12Gb device in use. - 1 - LPDDR3 SDRAM 6Gb/12Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid - 0 - non-LPDDR3 6Gb/12Gb device in use. All addresses are valid Present only in designs configured to support LPDDR3. Programming Mode: Static

ADDRMAP7 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_ROW_B16		Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 11, and 15 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 16 is set to 0. Programming Mode: Static	
ADDRMAP_ROW_B17		Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0 for DDR4 or set to 1 for LPDDR4 backward compability. Programming Mode: Static	Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0. Programming Mode: Static

ADDRMAP8 fields

Field	lan966x	lan969x	sparx5

ADDRMAP_BG_B0		Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32, and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Programming Mode: Static	Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Programming Mode: Static
ADDRMAP_BG_B1		Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Programming Mode: Static	

CRCPARCTL1 fields

Field	lan966x	lan969x	sparx5
PARITY_ENABLE		C/A Parity enable register. If RCD’s parity error detection or SDRAM’s parity detection is enabled, this register must be 1. Programming Mode: Static	C/A Parity enable re - 1: Enable generati C/A parity and dete of C/A parity error - Disable generation parity and disable detection of C/A par error If RCD’s parity detection or SDRAM parity detection is enabled, this registe should be 1. Progra Mode: Static

CRC_ENABLE		CRC enable Register. The setting of this register must match the CRC mode register setting in the DRAM. Programming Mode: Quasi-dynamic Group 2	CRC enable Registe Enable generation c - 0: Disable generat CRC The setting of t register should mat CRC mode register in the DRAM. Programming Mode Static
CRC_INC_DM		CRC calculation setting register. Present only in designs configured to support DDR4. Programming Mode: Static	CRC Calculation set register - 1: CRC inc DM signal - 0: CRC includes DM signal Present only in desi configured to suppo DDR4. Programmin Mode: Static
CAPARITY_DISABLE_BEFORE_SR		If DDR4-SDRAM's CA parity is enabled by INIT6.mr5[2:0]!=0 and this register is set to 1, CA parity is automatically disabled before self-refresh entry, and enabled after self-refresh exit by issuing MR5. If Geardown is used by MSTR.geardown_mode=1, this register must be set to 1. If this register set to 0, DRAMTMG5.t_ckesr and DRAMTMG5.t_cksre must be increased by PL(Parity latency). Programming Mode: Static	If DDR4-SDRAM's C parity is enabled by INIT6.mr5[2:0]!=0 a this register is set t CA parity is automa disabled before Self Refresh entry and e after Self-Refresh ex issuing MR5. - 1: CA parity is disabled be Self-Refresh entry - parity is not disable before Self-Refresh If Geardown is used MSTR.geardown_m this register must b to 1. If this register 0, DRAMTMG5.t_ck and DRAMTMG5.t_c must be increased b PL(Parity latency) Programming Mode Static

DBICTL fields

Field	lan966x	lan969x	sparx5

DM_EN		Indicates the DM enable signal in DDRC. This signal must be set the same logical value as DRAM’s mode register. - DDR4 - Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0 - LPDDR4 - Set this to inverted value of MR13[5] which is opposite polarity from this signal Programming Mode: Static	DM enable signal in DDRC. - 0 - DM is disabled. - 1 - DM is enabled. This signal must be set the same logical value as DRAM’s mode register. - DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. - LPDDR4: Set this to inverted value of MR13[5] which is opposite polarity from this signal Programming Mode: Quasi-dynamic Group 3
WR_DBI_EN		Write DBI enable signal in DDRC. This signal must be set the same value as DRAM’s mode register. - DDR4 - MR5 bit A11. When x4 devices are used, this signal must be set to 0 - LPDDR4 - MR3[7] Programming Mode: Quasi-dynamic Group 1	Write DBI enable signal in DDRC. - 0 - Write DBI is disabled. - 1 - Write DBI is enabled. This signal must be set the same value as DRAM’s mode register. - DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. - LPDDR4: MR3[7] Programming Mode: Quasi-dynamic Group 1

RD_DBI_EN		Read DBI enable signal in DDRC. This signal must be set the same value as DRAM’s mode register. - DDR4 - MR5 bit A12. When x4 devices are used, this signal must be set to 0 - LPDDR4 - MR3[6] Programming Mode: Quasi-dynamic Group 1	Read DBI enable signal in DDRC. - 0 - Read DBI is disabled. - 1 - Read DBI is enabled. This signal must be set the same value as DRAM’s mode register. - DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. - LPDDR4: MR3[6] Programming Mode: Quasi-dynamic Group 1

DCR fields

Field	lan966x	lan969x	sparx5

UDIMM	Un-buffered DIMM Address Mirroring: Indicates, if set, that there is address mirroring on the second rank of an un-buffered DIMM (the rank connected to CS#[1]). In this case, the PUB re-scrambles the bank and address when sending mode register commands to the second rank. This only applies to PUB internal SDRAM transactions. Transactions generated by the controller must make its own adjustments when using an un-buffered DIMM. DCR[NOSRA] must be set if address mirroring is enabled.	Un-buffered DIMM Address Mirroring.
DDR2T	DDR 2T Timing: Indicates, if set, that 2T timing should be used by PUB internally generated SDRAM transactions.	DDR 2T Timing.

NOSRA	No Simultaneous Rank Access: Specifies, if set, that simultaneous rank access on the same clock cycle is not allowed. This means that multiple chip select signals should not be asserted at the same time. This may be required on some DIMM systems.	No Simultaneous Rank Access.
BYTEMASK	Byte Mask: Mask applied to all beats of read data on all bytes lanes during read DQS gate training. This allows training to be conducted based on selected bit(s) from the byte lanes. Valid values for each bit are: 0 = Disable compare for that bit 1 = Enable compare for that bit Note that this mask applies in DDR3 MPR operation mode as well and must be in keeping with the PDQ field setting.	Byte Mask.

MPRDQ	Multi-Purpose Register (MPR) DQ (DDR3 Only): Specifies the value that is driven on non-primary DQ pins during MPR reads. Valid values are: 0 = Primary DQ drives out the data from MPR (0-1-0-1); non-primary DQs drive '0' 1 = Primary DQ and non-primary DQs all drive the same data from MPR (0-1-0-1)	Multi-Purpose Register (MPR) DQ.
PDQ	Primary DQ (DDR3 Only): Specifies the DQ pin in a byte that is designated as a primary pin for Multi-Purpose Register (MPR) reads. Valid values are 0 to 7 for DQ[0] to DQ[7], respectively.	Primary DQ.

DDR8BNK	DDR 8-Bank: Indicates, if set, that the SDRAM used has 8 banks. tRPA = tRP+1 and tFAW are used for 8-bank DRAMs, otherwise tRPA = tRP and no tFAW is used. Note that a setting of 1 for DRAMs that have fewer than 8 banks results in correct functionality, but less tight DRAM command spacing for the parameters.	DDR 8-Bank.
DDRMD	DDR Mode: SDRAM DDR mode. Valid values are: 000 = Reserved 001 = Reserved 010 = DDR2 011 = DDR3 100 - 111 = Reserved	DDR Mode.
DDRTYPE		DDR Type.
RESERVED_26_18		Reserved for future use.
UBG		Un-used Bank Group.
RESERVED_31		Reserved for future use.

DFIMISC fields

Field	lan966x	lan969x	sparx5
DFI_FREQUENCY	Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Programming Mode: Quasi-dynamic Group 1		

DFI_INIT_START	PHY init start request signal.When asserted it triggers the PHY init start request. Programming Mode: Quasi-dynamic Group 3	PHY init start request signal. Programming Mode: Quasi-dynamic Group 3	PHY init start request signal.When asserted it triggers the PH init start reques Programming Mode: Quasi-dynamic Group 3
CTL_IDLE_EN	Enables support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. For more information on ctl_idle functionality, see signal description of ctl_idle signal. Programming Mode: Static	Sets support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. For more information on ctl_idle functionality, see signal description of ctl_idle signal. Programming Mode: Static	Enables support of ctl_idle signa which is non-DF related pin specific to certain Synopsy PHYs. See signa description of ctl_idle signal for further details of ctl_idl functionality. Programming Mode: Static
DFI_INIT_COMPLETE_EN	PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation Programming Mode: Quasi-dynamic Group 3	PHY initialization complete enable signal. Programming Mode: Quasi-dynamic Group 3	PHY initialization complete enable signal. When asserted the dfi_init_complet signal can be used to trigger SDRAM initialisation Programming Mode: Quasi-dynamic Group 3

PHY_DBI_MODE		DBI implemented in DDRC or PHY. Present only in designs configured to support DDR4 and LPDDR4. Programming Mode: Static	DBI implemented in DDRC or PHY. - 0 - DDRC implements DBI functionality. - 1 - PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4. Programming Mode: Static
DIS_DYN_ADR_TRI		Sets PHY specific Dynamic Tristating. This functionality works only in DFI 1:2 frequency ratio mode regardless of MSTR.en_2t_timing_mode, so if either of the following condition is met no special IDLE command is issued on the DFI bus: - MEMC_FREQ_RATIO==1 - MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1 The special IDLE command means the following codes with the case where all the dfi_cs is 1: - (phase 0 and 1) dfi_ras_n=1 - (phase 0 and 1) dfi_cas_n= 1 - phase 0 and 1) dfi_we_n= 1 - (phase 0 and 1) dfi_bank [0]= 0 - (phase 0 and 1) dfi_act_n= 1 Programming Mode: Quasi-dynamic Group 3	

DFITMG0 fields

Field	lan966x	lan969x

DFI_T_CTRL_DELAY	Specifies the number of DFI clock cycles after an assertion or deassertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or deassertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/ LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4	Specifies the number of DF clock cycles after an assert or de-assertion of the DFI control signals that the cor signals at the PHY-DRAM interface reflect the assert or de-assertion. If the DFI clock and the memory cloc are not phase-aligned, this timing parameter must be rounded up to the next inte value. Note that if using RDIMM/LRDIMM, it is necessary to increment thi parameter by RDIMM's/ LRDIMM's extra cycle of latency in terms of DFI clo Unit: DFI clock cycles. Programming Mode: Quasi dynamic Group 4
DFI_RDDATA_USE_DFI_PHY_CLK	Defines whether dfi_rddata_en/dfi_rddata/ dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: - 0 in terms of HDR (DFI clock) cycles - 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: - If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 - Else, it must be set to 1 Programming Mode: Static	Defines whether dfi_rddata_en/dfi_rddata/ dfi_rddata_valid is generat using HDR (DFI clock) or S (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en terms of HDR (DFI clock) c SDR (DFI PHY clock) cycle Refer to PHY specification correct value. If using a Synopsys DWC DDR3/2 PH DWC DDR2/3-Lite/mDDR P DWC DDR multiPHY or DW Gen2 DDR multiPHY, this f must be set to 0; otherwise If MEMC_PROG_FREQ_RATI and MSTR.frequency_ratio this field must be set to 0 - Else, it must be set to 1 Programming Mode: Static

DFI_T_RDDATA_EN	Time from the assertion of a read command on the DFI inter to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if u RDIMM/LRDIMM, it may be necessary to use the adjusted va of CL in the calculation of trddata_en. This is to compensate the extra cycles of latency through the RDIMM/LRDIMM. Un DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_rddata_use_dfi_phy_clk. Programming Mode: Quasi-dynamic Group 1, Group 4	
DFI_WRDATA_USE_DFI_PHY_CLK	Defines whether dfi_wrdata_en/dfi_wrdata/ dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. - 0 in terms of HDR (DFI clock) cycles - 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: - If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 - Else, it must be set to 1 Programming Mode: Static	Defines whether dfi_wrdata_en/dfi_wrdata/ dfi_wrdata_mask is genera using HDR (DFI clock) or S (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is terms of HDR (DFI clock) c SDR (DFI PHY clock) cycle Selects whether value in DFITMG0.dfi_tphy_wrdata in terms of HDR (DFI clock SDR (DFI PHY clock) cycle Refer to PHY specification correct value. If using a Synopsys DWC DDR3/2 PH DWC DDR2/3-Lite/mDDR P DWC DDR multiPHY or DW Gen2 DDR multiPHY, this f must be set to 0; otherwise If MEMC_PROG_FREQ_RATI and MSTR.frequency_ratio this field must be set to 0 - Else, it must be set to 1 Programming Mode: Static

DFI_TPHY_WRDATA	Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. For more information on cor value, see PHY specification. Note, maximum supported valu 8. Unit: DFI clock cycles or DFI PHY clock cycles, depending DFITMG0.dfi_wrdata_use_dfi_phy_clk. Programming Mode: Quasi-dynamic Group 4
DFI_TPHY_WRLAT	Write latency. Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the D timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDI LRDIMM, it may be necessary to use the adjusted value of C the calculation of tphy_wrlat. This is to compensate for the e cycles of latency through the RDIMM/LRDIMM. For LPDDR4 dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles o DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Programming Mode: Quasi-dynamic Group 2, Group 4

DFITMG1 fields

Field	lan966x	lan969x	sp
DFI_T_PARIN_LAT	Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 4		Specifies the numb cycles between whe asserted and when dfi_parity_in signal Programming Mode Group 4

DFI_T_WRDATA_DELAY	Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For more information on correct value, see PHY specification. For DFI 3.0 PHY, set to twrdata_delay, a new timing parameter introduced in DFI 3.0. For DFI 2.1 PHY, set to tphy_wrdata + (delay of DFI write data to the DRAM). Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. If using DFITMG0.dfi_wrdata_use_dfi_phy_clk=1, add 1 to the value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4	Specifies the numb between when the is asserted and whe write data transfer DRAM bus. This co timing parameter t to PHY specificatio For DFI 3.0 PHY, se new timing parame 3.0. For DFI 2.1 PH + (delay of DFI wri Value to be progra DFI clocks, not PH FREQ_RATIO=2, di and round up to ne DFITMG0.dfi_wrda add 1 to the value. Programming Mode Group 4
DFI_T_DRAM_CLK_DISABLE	Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4	Specifies the numb from the assertion dfi_dram_clk_disab until the clock to th devices, at the PHY maintains a low val and the memory clo aligned, this timing rounded up to the n Programming Mode Group 4

DFI_T_DRAM_CLK_ENABLE	Specifies the number of DFI clock cycles from the deassertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4	Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4	Specifies the numb from the deassertio dfi_dram_clk_disab until the first valid clock to the DRAM the PHY-DRAM bou clock and the mem phase aligned, this should be rounded value. Programmin dynamic Group 4

DFI_T_CMD_LAT		Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, must be set to '0' or tCAL, which matches the CAL mode register setting in the DRAM. When enabling CAL mode with RDIMM/ LRDIMM, this field must be set to tCAL-CLA (Command Latency Adder). For more information on CLA, see JEDEC DDR4 Register Specification. If the PHY can add the latency for CAL mode, this must be set to '0'. Valid Range: 0 to 8. Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	Specifies the numb cycles between whe asserted and when command is driven. CAL mode, should l value which matche register setting in t can add the latency should be set to '0'. 5, 6, and 8 Program dynamic Group 2 ar

DFIUPD0 fields

Field	lan966x	lan969x
DIS_AUTO_CTRLUPD	When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2. The controller must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd. When '0', uMCTL2 issues dfi_ctrlupd_req periodically. Programming Mode: Quasi-dynamic Group 3	Sets the automatic dfi_ctrlupd_req generation by th uMCTL2. The controller must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd Programming Mode: Quasi-dynamic Group 3

DIS_AUTO_CTRLUPD_SRX	When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2 at self-refresh exit. When '0', uMCTL2 issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. Programming Mode: Static	Sets the automatic dfi_ctrlupd_req generation by th uMCTL2 at self-refresh exit. Programming Mode: Static
CTRLUPD_PRE_SRX	Selects dfi_ctrlupd_req requirements at SRX: - 0 - Send ctrlupd after SRX - 1 - Send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req is issued when SRX. For SNPS DDR32 PHY, keep the default value 0x0. Programming Mode: Static	Selects dfi_ctrlupd_req requirements at SRX. If DFIUPD0.dis_auto_ctrlupd_srx= this register has no impact, because no dfi_ctrlupd_req is issued when SRX. Programming Mode: Static
DFI_T_CTRLUP_MAX	Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Unit: DFI clock cycles. Programming Mode: Static	
DFI_T_CTRLUP_MIN	Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 deasserts dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. Programming Mode: Static	Specifies the minimum number DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. Programming Mode: Static

DFIUPD1 fields

Field	lan966x	lan969x	

DFI_T_CTRLUPD_INTERVAL_MIN_X1024	This is the minimum amount of time between uMCTL2 initiated DFI update requests (which is executed whenever the uMCTL2 is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the uMCTL2 is idle. The minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	This is betwe reque uMCT reduc which latenc uMCT this fi Progr
DFI_T_CTRLUPD_INTERVAL_MAX_X1024	This is the maximum amount of time between uMCTL2 initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	This is betwe reque updat dfi_ctr blocke receiv recali DFI c PHY F errors calibr may i allowe progr DFIUI must DFIUI Unit: Mode

DRAMTMG0 fields

Field	lan966x	lan969x	sparx5

WR2PRE	Specifies the minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies. where: - WL: Write latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present - tWR: Write recovery time. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/ LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. For DDR4, LPDDR4, LPDDR3, using nWR(WR) instead of tWR to calculate the value of this parameter. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	Minimum time between write and precharge to same bank. Unit: Clocks Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies where: - WL = write latency - BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. - tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR2/LPDDR3/ LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the

		LRDIMM. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
T_FAW	tFAW - valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tFAW Valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4

T_RAS_MAX	tRAS(max) - Specifies the maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:1 frequency ratio mode, t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). When the controller is operating in 1:2 frequency ratio mode, t_ras_max must be set to RoundDown((RoundDown(tRAS(max)/tCK/1024)-1)/2). Unit: Multiples of 1024 DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:2 frequency ratio mode, program this to (tRAS(max)-1)/2. No rounding up. Unit: Multiples of 1024 clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
T_RAS_MIN	tRAS(min) - Specifies the minimum time between activate and precharge to the same bank. When the controller is operating in 1:1 frequency ratio mode, t_ras_min must be set to RoundUp(tRASmin/tCK) When the controller is operating in 1:2 frequency ratio mode, 1T mode, t_ras_min must be set to RoundDown(RoundUp(tRASmin/tCK)/2) When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, t_ras min must be set to RoundUp(RoundUp(tRASmin/tCK)/2) Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tRAS(min): Minimum time between activate and precharge to the same bank. When the controller is operating in 1:2 frequency mode, 1T mode, program this to tRAS(min)/2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, program this to (tRAS(min)/2) and round it up to the next integer value. Unit: Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4

DRAMTMG1 fields

Field	lan966x	lan969x	sparx5

T_XP	tXP - Specifies the minimum time after power-down exit to any operation. For DDR3, this must be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tXP: Minimum time after power-down exit to any operation. For DDR3, this should be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4

RD2PRE	tRTP - Specifies the minimum time from read to precharge of same bank. - DDR2 - tAL + BL/2 + max(RoundUp(tRTP/tCK), 2) - 2 - DDR3 - tAL + max (RoundUp(tRTP/tCK), 4) - DDR4 - Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (**). - mDDR - BL/2 - LPDDR2 - Depends on if it is LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + RoundUp(tRTP/tCK) - 1. LPDDR2-S4: BL/2 + max(RoundUp(tRTP/tCK),2) - 2. - LPDDR3 - BL/2 + max(RoundUp(tRTP/tCK),4) - 4 - LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 ()** When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. For DDR4, using RTP instead of tRTP to calculate the value of this parameter. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	tRTP: Minimum time from read to precharge of same bank. - DDR2: tAL + BL/2 + max(tRTP, 2) - 2 - DDR3: tAL + max (tRTP, 4) - DDR4: Max of following two equations: tAL + max (tRTP, 4) or, RL + BL/2 - tRP (**). - mDDR: BL/2 - LPDDR2: Depends on if it's LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + tRTP - 1. LPDDR2-S4: BL/2 + max(tRTP,2) - 2. - LPDDR3: BL/2 + max(tRTP,4) - 4 - LPDDR4: BL/2 + max(tRTP,8) - 8 ()** When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Unit: Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

T_RC	tRC - Specifies the minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tRC: Minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DRAMTMG12 fields

Field	lan966x	lan969x	sparx5
T_MRD_PDA		tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_WR_MPR		This bit is used only in DDR4. Cycles between MPR Write and other command. Set this to tMOD + AL (or tMOD + PL + AL if C/A parity is also used). When the controller is operating in 1:2 frequency ratio mode, program this to (tWR_MPR/2) and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	

DRAMTMG2 fields

Field	lan966x	lan969x	

RD2WR	Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. See the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) + 1 Where: - WL: Write latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - RL: Read latency = CAS latency - WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 - RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that,	Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RD(tODTon(min)/tCK) + 1 Where: - WL: Write latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - RL: Read latency = CAS latency - WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 - RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that,	DDR2/3/m - WL DDR WR_PREA LPDDR3: RU(tDQSC LPDDR4(D RL + BL/2 tCK) + WR RD_POSTA LPDDR4(D RL + BL/2 tCK) + RD ODTLon - RU(tODTo Minimum command Include tir turnaroun per-rank, constraint PHY datab what shou Unit: Cloc write later length. Th value prog bit of the SDRAM - CAS laten = write pr unique to RD_POSTA postamble LPDDR4. LPDDR3/L is enabled (DERATEE derated tD used. Whe operating ratio mode calculated equation b to next int depending LRDIMM, to adjust t parameter the extra c through th Programm dynamic C and Group

	depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	

WR2RD	In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. See the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: - CWL: CAS write latency - WL: Write latency - PL: Parity latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification - tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/ LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: - CWL: CAS write latency - WL: Write latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification - tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/ LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	DDR4: CW tWTR_L L BL/2 + tW + BL/2 + minimum command same bank minimum command Includes t turnaroun and all pe global con Clocks. W write later latency - F BL = burs match the in the BL register to tWTR_L = read comm bank grou directly fr specificati internal w command directly fr specificati cycle for L LPDDR4 o controller mode, divi calculated equation b to next int Mode: Qua and Group

READ_LATENCY		Set this field to RL. Indicates the time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/ LRDIMM, it might be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	Set to RL command SDRAM in be set to F depending RDIMM/L necessary of RL to co extra cycl the RDIMI the contro 1:2 freque divide the using the and round This regis required f (except if set), as th latencies c and DFITM for those p Programm dynamic G and Group

WRITE_LATENCY		Set this field to WL. Indicates the Time from write command to write data on SDRAM interface. This must be set to WL. For mDDR, it must be set to 1. Note that, depending on the PHY, if using RDIMM/ LRDIMM, it might be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	Set to WL command SDRAM in be set to W should nor Note that, PHY, if usi LRDIMM, to adjust t compensa of latency LRDIMM. is operatin ratio mode calculated equation b to next int field is not and DDR3 MEMC_TR the DFI re latencies c and DFITM for those p Programm dynamic G and Group

DRAMTMG3 fields

Field	lan966x	lan969x	sparx5

T_MRD	tMRD- Indicates the number of cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: - DDR2/ mDDR: Time from MRS to any command - DDR3/4: Time from MRS to MRS command - LPDDR2: not used - LPDDR3/4: Time from MRS to non-MRS command When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tMRD: Cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_MOD	tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/ LRDIMM chip. Also note that if using RDIMM or LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/ LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tMOD: Parameter used only in DDR3 and DDR4. Cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If MPR writes for DDR4 are used, set to tMOD + AL (or tMPD_PAR + AL if C/A parity is also used). Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_MRW		Time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the above values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Programming Mode: Quasi-dynamic Group 2 and Group 4

DRAMTMG4 fields

Field	lan966x	lan969x	sparx5

T_RCD	tRCD - tAL: Indicates the minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	tRCD - tAL: Minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
T_CCD	DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
T_RRD	DDR4: tRRD_L: This is the minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	DDR4: tRRD_L: Minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_RP	tRP: Indicates the minimum time from single-bank precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp must be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp must be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp must be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tRP: Minimum time from precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp should be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp should be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp should be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DRAMTMG5 fields

Field	lan966x	lan969x	sparx5
T_CKSRX	This is the time before self-refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: - mDDR - 1 - LPDDR2 - 2 - LPDDR3 - 2 - LPDDR4 - tCKCKEH - DDR2 - 1 - DDR3 - tCKSRX - DDR4 - tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4		This is the time before Self Refresh Exit CK is maintained as a valid clock before issuing SRX. Specifies the clock stable t before SRX. Recommended settings: - mDDR: 1 - LPDDR2: 2 - LPDDR3: 2 - LPDDR4: tCKCKEH - DDR2: 1 - DDR3: tCKSRX - DDR4: tCKSRX When the controller is operating in 1:2 frequency mode, program this to recommended va divided by two and round it up to next integer. Programming Mode: Quasi-dyna Group 2 and Group 4

T_CKSRE	This is the time after self-refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: - mDDR - 0 - LPDDR2 - 2 - LPDDR3 - 2 - LPDDR4 - tCKELCK - DDR2 - 1 - DDR3 - Max (10 ns, 5 tCK) - DDR4(No RDIMM) - Max (10 ns, 5 tCK) (+ PL(parity latency)**)) - DDR4(RDIMM) - Max (Max (10 ns, 5 tCK) (+ PL(parity latency)(**)), tCKOff) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	This is the time after Self Refresh Down Entry that CK is maintained as a valid c Specifies the clock disable delay after S Recommended settings: - mDDR: 0 - LPDDR2: 2 - LPDDR3: 2 - LPDDR4: tCKELCK - DDR2: 1 - DDR3: max (10 ns tCK) - DDR4: max (10 ns, 5 tCK) (+ PL(parity latency)**)) ()**Only if CRCPARCTL1.caparity_disable_before_s this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programmin Mode: Quasi-dynamic Group 2 and Grou
T_CKESR	Indicates the minimum CKE low width for self-refresh or self-refresh power down entry to exit timing in memory clock cycles. Recommended settings: - mDDR - tRFC - LPDDR2 - tCKESR - LPDDR3 - tCKESR - LPDDR4 - max(tCKE, tSR) - DDR2 - tCKE - DDR3 - tCKE + 1 - DDR4(No RDIMM) - tCKE + 1 (+ PL(parity latency)**)) - DDR4(RDIMM) - t_cksre + tCKEV ()**Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	Minimum CKE low width for Self refresh Self refresh power down entry to exit ti in memory clock cycles. Recommended settings: - mDDR: tRFC - LPDDR2: tCKE LPDDR3: tCKESR - LPDDR4: max(tCKE tSR) - DDR2: tCKE - DDR3: tCKE + 1 - DDR4: tCKE + 1 (+ PL(parity latency)() ()**Only if CRCPARCTL1.caparity_disable_before_s this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programmin Mode: Quasi-dynamic Group 2 and Grou
T_CKE	Indicates the minimum number of cycles of CKE HIGH/LOW during power-down and self-refresh. - LPDDR2/LPDDR3 mode - Set this to the larger of tCKE or tCKESR - LPDDR4 mode - Set this to the larger of tCKE or tSR - Non-LPDDR2/non-LPDDR3/ non-LPDDR4 designs - Set this to tCKE value When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	Minimum number of cycles of CKE HIG LOW during power-down and self refres LPDDR2/LPDDR3 mode: Set this to the larger of tCKE or tCKESR - LPDDR4 mo Set this to the larger of tCKE or tSR. - N LPDDR2/non-LPDDR3/non-LPDDR4 des Set this to tCKE value. When the contro is operating in 1:2 frequency ratio mode program this to (value described above) and round it up to the next integer valu Unit: Clocks. Programming Mode: Quas dynamic Group 2 and Group 4

DRAMTMG8 fields

Field	lan966x	lan969x	sparx5
T_XS_DLL_X32	tXSDLL: Exit self-refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Quasi-dynamic Group 2, Group 4		tXSDLL: Exit Self Refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4
T_XS_X32	tXS: Exit self-refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Quasi-dynamic Group 2, Group 4		tXS: Exit Self Refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_XS_ABORT_X32		tXS_ABORT: Exit self-refresh to commands not requiring a locked DLL in self-refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Quasi-dynamic Group 2, Group 4	tXS_ABORT: Exit Self Refresh to commands not requiring a locked DLL in Self Refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 clocks. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4

T_XS_FAST_X32		tXS_FAST: Exit self-refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Quasi-dynamic Group 2, Group 4	tXS_FAST: Exit Self Refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 clocks. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4

DRAMTMG9 fields

Field	lan966x	lan969x	sparx5

WR2RD_S		Minimum time from write command to read command for different bank group. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/ system requirements mentioned above: CWL + BL/2 + tWTR_S Where: - CWL: CAS write latency - BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - tWTR_S: Internal write to read command delay for different bank group. This comes directly from the SDRAM specification WTR_S must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles.	CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Present only in designs configured to support DDR4. Unit: Clocks. Where: - CWL = CAS write latency - PL = Parity latency - BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM - tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

		Programming Mode: Quasi-dynamic Group 1, Group 2, Group 4	
T_RRD_S		tRRD_S: This is the minimum time between activates from bank "a" to bank "b" for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
T_CCD_S		tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 2, Group 4	tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
DDR4_WR_PREAMBLE		DDR4 Write preamble mode. Present only with MEMC_FREQ_RATIO=2. Programming Mode: Quasi-dynamic Group 2, Group 4	DDR4 Write preamble mode - 0: 1tCK preamble - 1: 2tCK preamble Present only with MEMC_FREQ_RATIO=2 Programming Mode: Quasi-dynamic Group 2 and Group 4

DSGCR fields

Field	lan966x	lan969x	sparx5
CKEOE	SDRAM CKE Output Enable: Enables, when set, the output driver on the I/O for SDRAM CKE pins.		
RSTOE	SDRAM Reset Output Enable: Enables, when set, the output driver on the I/O for SDRAM RST# pin.	SDRAM Reset Output Enable.	
ODTOE	SDRAM ODT Output Enable: Enables, when set, the output driver on the I/O for SDRAM ODT pins.		
CKOE	SDRAM CK Output Enable: Enables, when set, the output driver on the I/O for SDRAM CK/ CK# pins.		
ODTPDD	ODT Power Down Driver: Powers down, when set, the output driver on the I/O for ODT[3:0] pins. ODTPDD[0] controls the power down for ODT[0], ODTPDD[1] controls the power down for ODT[1], and so on.		

CKEPDD	CKE Power Down Driver: Powers down, when set, the output driver on the I/O for CKE[3:0] pins. CKEPDD[0] controls the power down for CKE[0], CKEPDD[1] controls the power down for CKE[1], and so on.	
SDRMODE	Single Data Rate Mode: Indicates, if set, that the external controller is configured to run in single data rate (SDR) mode. Otherwise if not set the controller is running in half data rate (HDR) mode. This bit not supported in the current version of the PUB.	Single Data Rate Mode.
RRMODE	Rise-to-Rise Mode: Indicates, if set, that the PHY mission mode is configured to run in rise-to-rise mode. Otherwise if not set the PHY mission mode is running in rise-to-fall mode.	
ATOAE	ATO Analog Test Enable.	
DTOOE	DTO Output Enable: Enables, when set, the output driver on the I/O for DTO pins.	DTO Output Enable.

DTOIOM	DTO I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DTO pins.	DTO I/O Mode.
DTOPDR	DTO Power Down Receiver: Powers down, when set, the input receiver on the I/O for DTO pins.	DTO Power Down Receiver.
DTOPDD	DTO Power Down Driver: Powers down, when set, the output driver on the I/O for DTO pins.	
DTOODT	DTO On-Die Termination: Enables, when set, the on-die termination on the I/O for DTO pins.	DTO On-Die Termination.
PUAD	PHY Update Acknowledge Delay: Specifies the number of clock cycles that the indication for the completion of PHY update from the PHY to the controller should be delayed. This essentially delays, by this many clock cycles, the deassertion of dfi_ctrlup_ack and dfi_phyupd_req signals relative to the time when the delay lines or I/Os are updated.	PHY Update Acknowledge Delay.

BRRMODE	Bypass Rise-to-Rise Mode: Indicates, if set, that the PHY bypass mode is configured to run in rise-to-rise mode. Otherwise if not set the PHY bypass mode is running in rise-to-fall mode.	
DQSGX	DQS Gate Extension: Specifies, if set, that the DQS gating must be extended by two DRAM clock cycles and then re-centered, i.e. one clock cycle extension on either side.	DQS Gate Extension.
CUAEN	Controller Update Acknowledge Enable: Specifies, if set, that the PHY should issue controller update acknowledge when the DFI controller update request is asserted. By default the PHY does not acknowledge controller initiated update requests but simply does an update whenever there is a controller update request. This speeds up the update.	Controller Update Acknowledge Enable.

LPPLLPD	Low Power PLL Power Down: Specifies, if set, that the PHY should respond to the DFI low power opportunity request and power down the PLL of the byte if the wakeup time request satisfies the PLL lock time.	Low Power PLL Power Down.
LPIOPD	Low Power I/O Power Down: Specifies, if set, that the PHY should respond to the DFI low power opportunity request and power down the I/Os of the byte.	Low Power I/O Power Down.

ZUEN	Impedance Update Enable: Specifies, if set, that in addition to DDL VT update, the PHY could also perform impedance calibration (update). Refer to the "Impedance Control Register 0-1 (ZQnCR0-1)" bit fields DFICU0, DFICU1 and DFICCU bits to control if an impedance calibration is performed (update) with a DFI controller update request. Refer to the "Impedance Control Register 0-1 (ZQnCR0-1)" bit fields DFIPU0 and DFIPU1 bits to control if an impedance calibration is performed (update) with a DFI PHY update request.	
BDISEN	Byte Disable Enable: Specifies, if set, that the PHY should respond to DFI byte disable request. Otherwise the byte disable from the DFI is ignored in which case bytes can only be disabled using the DXnGCR register.	Byte Disable Enable.

PUREN	PHY Update Request Enable: Specifies if set, that the PHY should issue PHYinitiated update request when there is DDL VT drift.	PHY Update Request Enable.	
CTLZUEN		Controller Impedance Update Enable.	
RESERVED_13		Reserved for future use.	
WRRMODE		Write Path Rise-to-Rise Mode.	
RRRMODE		Read Path Rise-to-Rise Mode.	
PHYZUEN		PHY Impedance Update Enable.	
LPACIOPD		Low Power AC I/O Power Down.	
RESERVED_31_25		Reserved for future use.	
RESERVED_31_24			Reserved for future use.

DTCR fields

Field	lan966x	lan969x	sparx5
RFSHDT	Refresh During Training: A non-zero value specifies that a burst of refreshes equal to the number specified in this field should be sent to the SDRAM after training each rank except the last rank.		

RANKEN	Rank Enable: Specifies the ranks that are enabled for data-training. Bit 0 controls rank 0, bit 1 controls rank 1, bit 2 controls rank 2, and bit 3 controls rank 3. Setting the bit to '1' enables the rank, and setting it to '0' disables the rank.	
DTEXD	Data Training Extended Write DQS: Enables, if set, an extended write DQS whereby two additional pulses of DQS are added as post-amble to a burst of writes. Generally this should only be enabled when running read bit deskew with the intention of performing read eye deskew prior to running write leveling adjustment.	

DTDSTP	Data Training Debug Step: A write of 1 to this bit steps the data training algorithm through a single step. This bit is used to initiate one step of the data training algorithm in question. This bit is self-clearing. To trigger the next step, this bit must be written to again. Note: The training steps must be repeated in order to get new data in the "Data Training Eye Data Register 0-1 (DTEDR0-1)" For example, to see the training results for a different lane, select that lane and repeat the training steps to populate DTEDR0 and DTEDR1 with the correct data.	
DTDEN	Data Training Debug Enable: Enables, if set, the data training single step debug mode.	
DTDBS	Data Training Debug Byte Select: Selects the byte during data training single step debug mode. Note: DTDEN is not used to enable this feature.	

DTWDQMO	Data Training WDQ Margin Override: If set, the Training WDQ Margin value specified in DTCR[11:8] (DTWDQM) is used during data training. Otherwise the value is computed as ¼ of the ddr_clk period measurement found during calibration of the WDQ LCDL.	
DTBDC	Data Training Bit Deskew Centering: Enables, if set, eye centering capability during write and read bit deskew training.	
DTWBDDM	Data Training Write Bit Deskew Data Mask, if set, it enables write bit deskew of the data mask.	
DTWDQM	Training WDQ Margin: Defines how close to 0 or how close to 2*(wdq calibration_value) the WDQ LCDL can be moved during training. Basically defines how much timing margin.	
DTCMPD	Read Data Training Compare Data: Specifies, if set, that DQS gate training should also check if the returning read data is correct. Otherwise data-training only checks if the correct number of DQS edges were returned.	

DTMPR	Read Data Training Using MPR (DDR3 Only): Specifies, if set, that DQS gate training should use the SDRAM Multi-Purpose Register (MPR) register. Otherwise data-training is performed by first writing to some locations in the SDRAM and then reading them back.	
DTRANK	Data Training Rank: Select the SDRAM rank to be used during Read DQS gate training, Read/Write Data Bit Deskew, Read/Write Eye Training.	
DTRPTN	Data Training Repeat Number: Repeat number used to confirm stability of DDR write or read. Note: The minimum value should be 0x4	

DTCR0 fields

Field	lan966x	lan969x	sparx5
DTRPTN		Data Training Repeat Number.	
RESERVED_5_4		Reserved for future use.	
DTMPR		Data Training Using MPR.	
DTCMPD		Data Training Compare Data.	
RESERVED_10_8		Reserved for future use.	
DTDBS4		Data Training Debug Byte Select Most Significant Bit.	
DTWBDDM		Data Training Write Bit Deskew Data Mask.	

DTBDC		Data Training Bit Deskew Centering.	
DTRDBITR		Data Training read DBI deskewing configuration.	
DTDBS		Data Training Debug Byte Select.	
DTDEN		Data Training Debug Enable.	
DTDSTP		Data Training Debug Step.	
DTEXD		Data Training Extended Write DQS.	
RESERVED_23		Reserved for future use.	
DTDRS		Data Training Debug Rank Select.	
RESERVED_27_26		Reserved for future use.	
RFSHDT		Refresh During Training and BIST.	
DTEXG			Data Training with Early/ Extended Gate.

DTCR1 fields

Field	lan966x	lan969x	sparx5
BSTEN		Basic Gate Training Enable.	
RDLVLEN		Read Leveling Enable.	
RDPRMBL_TRN		Read Preamble Training Enable.	
RESERVED_3		Reserved for future use.	
RDLVLGS		Read Leveling Gate Shift.	
RESERVED_7		Reserved for future use.	
RDLVLGDIFF		Read Leveling Gate Sampling Difference.	
WLVLDPRD		Write Leveling Validation Period.	
DTRANK		Data Training Rank.	
RESERVED_15_14		Reserved for future use.	
RANKEN		Rank Enable.	

RANKEN_RSVD		Rank Enable Reserved	
RESERVED_11			Reserved for future use.

DTPR0 fields

Field	lan966x	lan969x	sparx5
TRC	Activate to activate command delay (same bank). Valid values are 2 to 63.		
TRRD	Activate to activate command delay (different banks). Valid values are 1 to 15.	Activate to activate command delay (different banks).	
TRAS	Activate to precharge command delay. Valid values are 2 to 63.	Activate to precharge command delay.	
TRCD	Activate to read or write delay. Minimum time from when an activate command is issued to when a read or write to the activated row can be issued. Valid values are 2 to 15.		

TRP	Precharge command period: The minimum time between a precharge command and any other command. Note that the Controller automatically derives tRPA for 8- bank DDR2 devices by adding 1 to tRP. Valid values are 2 to 15.	Precharge command period.
TWTR	Internal write to read command delay. Valid values are 1 to 15.	
TRTP	Internal read to precharge command delay. Valid values are 2 to 15.	Internal read to precharge command delay.
RESERVED_7_4		Reserved for future use.
RESERVED_15		Reserved for future use.
RESERVED_23		Reserved for future use.
RESERVED_31_30		Reserved for future use.

DTPR1 fields

Field	lan966x	lan969x	sparx5

TAON_OFF_D	ODT turn-on/turn-off delays (DDR2 only). The delays are in clock cycles. Valid values are: 00 = 2/2.5 01 = 3/3.5 10 = 4/4.5 11 = 5/5.5 Most DDR2 devices utilize a fixed value of 2/2.5. For non-standard SDRAMs, the user must ensure that the operational Write Latency is always greater than or equal to the ODT turn-on delay. For example, a DDR2 SDRAM with CAS latency set to 3 and CAS additive latency set to 0 has a Write Latency of 2. Thus 2/2.5 can be used, but not 3/3.5 or higher.	
TWLO	Write leveling output delay: Number of clock cycles from when write leveling DQS is driven high by the control block to when the results from the SDRAM on DQ is sampled by the control block. This must include the SDRAM tWLO timing parameter plus the round trip delay from control block to SDRAM back to control block.	

TWLMRD	Minimum delay from when write leveling mode is programmed to the first DQS/ DQS# rising edge.	Minimum delay from when write leveling mode is programmed to the first DQS/DQS# rising edge..
TRFC	Refresh-to-Refresh: Indicates the minimum time, in clock cycles, between two refresh commands or between a refresh and an active command. This is derived from the minimum refresh interval from the datasheet, tRFC(min), divided by the clock cycle time. The default number of clock cycles is for the largest JEDEC tRFC(min parameter value supported.	
TFAW	4-bank activate period. No more than 4-bank activate commands may be issued in a given tFAW period. Only applies to 8-bank devices. Valid values are 2 to 63.	4-bank activate period.

TMOD	Load mode update delay (DDR3 only). The minimum time between a load mode register command and a non-load mode register command. Valid values are: 000 = 12 001 = 13 010 = 14 011 = 15 100 = 16 101 = 17 110 - 111 = Reserved.	Load mode update delay.
TMRD	Load mode cycle time: The minimum time between a load mode register command and any other command. For DDR3 this is the minimum time between two load mode register commands. Valid values for DDR2 are 2 to 3. For DDR3, the value used for tMRD is 4 plus the value programmed in these bits, i.e. tMRD value for DDR3 ranges from 4 to 7.	Load mode cycle time.
RESERVED_7_5		Reserved for future use.
RESERVED_15_11		Reserved for future use.
RESERVED_31_30		Reserved for future use.

DTPR2 fields

Field	lan966x	lan969x	sparx5

TCCD	Read to read and write to write command delay. Valid values are: 0 = BL/2 for DDR2 and 4 for DDR3 1 = BL/2 + 1 for DDR2 and 5 for DDR3	
TRTW	Read to Write command delay. Valid values are: 0 = standard bus turn around delay 1 = add 1 clock to standard bus turn around delay This parameter allows the user to increase the delay between issuing Write commands to the SDRAM when preceded by Read commands. This provides an option to increase bus turn-around margin for high frequency systems.	Read to Write command delay.

TRTODT	Read to ODT delay (DDR3 only). Specifies whether ODT can be enabled immediately after the read post-amble or one clock delay has to be added. Valid values are: 0 = ODT may be turned on immediately after read post-amble 1 = ODT may not be turned on until one clock after the read post-amble If tRTODT is set to 1, then the read-to-write latency is increased by 1 if ODT is enabled.	Read to ODT delay.
TDLLK	DLL locking time. Valid values are 2 to 1023.	
TCKE	CKE minimum pulse width. Also specifies the minimum time that the SDRAM must remain in power down or self refresh mode. For DDR3 this parameter must be set to the value of tCKESR which is usually bigger than the value of tCKE. Valid values are 2 to 15.	CKE minimum pulse width.

TXP	Power down exit delay. The minimum time between a power down exit command and any other command. This parameter must be set to the maximum of the various minimum power down exit delay parameters specified in the SDRAM datasheet, i.e. max(tXP, tXARD, tXARDS) for DDR2 and max(tXP, tXPDLL) for DDR3. Valid values are 2 to 31.	
TXS	Self refresh exit delay. The minimum time between a self refresh exit command and any other command. This parameter must be set to the maximum of the various minimum self refresh exit delay parameters specified in the SDRAM datasheet, i.e. max(tXSNR, tXSRD) for DDR2 and max(tXS, tXSDLL) for DDR3. Valid values are 2 to 1023.	Self refresh exit delay.
RESERVED_15_10		Reserved for future use.
RESERVED_23_20		Reserved for future use.
RESERVED_27_25		Reserved for future use.
RESERVED_31_29		Reserved for future use.

DTPR3 fields

Field	lan966x	lan969x	sparx5
TDQSCK		DQS output access time from CK/CK#.	
RESERVED_7_3		Reserved for future use.	
TDQSCKMAX		Maximum DQS output access time from CK/CK#.	
RESERVED_15_11		Reserved for future use.	
TDLLK		DLL locking time.	
TCCD		Read to read and write to write command delay.	
TOFDX		ODT turn-off delay extension.	

DTPR4 fields

Field	lan966x	lan969x	sparx5
TXP		Power down exit delay.	
RESERVED_7_5		Reserved for future use.	
TWLO		Write leveling output delay.	
RESERVED_15_12		Reserved for future use.	
TRFC		Refresh-to-Refresh.	
RESERVED_27_26		Reserved for future use.	
TAOND_TAOFD		ODT turn-on/turn-off delays.	
RESERVED_31_30		Reserved for future use.	

DTPR5 fields

Field	lan966x	lan969x	sparx5
TWTR		Internal write to read command delay.	
RESERVED_7_5		Reserved for future use.	
TRCD		Activate to read or write delay.	
RESERVED_15		Reserved for future use.	

TRC		Activate to activate command delay (same bank).
RESERVED_31_24		Reserved for future use.

DXCCR fields

Field	lan966x	lan969x	sparx5
DDPDRCDO	Dynamic Data Power Down Receiver Count Down Offset: Offset applied in calculating window of time where receiver is powered up		
DDPDDCDO	Dynamic Data Power Down Driver Count Down Offset: Offset applied in calculating window of time where driver is powered up		

DYNDXPDR	Data Power Down Receiver: Dynamically powers down, when set, the input receiver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDR and DXnGCR.DXPDR are not set to 1. Receiver is powered-up on a DFI READ command and powered-down (trddata_en + fixed_read_latency + n) HDR cycles after the last DFI READ command. Note that n is defined by the register bit field DXCCR[31:28] (DDPDRCDO).	

DYNDXPDD	Dynamic Data Power Down Driver: Dynamically powers down, when set, the output driver on I/O for the DQ pins of the active DATX8 macros. Applies only when DXPDD and DXnGCR.DXPDD are not set to 1. Driver is powered-up on a DFI WRITE command and powered-down (twrlat + WL/2 + n) HDR cycles after the last DFI WRITE command. Note that n is defined by the register bit field DXCCR[27:24] (DDPDDCDO).	
UDQIOM	Unused DQ I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for unused DQ pins.	Unused DQ I/O Mode.
UDQPDR	Unused DQ Power Down Receiver: Powers down, when set, the input receiver on the I/O for unused DQ pins.	
UDQPDD	Unused DQ Power Down Driver: Powers down, when set, the output driver on the I/O for unused DQ pins.	

UDQODT	Unused DQ On-Die Termination: Enables, when set, the on-die termination on the I/O for unused DQ pins.	
MSBUDQ	Most Significant Byte Unused DQs: Specifies the number of DQ bits that are not used in the most significant byte. The used (valid) bits for this byte are [8-MSBDQ-1:0]. To disable the whole byte, use the DXnGCR.DXEN register.	Most Significant Byte Unused DQs.
DQSNRES	DQS Resistor: Selects the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value. Refer PHY databook for pull-down/pull-up resistor values (RA_SEL/RB_SEL) for DQS/DQS_b.	DQS# Resistor.

DQSRES	DQS Resistor: Selects the on-die pull-down/pull-up resistor for DQS pins. DQSRES[3] selects pull-down (when set to 0) or pull-up (when set to 1). DQSRES[2:0] selects the resistor value. Refer PHY databook for pull-down/pull-up resistor values (RA_SEL/RB_SEL) for DQS/DQS_b.	DQS Resistor.
DXPDR	Data Power Down Receiver: Powers down, when set, the input receiver on I/O for DQ, DM, and DQS/ DQS# pins of all DATX8 macros. This bit is ORed with the PDR configuration bit of the individual DATX8.	
DXPDD	Data Power Down Driver: Powers down, when set, the output driver on I/O for DQ, DM, and DQS/ DQS# pins of all DATX8 macros. This bit is ORed with the PDD configuration bit of the individual DATX8.	

MDLEN	Master Delay Line Enable: Enables, if set, all DATX8 master delay line calibration to perform subsequent period measurements following the initial period measurements that are performed after reset or on when calibration is manually triggered. These additional measurements are accumulated and filtered as long as this bit remains high. This bit is ANDed with the MDLEN bit in the individual DATX8.	Master Delay Line Enable.
DXIOM	Data I/O Mode: Selects SSTL mode (when set to 0) or CMOS mode (when set to 1) of the I/O for DQ, DM, and DQS/ DQS# pins of all DATX8 macros. This bit is ORed with the IOM configuration bit of the individual DATX8.	Data I/O Mode.

DXODT	Data On-Die Termination: Enables, when set, the on-die termination on the I/O for DQ, DM, and DQS/ DQS# pins of all DATX8 macros. This bit is ORed with the ODT configuration bit of the individual DATX8 ("DATX8 General Configuration Register (DXnGCR)"	Data On-Die Termination.	
DQSGLB		Read DQS Gate I/O Loopback.	
DXSR		Data Slew Rate.	
RESERVED_19_18		Reserved for future use.	
QSCNTENCTL		QS Counter Enable Control.	
QSCNTEN		QS Counter Enable.	
DXDCCBYP		DATX8 Duty Cycle Correction Bypass.	
RESERVED_28_24		Reserved for future use.	
RKLOOP		Rank looping (per-rank eye centering) enable.	
X4DQSMD		X4 DQS Mode.	
X4MODE		X4 SDRAM Mode.	
RESERVED_20_18			Reserved for future use.

ECCCFG0 fields

Field	lan966x	lan969

ECC_REGION_MAP_GRANU	Indicates granularity of selectable protected region. Define one region size for ECCCFG0.ecc_region_map. - 0 - 1/8 of memory spaces - 1 - 1/16 of memory spaces - 2 - 1/32 of memory spaces - 3 - 1/64 of memory spaces Programming Mode: Static	Indicates granularity protected region. Def size for ECCCFG0.ecc Programming Mode:
ECC_REGION_MAP_OTHER	When ECCCFG0.ecc_region_map_granu>0, there is a region which is not controlled by ecc_region_map. This register defines the region to be protected or non-protected for Inline ECC. - 0 - Non-Protected - 1 - Protected This register is valid only when ECCCFG0.ecc_region_map_granu>0 && ECCCFG0.ecc_mode=4. Programming Mode: Static	When ECCCFG0.ecc_region there is a region whic controlled by ecc_reg register defines the re protected or non-prot ECC. This register is ECCCFG0.ecc_region && ECCCFG0.ecc_m Programming Mode:
ECC_AP_ERR_THRESHOLD	Sets threshold for address parity error. ECCAPSTAT.ecc_ap_e number of ECC errors (correctable/uncorrectable) within one this threshold. This register value must be less than "Total nu checks within one burst" when this feature is used, "Total nur check within one burst" is calculated by (DRAM Data width) x 64. Programming Mode: Static	
BLK_CHANNEL_IDLE_TIME_X32	Indicates the number of cycles on HIF interface with no acces regions which causes flush of all the block channels. In order channel, uMCTL2 injects write ECC command (when there is HIF command) if there is any write in the block and then stop block address. - 0 - Indicates no timeout (feature is disabled, with this version) - 1 - Indicates 32 cycles - 2 - Indicates 2*32 on Unit: Multiples of 32 DFI clock cycles. For more informatio program this register field, see "Note 1" in the "Notes on Tim section. Programming Mode: Quasi-dynamic Group 3	
ECC_REGION_MAP	Selectable Protected Region setting. Memory space is divided regions which is determined by ECCCFG0.ecc_region_map_g Highest 1/8 memory space is always ECC region. Lowest 7 re Selectable Protected Regions. The Selectable Protected Regio protected/non-protected selectively by ECCCFG0.ecc_region_ Other upper regions are non-protected region if any. Each bit ECCCFG0.ecc_region_map[6:0] correspond to each of lowest respectively. In order to protect a region with ECC, set the co to 1, otherwise set to 0. All "0"s is invalid - there must be at le protected region if inline ECC is enabled through ECCCFG0.e register. All regions are protected with the following setting. ecc_region_map=7'b1111111 - ecc_region_map_granu=0 Onl region is protected with the following setting. - ecc_region_map=7'b0000001 - ecc_region_map_granu=3 Pro Mode: Quasi-dynamic Group 3	

ECC_REGION_REMAP_EN	Enables remapping ECC region feature. Only supported when inline ECC is enabled. - 0 - Disable - 1 - Enable Programming Mode: Static	Enables remapping E feature. Only support ECC is enabled. Progr Static
ECC_AP_EN	Enables address protection feature. Only supported when inline ECC is enabled. - 0 - Disable - 1 - Enable Programming Mode: Static	Enables address prote Only supported when enabled. Programmin
DIS_SCRUB	Disables ECC scrubs. Valid only when ECCCFG0.ecc_mode = 3’b101 and MEMC_USE_RMW is defined. Note: Scrub is not s inline ECC mode and the register value is don’t care. Progran Static	
ECC_MODE	ECC mode indicator. - 000 - ECC disabled - 100 - ECC enabled - SEC/DED over 1 beat - 101 - ECC enabled - Advanced ECC X4/X8 (Illegal value when MEMC_INLINE_ECC=1) - all other settings are reserved for future use Programming Mode: Static	ECC mode indicator. described in "Values" reserved. Programmi

INIT0 fields

Field	lan966x	lan969x	sparx5

SKIP_DRAM_INIT	If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed. - 00 - SDRAM Initialization routine is run after power-up - 01 - SDRAM Initialization routine is skipped after power-up. The controller starts up in normal Mode - 11 - SDRAM Initialization routine is skipped after power-up. The controller starts up in self-refresh Mode - 10 - Reserved Programming Mode: Quasi-dynamic Group 2	If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed. Value "10" is reserved. Programming Mode: Quasi-dynamic Group 2	If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed - 00 - SDRAM Intialization routine is run after power-up - 01 - SDRAM Intialization routine is skipped after power-up. Controller starts up in Normal Mode - 11 - SDRAM Intialization routine is skipped after power-up. Controller starts up in Self-refresh Mode - 10 - SDRAM Intialization routine is run after power-up. Programming Mode: Quasi-dynamic Group 2

POST_CKE_X1024	Indicates the number of cycles to wait after driving CKE high to start the SDRAM initialization sequence. DDR2 typically requires a 400 ns delay, requiring this value to be programmed to 2 at all clock speeds. LPDDR2/ LPDDR3 typically requires this to be programmed for a delay of 200 us. LPDDR4 typically requires this to be programmed for a delay of 2 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	Cycles to wait after driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 typically requires a 400 ns delay, requiring this value to be programmed to 2 at all clock speeds. LPDDR2/ LPDDR3 typically requires this to be programmed for a delay of 200 us. LPDDR4 typically requires this to be programmed for a delay of 2 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static

PRE_CKE_X1024	Indicates the number of cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. DDR2 specifications typically require this to be programmed for a delay of >= 200 us. LPDDR2/LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. For DDR3/DDR4 RDIMMs, this must include the time needed to satisfy tSTAB. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 specifications typically require this to be programmed for a delay of >= 200 us. LPDDR2/ LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. For DDR3/DDR4 RDIMMs, this should include the time needed to satisfy tSTAB Programming Mode: Static

INIT1 fields

Field	lan966x	lan969x	sparx5

DRAM_RSTN_X1024	Indicates the number of cycles to assert SDRAM reset signal during init sequence. This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices. For use with a Synopsys DDR PHY, this must be set to a minimum of 1. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	Number of cycles to assert SDRAM reset signal during init sequence. This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices. For use with a Synopsys DDR PHY, this should be set to a minimum of 1. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 1024 DFI clock cycles. Programming Mode: Static
PRE_OCD_X32	Indicates the wait period before driving the OCD complete command to SDRAM. There is no known specific requirement for this; it may be set to zero. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	Wait period before driving the OCD complete command to SDRAM. Unit: Counts of a global timer that pulses every 32 DFI clock cycles. There is no known specific requirement for this; it may be set to zero. Programming Mode: Static

INIT3 fields

Field	lan966x	lan969x	sparx5

MR	DDR2: Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/ DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/ LPDDR4 - Value to write to MR1 register Programming Mode: Quasi-dynamic Group 1, Group 4	DDR2:Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/ DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/ LPDDR4 - Value to write to MR1 register Programming Mode: Quasi-dynamic Group 1, Group 4	DDR2: Value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/ DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/ LPDDR4 - Value to write to MR1 register Programming Mode: Quasi-dynamic Group 1 and Group 4
EMR	DDR2: Indicates the value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/ LPDDR4 - Value to write to MR2 register. Programming Mode: Quasi-dynamic Group 4		DDR2: Value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/ DDR4: Value to write to MR1 register Set bit 7 to 0. If PHY-evaluation mode training is enabled, this bit is set appropriately by the uMCTL2 during write leveling. mDDR: Value to write to EMR register. LPDDR2/ LPDDR3/LPDDR4 - Value to write to MR2 register Programming Mode: Quasi-dynamic Group 4

INIT4 fields

Field	lan966x	lan969x	sparx5

EMR2	DDR2: Indicates the value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register. LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register. mDDR: Unused. Programming Mode: Quasi-dynamic Group 4	DDR2: Value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register LPDDR2/LPDDR3/ LPDDR4: Value to write to MR3 register mDDR: Unused Programming Mode: Quasi-dynamic Group 4
EMR3	DDR2: Indicates the value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register. mDDR/LPDDR2/LPDDR3: Unused. LPDDR4: Value to write to MR13 register. Programming Mode: Quasi-dynamic Group 2, Group 4	DDR2: Value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register mDDR/LPDDR2/ LPDDR3: Unused LPDDR4: Value to write to MR13 register Programming Mode: Quasi-dynamic Group 2 and Group 4

INIT5 fields

Field	lan966x	lan969x	sparx5

DEV_ZQINIT_X32	ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR2/LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR2/LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Static	ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR2/ LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR2/ LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
MAX_AUTO_INIT_X1024		Maximum duration of the auto initialization, tINIT5. Present only in designs configured to support LPDDR2/ LPDDR3. LPDDR2/ LPDDR3 typically requires 10 us. Unit: 1024 DFI clock cycles. Programming Mode: Static

INIT6 fields

Field	lan966x	lan969x	sparx5
MR5		DDR4 - Indicates the value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Programming Mode: Quasi-dynamic Group 1, Group 4	DDR4- Value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Programming Mode: Quasi-dynamic Group 1 and Group 4
MR4		DDR4 - Indicates the value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Programming Mode: Quasi-dynamic Group 2, Group 4	DDR4- Value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Programming Mode: Quasi-dynamic Group 2 and Group 4

INIT7 fields

Field	lan966x	lan969x	sparx5
MR6		DDR4 - Indicates the value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Programming Mode: Quasi-dynamic Group 4	DDR4- Value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Programming Mode: Quasi-dynamic Group 4

MSTR fields

Field	lan966x	lan969x

ACTIVE_RANKS	Only present for multi-rank configurations. Each bit represents one rank. For two-rank configurations, only bits[25:24] are present. - 1 - Populated - 0 - Unpopulated LSB is the lowest rank number. For two ranks following combinations are legal: - 01 - One rank - 11 - Two ranks - Others - Reserved For four ranks following combinations are legal: - 0001 - One rank - 0011 - Two ranks - 1111 - Four ranks Programming Mode: Static	Only present for multi-rank configurations. Each bit repres one rank. For two-rank configu only bits[25:24] are present. - Populated - 0 - Unpopulated LS lowest rank number. For two ra only the following values are le OneRank - Tworanks - Others - Reserved For four ranks follow combinations are legal: - 0001 rank - 0011 - Two ranks - 1111 ranks Programming Mode: Sta
BURST_RDWR	Indicates SDRAM burst length used: - 0001 - Burst length of 2 (only supported for mDDR) - 0010 - Burst length of 4 - 0100 - Burst length of 8 - 1000 - Burst length of 16 (only supported for mDDR, LPDDR2, and LPDDR4) All other values are reserved. This bit controls the burst size used to access the SDRAM. This must match the burst length mode register setting in the SDRAM. (For BC4/8 on-the-fly mode of DDR3 and DDR4, set this field to 0x0100) Burst length of 2 is not supported with AXI ports when MEMC_BURST_LENGTH is 8. Burst length of 2 is only supported when the controller is operating in 1:1 frequency mode. For DDR3, DDR4 and LPDDR3, this must be set to 0x0100 (BL8). For LPDDR4, this must be set to 0x1000 (BL16). Programming Mode: Static	Indicates SDRAM burst length All other values are reserved.("Values" section) This bit contr burst size used to access the S This must match the burst leng mode register setting in the SD (For BC4/8 on-the-fly mode of and DDR4, set this field to 0x0 Burst length of 2 is not suppor AXI ports when MEMC_BURST_LENGTH is 8. length of 2 is only supported w controller is operating in 1:1 frequency mode. For DDR3, DI LPDDR3, this must be set to 0x (BL8). For LPDDR4, this must to 0x1000 (BL16). Programmin Mode: Static
DLL_OFF_MODE	Set to: - 1 - When the uMCTL2 and DRAM has to be put in DLL-off mode for low frequency operation - 0 - To put uMCTL2 and DRAM in DLL-on mode for normal frequency operation If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), dll_off_mode is not supported, and this bit must be set to '0'. Programming Mode: Quasi-dynamic Group 2	Sets DLL-off mode. If DDR4 CR parity retry is enabled (CRCPARCTL1.crc_parity_retry = 1), dll_off_mode is not suppo and this bit must be set to '0'. Programming Mode: Quasi-dyn Group 2

DATA_BUS_WIDTH	Selects proportion of DQ bus width that is used by the SDRAM. - 00 - Full DQ bus width to SDRAM - 01 - Half DQ bus width to SDRAM - 10 - Quarter DQ bus width to SDRAM - 11 - Reserved Note that half bus width mode is only supported when the SDRAM bus width is a multiple of 16, and quarter bus width mode is only supported when the SDRAM bus width is a multiple of 32 and the configuration parameter MEMC_QBUS_SUPPORT is set. Bus width refers to DQ bus width (excluding any ECC width). Programming Mode: Static	Selects proportion of DQ bus w that is used by the SDRAM. No half bus width mode is only sup when the SDRAM bus width is multiple of 16, and quarter bus mode is only supported when t SDRAM bus width is a multiple and the configuration paramet MEMC_QBUS_SUPPORT is set width refers to DQ bus width (excluding any ECC width). Programming Mode: Static
EN_2T_TIMING_MODE	If 1, then uMCTL2 uses 2T timing, otherwise uses 1T timing. In 2T timing, all command signals (except chip select) are held for 2 clocks on the SDRAM bus. Chip select is asserted on the second cycle of the command. Note: - 2T timing is not supported in LPDDR2/LPDDR3/ LPDDR4 mode - 2T timing is not supported if the configuration parameter MEMC_CMD_RTN2IDLE is set - 2T timing is not supported in DDR4 geardown mode - 2T timing is not supported in Shared-AC dual channel mode and the register value is don’t care Programming Mode: Static	Sets uMCTL2 timing mode. In timing, all command signals (e chip select) are held for 2 cloc the SDRAM bus. Chip select is asserted on the second cycle o command. Note: - 2T timing is supported in LPDDR2/LPDDR3 LPDDR4 mode - 2T timing is no supported if the configuration parameter MEMC_CMD_RTN2 set - 2T timing is not supported DDR4 geardown mode - 2T tim not supported in Shared-AC du channel mode and the register don’t care Programming Mode
BURSTCHOP	When this bit is set, enables burst-chop (BC4 or 8 on-the-fly) in DDR3/ DDR4. Burst Chop for reads is exercised only: - In HIF configurations (UMCTL2_INCL_ARB not set) - If in full bus width mode (MSTR.data_bus_width = 00) - If MEMC_BURST_LENGTH=8 or 16 Burst Chop for writes is exercised only: - If CRC is disabled (CRCPARCTL1.crc_enable = 0) BC4 (fixed) mode is not supported. Programming Mode: Static	Enables Burst Chop(BC4 or 8 o fly) in DDR3/DDR4. Burst Chop reads is exercised only: - In HI configurations (UMCTL2_INCL not set) - If in full bus width mo (MSTR.data_bus_width = 00) - MEMC_BURST_LENGTH=8 or Burst Chop for writes is exerci only: - If CRC is disabled (CRCPARCTL1.crc_enable = 0) (fixed) mode is not supported. Programming Mode: Static

DDR3	Selects DDR3 SDRAM. - 1 - DDR3 SDRAM device in use - 0 - non-DDR3 SDRAM device in use Present only in designs configured to support DDR3. Programming Mode: Static	Selects DDR3 SDRAM. Present designs configured to support Programming Mode: Static
DDR4		Selects DDR4 SDRAM. Present designs configured to support Programming Mode: Static
GEARDOWN_MODE		Indicates the DRAM in geardo mode. This register can be cha only when the controller is in t refresh mode. This signal must the same value as MR3 bit A3. Geardown mode is not support the configuration parameter MEMC_CMD_RTN2IDLE is set Geardown mode is not support the configuration parameter UMCTL2_SHARED_AC is set (i Shared-AC mode) and the regis value is don’t care Programmin Mode: Quasi-dynamic Group 2
DEVICE_CONFIG		Indicates the configuration of t device used in the system. Programming Mode: Static
LPDDR2		
LPDDR3		

ODTCFG fields

Field	lan966x	lan969x	sparx5

WR_ODT_HOLD	DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: - BL8 - 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) - BL4 - 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: - BL8 - 0x6 DDR4: - BL8 - 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: - BL8 - 7 + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 4	DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: - BL8: 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) - BL4: 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: - BL8: 0x6 DDR4: - BL8: 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: - BL8: 7 + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4

WR_ODT_DELAY	Indicates the delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: - CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: - 0x0 DDR4: - DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: - WL - 1 - RU(tODTon(max)/tCK)) Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 4	The delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: - CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: - 0x0 DDR4: - DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: - WL - 1 - RU(tODTon(max)/tCK)) Programming Mode: Quasi-dynamic Group 1 and Group 4

RD_ODT_HOLD	DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: - BL8 - 0x6 (not DDR2-1066), 0x7 (DDR2-1066) - BL4 - 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: - BL8 - 0x6 DDR4: - BL8 - 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) LPDDR3: - BL8 - 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 4	DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: - BL8: 0x6 (not DDR2-1066), 0x7 (DDR2-1066) - BL4: 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: - BL8 - 0x6 DDR4: - BL8: 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: - BL8: 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4

RD_ODT_DELAY	Indicates the delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: - CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: - CL - CWL DDR4: - CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) If (CL - CWL - RD_PREAMBLE + WR_PREAMBLE) < 0, uMCTL2 does not support ODT for read operation. LPDDR3: - RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Programming Mode: Quasi-dynamic Group 1, Group 4	The delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: - CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: - CL - CWL DDR4: - CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) If (CL - CWL - RD_PREAMBLE + WR_PREAMBLE) < 0, uMCTL2 does not support ODT for read operation. LPDDR3: - RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4

PCCFG fields

Field	lan966x	lan969x	sp

BL_EXP_MODE	Burst length expansion mode. By default (that is, bl_exp_mode==0) XPI expands every AXI burst into multiple HIF commands, using the memory burst length as a unit. If set to 1, then XPI uses half of the memory burst length as a unit. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: - MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) - MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Functionality is also not supported if Data Channel Interleave is enabled. Programming Mode: Static	Burst length expansion mode. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: - MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) - MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Functionality is also not supported if Data Channel Interleave is enabled. Programming Mode: Static	Burst length mode. By de bl_exp_mode expands eve into multiple commands, u memory bur unit. If set to will use half burst length applies to bo writes. Wher MSTR.data_ setting bl_ex has no effect used in case Writes is ena (UMCTL2_PA in order to a minimize t_c DDR4 and t_ in LPDDR4. bl_exp_mode recommende LPDDR4. No DBICTL.dm_ functionality supported in cases: - UMCTL2_PA UMCTL2_PA MSTR.data_ MEMC_BUR and MSTR.burst_ (LPDDR4 on UMCTL2_PA MSTR.data_ MEMC_BUR and MSTR.burst_ (DDR4 only) MSTR.burstc CRCPARCTL Functionalit supported if Interleave is Programmin

PAGEMATCH_LIMIT	Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Programming Mode: Static	Page match four limit. Programming Mode: Static	Page match to 1, limits t consecutive DDRC transa be granted b Arbiter to fo Match featu set to 0, ther imposed on consecutive DDRC transa Programmin
GO2CRITICAL_EN	If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr/ co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr/ co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. For uPCTL2, this register field must be set to 0. Programming Mode: Static	If enabled, sets co_gs_go2critical_wr and co_gs_go2critical_lpr/ co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If disabled, co_gs_go2critical_wr and co_gs_go2critical_lpr/ co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. For uPCTL2, this register field must be set to 0. Programming Mode: Static	If set to 1 (e co_gs_go2cr co_gs_go2cr co_gs_go2cr signals going based on urg (awurgent, a coming from set to 0 (disa co_gs_go2cr co_gs_go2cr co_gs_go2cr signals at DI to 1b'0. Prog Mode: Static

PGCR2 fields

Field	lan966x	lan969x	sparx5
DYNACPDD	Dynamic AC Power Down Driver: Powers down, when set, the output driver on I/O for ADDR and BA. This bit is ORed with bit ACIOCR[3] (ACPDD).		

LPMSTRC0	Low-Power Master Channel 0: set to 1 to have channel 0 act as master to drive channel 1 low-power functions simultaneously. Only valid in shared-AC mode.	
ACPDDC	AC Power-Down with Dual Channels : Set to 1 to power-down address/ command lane when both data channels are powered-down. Only valid in shared-AC mode.	
SHRAC	Shared-AC mode: set to 1 to enable shared address/ command mode with two independent data channels - available only if shared address/ command mode support is compiled in.	

DTPMXTMR	Data Training PUB Mode Timer Exit: Specifies the number of controller clocks to wait when entering and exiting pub mode data training. The default value ensures controller refreshes do not cause memory model errors when entering and exiting data training. The value should be increased if controller initiated SDRAM ZQ short or long operation may occur just before or just after the execution of data training.	Data Training PUB Mode Exit Timer.
FXDLAT	Fixed Latency: Specified whether all reads should be returned to the controller with a fixed read latency. Enabling fixed read latency increases the read latency. Valid values are: 0 = Disable fixed read latency 1 = Enable fixed read latency Fixed read latency is calculated as (12 + (maximum DXnGTR.RxDGSL)/2) HDR clock cycles	Fixed Latency.

NOBUB	No Bubbles: Specified whether reads should be returned to the controller with no bubbles. Enabling no-bubble reads increases the read latency. Valid values are: 0 = Bubbles are allowed during reads 1 = Bubbles are not allowed during reads	
TREFPRD	Refresh Period: Indicates the period in clock cycles after which the PUB has to issue a refresh command to the SDRAM. This is derived from the maximum refresh interval from the datasheet, tRFC(max) or REFI, divided by the clock cycle time. A further 400 clocks must be subtracted from the derived number to account for command flow and missed slots of refreshes in the internal PUB blocks. The default corresponds to DDR3 9*7.8us at 1066MHz when a burst of 9 refreshes are issued at every refresh interval.	Refresh Period.
CSNCIDMUX		CSN and CID Multiplexing.
FXDLATINCR		Fixed Latency Programmable Increment.
RFSHMODE		Refresh Mode.
RESERVED_31		Reserved for future use.

PTR0 fields

Field	lan966x	lan969x	sparx5
TPLLPD	PLL Power-Down Time: Number of configuration or APB clock cycles that the PLL must remain in power-down mode, i.e. number of clock cycles from when PLL power-down pin is asserted to when PLL power-down pin is deasserted. This must correspond to a value that is equal to or more than 1us. Default value corresponds to 1us.	PLL Power-Down Time.	
TPLLGS	PLL Gear Shift Time: Number of configuration or APB clock cycles from when the PLL reset pin is deasserted to when the PLL gear shift pin is deasserted. This must correspond to a value that is equal to or more than 4us. Default value corresponds to 4us.	PLL Gear Shift Time.	

TPHYRST	PHY Reset Time: Number of configuration or APB clock cycles that the PHY reset must remain asserted after PHY calibration is done before the reset to the PHY is deasserted. This is used to extend the reset to the PHY so that the reset is asserted for some clock cycles after the clocks are stable. Valid values are from 1 to 63 (the value must be non-zero).	PHY Reset Time.

PTR1 fields

Field	lan966x	lan969x	sparx5
TPLLLOCK	PLL Lock Time: Number of configuration or APB clock cycles for the PLL to stabilize and lock, i.e. number of clock cycles from when the PLL reset pin is deasserted to when the PLL has lock and is ready for use. This must correspond to a value that is equal to or more than 100us. Default value corresponds to 100us.	PLL Lock Time.	

TPLLRST	PLL Reset Time: Number of configuration or APB clock cycles that the PLL must remain in reset mode, i.e. number of clock cycles from when PLL power-down pin is deasserted and PLL reset pin is asserted to when PLL reset pin is deasserted. The setting must correspond to a value that is equal to, or greater than, 3us.	PLL Reset Time.
RESERVED_14_13		Reserved for future use.

PTR2 fields

Field	lan966x	lan969x	sparx5
TWLDLYS	Write Leveling Delay Settling Time: Number of controller clock cycles from when a new value of the write leveling delay is applies to the LCDL to when to DQS high is driven high. This allows the delay to settle.	Write Leveling Delay Settling Time.	
TCALH	Calibration Hold Time: Number of controller clock cycles from when the clock was disabled (cal_clk_en deasserted) to when calibration is enable (cal_en asserted).	Calibration Hold Time.	

TCALS	Calibration Setup Time: Number of controller clock cycles from when calibration is enabled (cal_en asserted) to when the calibration clock is asserted again (cal_clk_en asserted).	Calibration Setup Time.
TCALON	Calibration On Time: Number of clock cycles that the calibration clock is enabled (cal_clk_en asserted).	Calibration On Time.
RESERVED_31_20		Reserved for future use.

PTR3 fields

Field	lan966x	lan969x	sparx5
TDINIT1	DRAM Initialization Time 1: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = CKE high time to first command (tRFC + 10 ns or 5 tCK, whichever is bigger) DDR2 = CKE high time to first command (400 ns) Default value corresponds to DDR3 tRFC of 360ns at 1066 MHz.	DRAM Initialization Time 1.	

TDINIT0	DRAM Initialization Time 0: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = CKE low time with power and clock stable (500 us) DDR2 = CKE low time with power and clock stable (200 us) Default value corresponds to DDR3 500 us at 1066 MHz. During Verilog simulations, it is recommended that this value is changed to a much smaller value in order to avoid long simulation times. However, this may cause a memory model error, due to a violation of the CKE setup sequence. This violation is expected if this value is not programmed to the required SDRAM CKE low time, but memory models should be able to tolerate this violation without malfunction of the model.	DRAM Initialization Time 0.
RESERVED_31_30		Reserved for future use.

PTR4 fields

Field	lan966x	lan969x	sparx5
TDINIT3	DRAM Initialization Time 3: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = Time from ZQ initialization command to first command (1 us) Default value corresponds to the DDR3 640ns at 1066 MHz.	DRAM Initialization Time 3.	
TDINIT2	DRAM Initialization Time 2: DRAM initialization time in DRAM clock cycles corresponding to the following: DDR3 = Reset low time (200 us on power-up or 100 ns after power-up) Default value corresponds to DDR3 200 us at 1066 MHz.	DRAM Initialization Time 2.	
RESERVED_31_29		Reserved for future use.	

PWRCTL fields

Field	lan966x	lan969x

DIS_CAM_DRAIN_SELFREF	Indicates whether skipping CAM draining is allowed when entering self-refresh. This register field cannot be modified while PWRCTL.selfref_sw == 1. - 0 - CAMs must be empty before entering SR - 1 - CAMs are not emptied before entering SR (unsupported) Note, PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. PWRCTL.dis_cam_drain_selfref=0 is required. Programming Mode: Dynamic	Indicates whether skipping draining is allowed when entering self-refresh. This register field cannot be mod while PWRCTL.selfref_sw = Note, PWRCTL.dis_cam_drain_sel is unsupported in this relea PWRCTL.dis_cam_drain_sel is required. Programming M Dynamic
SELFREF_SW	A value of 1 to this register causes system to move to self-refresh state immediately, as long as it is not in INIT or DPD/MPSM operating_mode. This is referred to as Software Entry/Exit to self-refresh. - 1 - Software Entry to self-refresh - 0 - Software Exit from self-refresh Programming Mode: Dynamic	A value of 1 to this register causes system to move to se refresh state immediately, a as it is not in INIT or DPD/M operating_mode. This is refe to as Software Entry/Exit to refresh. Programming Mode Dynamic
EN_DFI_DRAM_CLK_DISABLE	Enables the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR2/DDR3, can only be asserted in self-refresh. In DDR4, can be asserted in following: - In Self-refresh - In Maximum Power Saving Mode In mDDR/LPDDR2/LPDDR3, can be asserted in following: - In Self-refresh - In Power Down - In Deep Power Down - During Normal operation (Clock Stop) In LPDDR4, can be asserted in following: - In Self-refresh Power Down - In Power Down - During Normal operation (Clock Stop) Programming Mode: Dynamic	Enables the assertion of dfi_dram_clk_disable whene clock is not required by the SDRAM. Assertion of dfi_dram_clk_disable is as follows: In DDR2/DDR3, can be asserted in self-refresh. DDR4, can be asserted in following: - In Self-refresh - Maximum Power Saving Mo mDDR/LPDDR2/LPDDR3, ca asserted in following: - In S refresh - In Power Down - In Deep Power Down - During Normal operation (Clock St LPDDR4, can be asserted in following: - In Self-refresh P Down - In Power Down - Du Normal operation (Clock St Programming Mode: Dynam

POWERDOWN_EN	If true then the uMCTL2 goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic	Sets Power-down mode. Thi register bit may be re-programmed during the cou normal operation. Programm Mode: Dynamic
SELFREF_EN	If true then the uMCTL2 puts the SDRAM into self-refresh after a programmable number of cycles "maximum idle clocks before self-refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic	Sets Self-refresh. This regis may be re-programmed dur the course of normal operat Programming Mode: Dynam
MPSM_EN		Sets Maximum powersaving mode. Present only in desig configured to support DDR4 non-DDR4, this register mu be set to 1. Note that MPSM not supported when using a Synopsys DWC DDR PHY, if PHY parameter DWC_AC_CS_USE is disable the MPSM exit sequence re the chip-select signal to tog FOR PERFORMANCE ONLY Programming Mode: Dynam

DEEPPOWERDOWN_EN	

RFSHCTL0 fields

Field	lan966x	lan969x	
REFRESH_MARGIN	Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom/32. Note that internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32 * 32 if RFSHTMG.t_rfc_nom_x1_sel=0. If RFSHTMG.t_rfc_nom_x1_sel=1 (for LPDDR2/LPDDR3/ LPDDR4 per-bank refresh only), internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32. Note that, in LPDDR2/ LPDDR3/LPDDR4, internally used t_rfc_nom may be divided by four if derating is enabled (DERATEEN.derate_enable=1). Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related		Thresho DFI cloc critical expires. be issue is reach that this the defa shown a be less t_rfc_no LPDDR2 internal may be RFSHTI if derati (DERAT Otherw t_rfc_no RFSHTI Unit: M clocks. Dynami

REFRESH_TO_X1_X32	If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. FOR PERFORMANCE ONLY. Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Dynamic - Refresh Related	

REFRESH_BURST	The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. - 0 - Single refresh - 1 - Burst-of-2 refresh - 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/ LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. Programming Mode: Dynamic - Refresh Related	The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. - 0 - Single refresh - 1 - Burst-of-2 refresh - 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/ LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. In LPDDR4 mode, if per-bank refresh is enabled (RFSHCTL0.per_bank_refresh = 1), and automatic switching	The pro the num that is a before t the refr execute perform penalty each gr Therefo refreshe the per- these pa number RFSHCT slightly lower n worst-ca with ref refresh 7 - burs informa feature DDR2 J JESD79 the refr and not refresh over 8*t burst re mode, a Granula refreshe 1X mod mode a mode. I updates the sett RFSHCT ensure violated update before a In this s burst w PHY-init complet Dynami

		from per-bank to all-bank refresh is enabled (RFSHCTL0.auto_refab_en = 2’b01 or RFSHCTL0.auto_refab_en = 2’b10), the uCMTL2 divides this value by 8 when it switches automatically from per-bank to all-bank refresh. Programming Mode: Dynamic - Refresh Related	
PER_BANK_REFRESH			- 1 - Per bank re allows t banks. I support devices support LPDDR4 in desig support LPDDR4 Static
REFRESH_TO_X32			If the re also kno expired has not (RFSHC times ye refresh specula perform refresh before i require bus is id determi RFSHCT the refr at least refresh, refresh Specula continu there ar or until are issu FOR PE Unit: M clocks. Dynami

RFSHCTL3 fields

Field	lan966x	lan969x
REFRESH_UPDATE_LEVEL	Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that registers have been updated. refresh_update_level must not be togg the DDRC is in reset (core_ddrc_rstn = 0). The refresh registers are automatically updated when exiting reset. Programming Mode: Dyn	
DIS_AUTO_REFRESH	When '1', disable auto-refresh generated by the uMCTL2. When auto-refresh is disabled, the SoC must generate refreshes using the registers DBGCMD.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the uMCTL2. If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), disable auto-refresh is not supported, and this bit must be set to '0'. (DDR4 only) If FGR mode is enabled (RFSHCTL3.refresh_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly. Programming Mode: Dynamic - Refresh Related	Disables auto-refresh gene the uMCTL2. When auto-r disabled, the SoC must ge refreshes using the registe DBGCMD.rankn_refresh. W dis_auto_refresh transition 1, any pending refreshes a immediately scheduled by uMCTL2. If DDR4 CRC/pa enabled (CRCPARCTL1.crc_parity_ = 1), disable auto-refresh supported, and this bit mu '0'. (DDR4 only) If FGR mo enabled (RFSHCTL3.refre 0), disable auto-refresh is supported, and this bit mu '0'. This register field is ch the fly. Programming Mod Refresh Related

REFRESH_MODE		Indicates fine granularity mode. Everything not desc "Values" section is reserve Only Fixed 1x mode is sup RFSHCTL3.dis_auto_refre on-the-fly modes are not su this version of the uMCTL must be set up while the c in reset or while the contr self-refresh mode. Changi during normal operation is allowed. Making this a dyn register is supported in fut of the uMCTL2 - This regis effect only if a DDR4 SDRA in use (MSTR.ddr4 = 1) Pr Mode: Quasi-dynamic Grou

RFSHTMG fields

Field	lan966x	lan969x	sparx5

T_RFC_NOM_X1_X32	Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). When the controller is operating in 1:1 mode, set this register to RoundDown(tREFI/tCK) When the controller is operating in 1:2 mode, set this register to RoundDown(RoundDown(tREFI/tCK)/2) In both the previous cases, if RFSHTMG.t_rfc_nom_x1_sel = 0, divide the previous result by 32 and round down. For LPDDR2/LPDDR3/LPDDR4: - If using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), use tREFIab in the previous calculations - If using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), use tREFIpb in the previous calculations For DDR4 mode, tREFI value is different depending on the refresh mode. You must program appropriate value from the spec based on the value programmed in the refresh mode register. Note: - RFSHTMG.t_rfc_nom_x1_x32 must be greater than 0x1 - If RFSHTMG.t_rfc_nom_x1_sel == 1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min - If RFSHTMG.t_rfc_nom_x1_sel == 0, RFSHTMG.t_rfc_nom_x1_x32 * 32 must be greater than RFSHTMG.t_rfc_min - In non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE - In DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF - In DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF Unit: DFI clock cycles or	

	multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Programming Mode: Dynamic - Refresh Related	
T_RFC_MIN	tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min must be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min must be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: - If using all-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCab - If using per-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the previous equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. You must program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI clock cycles. Programming Mode: Dynamic - Refresh Related	tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min should be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min should be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: - if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab - if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user should program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: Clocks. Programming Mode: Dynamic - Refresh Related
LPDDR3_TREFBW_EN		Used only when LPDDR3 memory type is connected. Should only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: - 0 - tREFBW parameter not used - 1 - tREFBW parameter used Programming Mode: Static

T_RFC_NOM_X32		tREFI: Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). For LPDDR2/ LPDDR3/LPDDR4: - if using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), this register should be set to tREFIab - if using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), this register should be set to tREFIpb When the controller is operating in 1:2 frequency ratio mode, program this to (tREFI/2), no rounding up. In DDR4 mode, tREFI value is different depending on the refresh mode. The user should program the appropriate value from the spec based on the value programmed in the refresh mode register. Note that RFSHTMG.t_rfc_nom_x32 * 32 must be greater than RFSHTMG.t_rfc_min, and RFSHTMG.t_rfc_nom_x32 must be greater than 0x1. - Non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x32 must be less than or equal to 0xFFE. - DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x32 must be less than or equal to 0x7FF. - DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x32 must be less than or equal to 0x3FF. Unit: Multiples of 32 clocks. Programming Mode: Dynamic - Refresh Related

SBRCTL fields

Field	lan966x	lan969x	sparx5

SCRUB_INTERVAL	Scrub interval. (512 x scrub_interval) number of clock cycles between two scrub read commands. If set to 0, scrub commands are issued back-to-back. This mode of operation (scrub_interval=0) can typically be used for scrubbing the full range of memory at once before or after SW controlled low power operations. After completing the full range of scrub while scrub_interval=0, scrub_done register is set and sbr_done_intr interrupt signal is asserted. This mode can not be used with Inline ECC: If MEMC_INLINE_ECC is 1 and scrub_interval is programme to 0, then RMW logic inside scrubber is disabled. New programmed value takes effect only after scrubber is disabled by programming scrub_en to 0. Unit: Multiples of 512 sbr_clk cycles. Programming Mode: Dynamic	Scrub interval. (512 x scrub_interval) number of clock cycles between two scrub read commands. If s to 0, scrub commands are issued back-to-back. This mode of operation (scrub_interval=0) can typically be used for scrubbing the full range o memory at once before or after SW controlled low power operations. After completing the full range scrub while scrub_interval=0, scrub_done register is set and sbr_done_intr interrup signal is asserted. This mode can’t be used with Inline ECC: If MEMC_INLINE_ECC is 1 and scrub_interval is programme to 0, then RM logic inside scrubber is disabled. New programme value will take effect only after scrubber is disabled programming scrub_en to Programming Mode: Dynamic

SCRUB_BURST	Scrub burst count. Determines the number of back-to-back scrub read commands that can be issued together when the controller is in one of the HW controlled low power modes with Sideband ECC, both normal operation mode and low-power mode with Inline ECC. During these modes, the period of the scrub burst becomes "scrub_burst*scrub_interval" cycles. During normal operation mode of the controller with Sideband ECC (not in power-down or self-refresh), scrub_burst is ignored and only one scrub command is generated. Valid values are (Sideband ECC): 1: 1 read, 2: 4 reads, 3: 16 reads, 4: 64 reads, 5: 256 reads, 6: 1024 reads. (Inline ECC): 1: 8 reads, 2: 16 reads, 3: 32 reads. New programmed value takes effect only after scrubber is disabled by programming scrub_en to 0. Programming Mode: Dynamic		Scrub burst count. Determines the number of back-to-back scrub read commands that can be issued together when the controller is in one of the HW controlled low power modes with Sideband ECC both normal operation mo and low-power mode with Inline ECC. During these modes, the period of the scrub burst becomes "scrub_burst*scrub_interv cycles. During normal operation mode of the controller with Sideband ECC (not in power-down o self refresh), scrub_burst i ignored and only one scru command is generated. Valid values are (Sideband ECC): 1: 1 read, 2: 4 reads 3: 16 reads, 4: 64 reads, 5 256 reads, 6: 1024 reads. (Inline ECC): 1: 8 reads, 2 16 reads, 3: 32 reads. New programmed value will tak effect only after scrubber disabled by programming scrub_en to 0. Programmi Mode: Dynamic
SCRUB_MODE	- scrub_mode:0 ECC scrubber performs reads - scrub_mode:1 ECC scrubber performs writes Programming Mode: Dynamic	Sets scrub_mode. Programming Mode: Dynamic	scrub_mode:0 ECC scrubb will perform reads scrub_mode:1 ECC scrubb will perform writes Programming Mode: Dynamic

SCRUB_DURING_LOWPOWER	Continue scrubbing during low power. If set to 1, burst of scrubs is issued in hardware controlled low power modes. There are two such modes: automatically initiated by idleness or initiated by Hardware low power interface. If set to 0, the scrubber does not attempt to send commands while the DDRC is in HW controlled low power modes. In this case, the scrubber remembers the last address issued and automatically continues from there when the DDRC exits the low power mode. Programming Mode: Dynamic	Continue scrubbing during low power. If enabled, burst of scrubs is issued in hardware controlled low power modes. There are two such modes: automatically initiated by idleness or initiated by Hardware low power interface. If disabled, the scrubber does not attempt to send commands while the DDRC is in HW controlled low power modes. In this case, the scrubber remembers the last address issued and automatically continues from there when the DDRC exits the low power mode. Programming Mode: Dynamic	Continue scrubbing during low power. If set to 1, burs of scrubs will be issued in HW controlled low power modes. There are two such modes: automatically initiated by idleness or initiated by Hardware low power interface. If set to 0 the scrubber will not attempt to send command while the DDRC is in HW controlled low power mod In this case, the scrubber will remember the last address issued and will automatically continue fro there when the DDRC exit the LP mode. Programmin Mode: Dynamic

SCRUB_EN	Enables ECC scrubber. If set to 1, enables the scrubber to generate background read commands after the memories are initialized. If set to 0, disables the scrubber, resets the address generator to 0 and clears the scrubber status. This bitfield must be accessed separately from the other bitfields in this register. Programming Mode: Dynamic	Enables ECC scrubber. (Enabled)Enables the scrubber to generate background read commands after the memories are initialized. (Disabled)Disables the scrubber, resets the address generator to 0 and clears the scrubber status. This bitfield must be accessed separately from the other bitfields in this register. Programming Mode: Dynamic	Enable ECC scrubber. If se to 1, enables the scrubber generate background read commands after the memories are initialized. I set to 0, disables the scrubber, resets the addre generator to 0 and clears the scrubber status. This bitfield must be accessed separately from the other bitfields in this register. Programming Mode: Dynamic

SCHCR1 fields

Field	lan966x	lan969x	sparx5
RESERVED_1_0		Reserved for future use.	
ALLRANK		All Ranks Enabled.	
RESERVED_3		Reserved for future use.	
SCBK		Scheduler Command Bank Address.	
SCBG		Scheduler Command Bank Group.	
SCADDR		Scheduler Command Address.	
SCRNK		Scheduler Rank Address.	

ZQ0CR0 fields

Field	lan966x	lan969x	sparx5
ZQ0_ZQPD	ZQ Power Down: Powers down, if set, the PZQ cell.		
ZQ0_ZCALEN	Impedance Calibration Enable: Enables, if set, the impedance calibration of this ZQ control block when impedance calibration is triggered using either the ZCAL bit of PIR register or the DFI update interface.		
ZQ0_ZCALBYP	Impedance Calibration Bypass: Bypasses, if set, impedance calibration of this ZQ control block when impedance calibration is already in progress. Impedance calibration can be disabled prior to trigger by using the ZCALEN bit.		
ZQ0_ZDEN	Impedance Over-ride Enable: When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZDATA field. Otherwise, the control is generated automatically by the impedance control logic.		

ZQ0_ZDATA	Impedance Over-Ride Data: Data used to directly drive the impedance control. ZDATA field mapping for D3F I/Os is as follows: ZDATA[27:21] is used to select the pull-up on-die termination impedance ZDATA[20:14] is used to select the pull-down on-die termination impedance ZDATA[13:7] is used to select the pull-up output impedance ZDATA[6:0] is used to select the pull-down output impedance ZDATA field mapping for D3A/B/R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance The default value is 0x000014A for I/O	

	type D3C/R and 0x0001830 for I/O type D3F.		

ZQ0CR1 fields

Field	lan966x	lan969x	sparx5
ZQ0_DFIPU1	DFI Update Interface 1: Sets this impedance controller to be enabled for calibration when the DFI PHY update interface 1 (channel 1) requests an update. Only valid in shared-AC mode.		
ZQ0_DFIPU0	DFI Update Interface 0: Sets this impedance controller to be enabled for calibration when the DFI PHY update interface 0 (channel 0) requests an update.		
ZQ0_DFICCU	DFI Concurrent Controller Update Interface: Sets this impedance controller to be enabled for calibration when both of the DFI controller update interfaces request an update on the same clock. This provides the ability to enable impedance calibration updates for the Address/ Command lane. Only valid in shared-AC mode.		

ZQ0_DFICU1	DFI Controller Update Interface 1: Sets this impedance controller to be enabled for calibration when the DFI controller update interface 1 (channel 1) requests an update.	
ZQ0_DFICU0	DFI Controller Update Interface 0: Sets this impedance controller to be enabled for calibration when the DFI controller update interface 0 (channel 0) requests an update.	
ZQ0_ZPROG	Impedance Divide Ratio: Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4] = On-die termination divide select ZPROG[3:0] = Output impedance divide select	

ZQ0PR fields

Field	lan966x	lan969x	sparx5
RESERVED_7_0		Reserved for future use.	
ZPROG_ASYM_DRV_PU		Asymmetric Drive Pull-up Impedance Divide Ratio.	
ZPROG_ASYM_DRV_PD		Asymmetric Drive Pull-down Impedance Divide Ratio.	
ZPROG_PU_ODT_ONLY		ODT Pull-up Impedance Divide Ratio.	

PU_DRV_ADJUST		Pull-up Drive Strength Adjustment.	
PD_DRV_ADJUST		Pull-down Drive Strength Adjustment.	
RESERVED_27_24		Reserved for future use.	
PU_ODT_ONLY		Pull-up ODT Only Enable.	
ZSEGBYP		Impedance Calibration Segment Bypass.	
ODT_ZDEN		On-Die Termination Over-ride Enable.	
DRV_ZDEN		Output Impedance Over-Ride Enable.	
ZQDIV			Impedance Divide Ratio.
ZCTRL_UPPER			ZCTRL Upper Bus.
RESERVED_31_28			Reserved for future use.

ZQ1CR0 fields

Field	lan966x	lan969x	sparx5
ZQ1_ZQPD	ZQ Power Down: Powers down, if set, the PZQ cell.		

ZQ1_ZCALEN	Impedance Calibration Enable: Enables, if set, the impedance calibration of this ZQ control block when impedance calibration is triggered using either the ZCAL bit of PIR register or the DFI update interface.	
ZQ1_ZCALBYP	Impedance Calibration Bypass: Bypasses, if set, impedance calibration of this ZQ control block when impedance calibration is already in progress. Impedance calibration can be disabled prior to trigger by using the ZCALEN bit.	
ZQ1_ZDEN	Impedance Over-ride Enable: When this bit is set, it allows users to directly drive the impedance control using the data programmed in the ZDATA field. Otherwise, the control is generated automatically by the impedance control logic.	

ZQ1_ZDATA	Impedance Over-Ride Data: Data used to directly drive the impedance control. ZDATA field mapping for D3F I/Os is as follows: ZDATA[27:21] is used to select the pull-up on-die termination impedance ZDATA[20:14] is used to select the pull-down on-die termination impedance ZDATA[13:7] is used to select the pull-up output impedance ZDATA[6:0] is used to select the pull-down output impedance ZDATA field mapping for D3A/B/R I/Os is as follows: ZDATA[27:20] is reserved and returns zeros on reads ZDATA[19:15] is used to select the pull-up on-die termination impedance ZDATA[14:10] is used to select the pull-down on-die termination impedance ZDATA[9:5] is used to select the pull-up output impedance ZDATA[4:0] is used to select the pull-down output impedance The default value is 0x000014A for I/O	

	type D3C/R and 0x0001830 for I/O type D3F.		

ZQ1CR1 fields

Field	lan966x	lan969x	sparx5
ZQ1_DFIPU1	DFI Update Interface 1: Sets this impedance controller to be enabled for calibration when the DFI PHY update interface 1 (channel 1) requests an update. Only valid in shared-AC mode.		
ZQ1_DFIPU0	DFI Update Interface 0: Sets this impedance controller to be enabled for calibration when the DFI PHY update interface 0 (channel 0) requests an update.		
ZQ1_DFICCU	DFI Concurrent Controller Update Interface: Sets this impedance controller to be enabled for calibration when both of the DFI controller update interfaces request an update on the same clock. This provides the ability to enable impedance calibration updates for the Address/ Command lane. Only valid in shared-AC mode.		

ZQ1_DFICU1	DFI Controller Update Interface 1: Sets this impedance controller to be enabled for calibration when the DFI controller update interface 1 (channel 1) requests an update.	
ZQ1_DFICU0	DFI Controller Update Interface 0: Sets this impedance controller to be enabled for calibration when the DFI controller update interface 0 (channel 0) requests an update.	
ZQ1_ZPROG	Impedance Divide Ratio: Selects the external resistor divide ratio to be used to set the output impedance and the on-die termination as follows: ZPROG[7:4] = On-die termination divide select ZPROG[3:0] = Output impedance divide select	

ZQ1PR fields

Field	lan966x	lan969x	sparx5
RESERVED_7_0		Reserved for future use.	
ZPROG_ASYM_DRV_PU		Asymmetric Drive Pull-up Impedance Divide Ratio.	
ZPROG_ASYM_DRV_PD		Asymmetric Drive Pull-down Impedance Divide Ratio.	
ZPROG_PU_ODT_ONLY		ODT Pull-up Impedance Divide Ratio.	

PU_DRV_ADJUST		Pull-up Drive Strength Adjustment.	
PD_DRV_ADJUST		Pull-down Drive Strength Adjustment.	
RESERVED_27_24		Reserved for future use.	
PU_ODT_ONLY		Pull-up ODT Only Enable.	
ZSEGBYP		Impedance Calibration Segment Bypass.	
ODT_ZDEN		On-Die Termination Over-ride Enable.	
DRV_ZDEN		Output Impedance Over-Ride Enable.	
ZQDIV			Impedance Divide Ratio.
ZCTRL_UPPER			ZCTRL Upper Bus.
RESERVED_31_28			Reserved for future use.

ZQ2PR fields

Field	lan966x	lan969x	sparx5
RESERVED_7_0		Reserved for future use.	
ZPROG_ASYM_DRV_PU		Asymmetric Drive Pull-up Impedance Divide Ratio.	
ZPROG_ASYM_DRV_PD		Asymmetric Drive Pull-down Impedance Divide Ratio.	
ZPROG_PU_ODT_ONLY		ODT Pull-up Impedance Divide Ratio.	
PU_DRV_ADJUST		Pull-up Drive Strength Adjustment.	

PD_DRV_ADJUST		Pull-down Drive Strength Adjustment.	
RESERVED_27_24		Reserved for future use.	
PU_ODT_ONLY		Pull-up ODT Only Enable.	
ZSEGBYP		Impedance Calibration Segment Bypass.	
ODT_ZDEN		On-Die Termination Over-ride Enable.	
DRV_ZDEN		Output Impedance Over-Ride Enable.	
ZQDIV			Impedance Divide Ratio.
ZCTRL_UPPER			ZCTRL Upper Bus.
RESERVED_31_28			Reserved for future use.

ZQCR fields

Field	lan966x	lan969x	sparx5
RESERVED_0		Reserved for future use.	
TERM_OFF		Termination OFF.	
ZQPD		ZQ Power Down.	
RESERVED_7_3		Reserved for future use.	
PGWAIT		Programmable Wait.	
ZCALT		Impedance Calibration Type.	
AVGMAX		Maximum Averaging Round.	
AVGEN		Averaging Algorithm Enable.	

IODLMT		IO VT Drift Limit.	
RESERVED_26_25		Reserved for future use.	
FORCE_ZCAL_VT_UPDATE		Force Impedance Calibration VT Update.	
RESERVED_31_28		Reserved for future use.	
ASYM_DRV_EN			Enable Asymmetric Drive Strength Enable.
PU_ODT_ONLY			Pull-up ODT Only Enable.
DIS_NON_LIN_COMP			Disable Non-linear Compensation Enable.
ZCTRL_UPPER			ZCTRL Upper Bus.

References

- [1] DesignWare Cores Enhanced Universal DDR Memory Controller (uMCTL2) Databook