

# pFREYA DAQ documentation

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## Summary

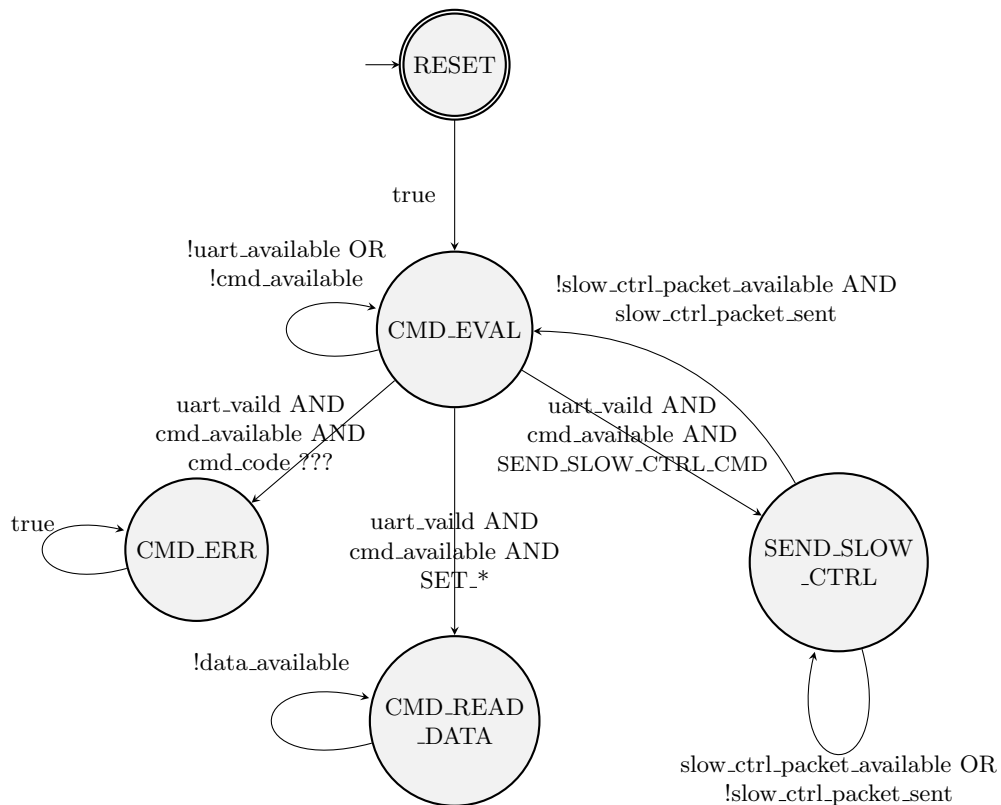
This document provides information on the Data Acquisition (DAQ) system to test the pFREYA16 and pFREYATS ASICs. The system is based on a Xilinx Ultrascale+ FPGA Evaluation Board (KCU116) and it is written in SystemVerilog/Verilog.

**1 State machine**

**2**

# 1 State machine

This section illustrates the state machine on the FPGA.



## References

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