3.3.8.2 Memory maps

The peripheral bridges are used to access the registers of most of the modules on this device. See AIPS0 Memory Map and AIPS1 Memory Map for the memory slot assignment for each module.

3.3.8.3 AIPS_Lite MPRA register reset value

- AIPS*x*_MPRA reset value is 0x7770_0000

Therefore, masters 0, 1, and 2 are trusted bus masters after reset.

3.3.8.4 AIPS_Lite PACRA-P and PACRU register reset values

The reset values for the AIPS_Lite registers are listed in the following table.

Register name	AIPS0 reset value	AIPS1 reset value
PACRA	0x5000_4000	0x5000_0000
PACRB	0x4400_4400	0x0000_0000
PACRC	0x0000_0000	0x0000_0000
PACRD	0x0000_0004	0x0000_0000
PACRE	0x4444_4444	0x4444_4444
PACRF	0x4444_4444	0x4444_4444
PACRG	0x4444_4444	0x4444_4444
PACRH	0x4444_4444	0x4444_4444
PACRI	0x4444_4444	0x4444_4444
PACRJ	0x4444_4444	0x4444_4444
PACRK	0x4444_4444	0x4444_4444
PACRL	0x4444_4444	0x4444_4444
PACRM	0x4444_4444	0x4444_4444
PACRN	0x4444_4444	0x4444_4444
PACRO	0x4444_4444	0x4444_4444
PACRP	0x4444_4444	0x4444_4444
PACRU	0x4400_0000	0x4400_0000

3.3.9 DMA request multiplexer configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

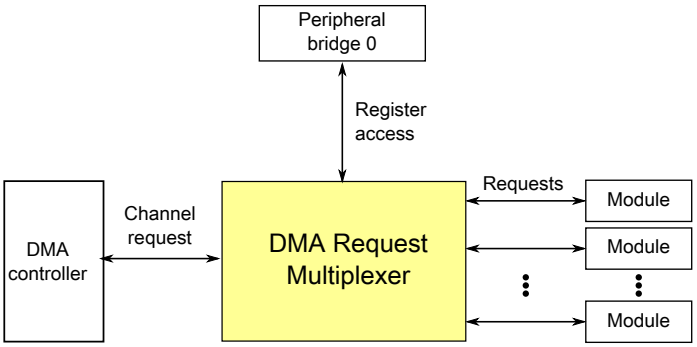

Figure 3-14. DMA request multiplexer configuration

Table 3-25. Reference links to related information

Topic	Related module	Reference
Full description	DMA request multiplexer	DMA Mux
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Channel request	DMA controller	DMA Controller
Requests		DMA request sources

3.3.9.1 DMA MUX request sources

This device includes a DMA request mux that allows up to 63 DMA request signals to be mapped to any of the 16 DMA channels. Because of the mux there is not a hard correlation between any of the DMA request sources and a specific DMA channel.

Table 3-26. DMA request sources - MUX 0

Source number	Source module	Source description
0	—	Channel disabled[1]
1	Reserved	Not used
2	UART0	Receive
3	UART0	Transmit
4	UART1	Receive
5	UART1	Transmit
6	UART2	Receive
7	UART2	Transmit
8	UART3	Receive
9	UART3	Transmit

Table continues on the next page...

Table 3-26. DMA request sources - MUX 0 (continued)

Source number	Source module	Source description
10	UART4	Transmit or Receive
11	UART5	Transmit or Receive
12	I^2S0	Receive
13	I^2S0	Transmit
14	SPI0	Receive
15	SPI0	Transmit
16	SPI1	Transmit or Receive
17	SPI2	Transmit or Receive
18	I^2C0	—
19	I^2C1 or I^2C2	—
20	FTM0	Channel 0
21	FTM0	Channel 1
22	FTM0	Channel 2
23	FTM0	Channel 3
24	FTM0	Channel 4
25	FTM0	Channel 5
26	FTM0	Channel 6
27	FTM0	Channel 7
28	FTM1	Channel 0
29	FTM1	Channel 1
30	FTM2	Channel 0
31	FTM2	Channel 1
32	FTM3	Channel 0
33	FTM3	Channel 1
34	FTM3	Channel 2
35	FTM3	Channel 3
36	FTM3	Channel 4
37	FTM3	Channel 5
38	FTM3	Channel 6
39	FTM3	Channel 7
40	ADC0	—
41	ADC1	—
42	CMP0	—
43	CMP1	—
44	CMP2	—
45	DAC0	—
46	DAC1	—
47	CMT	—
48	PDB	—

Table continues on the next page...

Table 3-26. DMA request sources - MUX 0 (continued)

Source number	Source module	Source description
49	Port control module	Port A
50	Port control module	Port B
51	Port control module	Port C
52	Port control module	Port D
53	Port control module	Port E
54	IEEE 1588 Timers	Timer 0
55	IEEE 1588 Timers	Timer 1
56	IEEE 1588 Timers	Timer 2
57	IEEE 1588 Timers	Timer 3
58	DMA MUX	Always enabled
59	DMA MUX	Always enabled
60	DMA MUX	Always enabled
61	DMA MUX	Always enabled
62	DMA MUX	Always enabled
63	DMA MUX	Always enabled

1. Configuring a DMA channel to select source 0 or any of the reserved sources disables that DMA channel.

3.3.9.2 DMA transfers via PIT trigger

The PIT module can trigger a DMA transfer on the first four DMA channels. The assignments are detailed at PIT/DMA Periodic Trigger Assignments .

3.3.10 DMA Controller Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

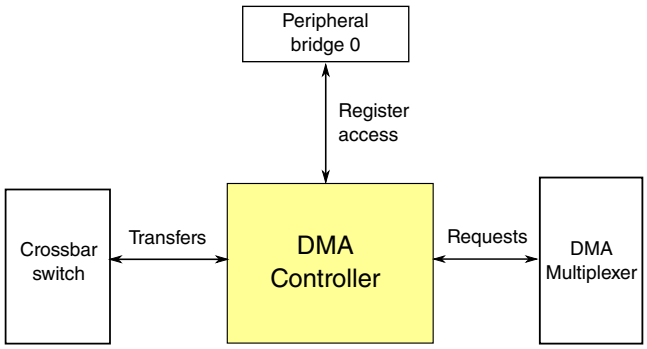

Figure 3-15. DMA Controller configuration

Table 3-27. Reference links to related information

Topic	Related module	Reference
Full description	DMA Controller	DMA Controller
System memory map		System memory map
Register access	Peripheral bridge (AIPS-Lite 0)	AIPS-Lite 0
Clocking		Clock distribution
Power management		Power management
Transfers	Crossbar switch	Crossbar switch

3.3.11 External Watchdog Monitor (EWM) Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.