Chapter 37
12-bit Digital-to-Analog Converter (DAC)

37.1 Introduction

NOTE

For the chip-specific implementation details of this module's instances, see the chip configuration information.

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, op-amps, or ADC.

37.2 Features

The features of the DAC module include:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 V_{in} to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources
- Static operation in Normal Stop mode
- 16-word data buffer supported with configurable watermark and multiple operation modes
- DMA support

37.3 Block diagram

The block diagram of the DAC module is as follows:

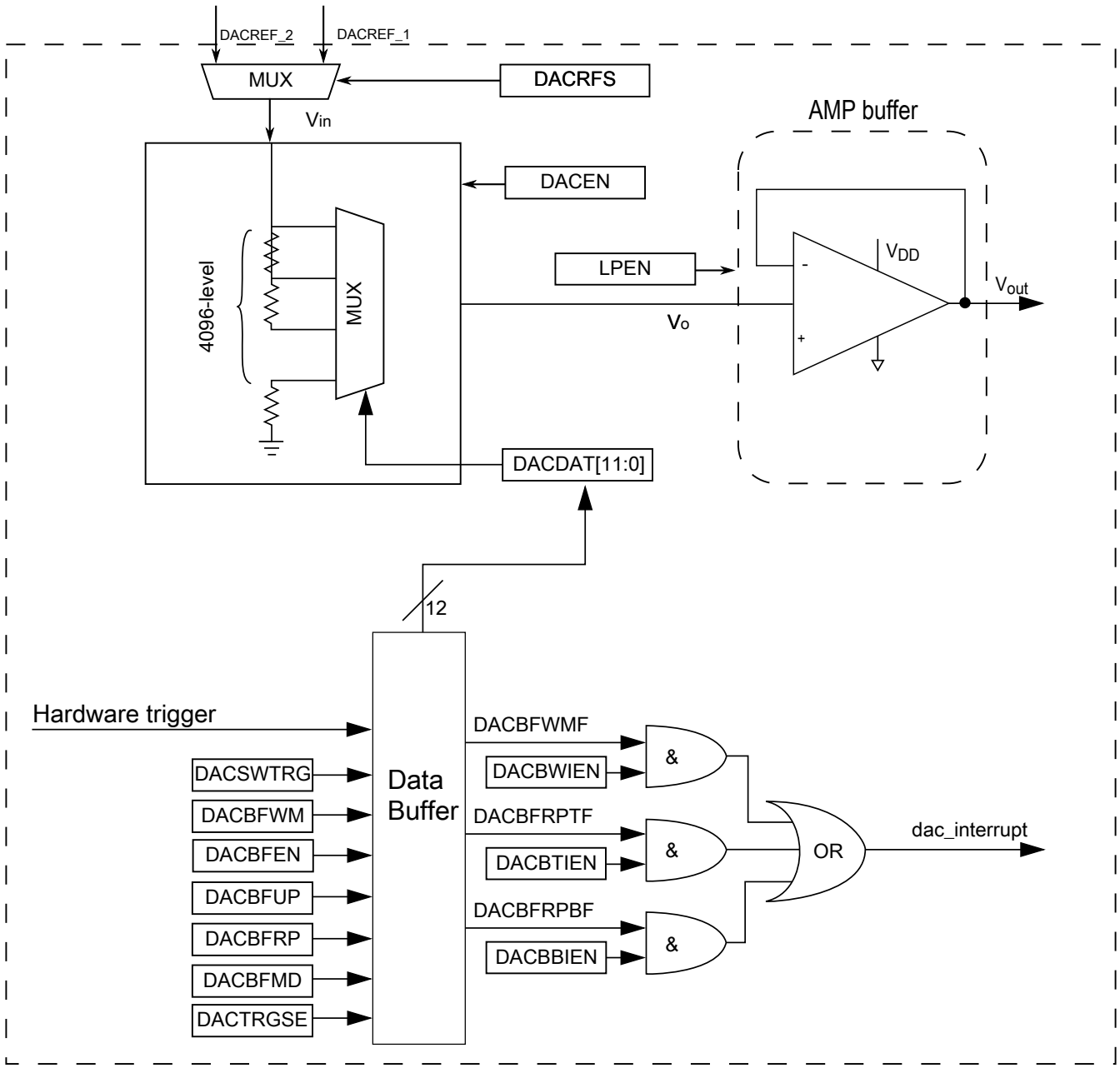

Figure 37-1. DAC block diagram

37.4 Memory map/register definition

The DAC has registers to control analog comparator and programmable voltage divider to perform the digital-to-analog functions.

DAC memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_C000	DAC Data Low Register (DAC0_DAT0L)	8	R/W	00h	37.4.1/933
400C_C001	DAC Data High Register (DAC0_DAT0H)	8	R/W	00h	37.4.2/933
400C_C002	DAC Data Low Register (DAC0_DAT1L)	8	R/W	00h	37.4.1/933
400C_C003	DAC Data High Register (DAC0_DAT1H)	8	R/W	00h	37.4.2/933
400C_C004	DAC Data Low Register (DAC0_DAT2L)	8	R/W	00h	37.4.1/933
400C_C005	DAC Data High Register (DAC0_DAT2H)	8	R/W	00h	37.4.2/933
400C_C006	DAC Data Low Register (DAC0_DAT3L)	8	R/W	00h	37.4.1/933
400C_C007	DAC Data High Register (DAC0_DAT3H)	8	R/W	00h	37.4.2/933
400C_C008	DAC Data Low Register (DAC0_DAT4L)	8	R/W	00h	37.4.1/933
400C_C009	DAC Data High Register (DAC0_DAT4H)	8	R/W	00h	37.4.2/933
400C_C00A	DAC Data Low Register (DAC0_DAT5L)	8	R/W	00h	37.4.1/933
400C_C00B	DAC Data High Register (DAC0_DAT5H)	8	R/W	00h	37.4.2/933
400C_C00C	DAC Data Low Register (DAC0_DAT6L)	8	R/W	00h	37.4.1/933
400C_C00D	DAC Data High Register (DAC0_DAT6H)	8	R/W	00h	37.4.2/933
400C_C00E	DAC Data Low Register (DAC0_DAT7L)	8	R/W	00h	37.4.1/933
400C_C00F	DAC Data High Register (DAC0_DAT7H)	8	R/W	00h	37.4.2/933
400C_C010	DAC Data Low Register (DAC0_DAT8L)	8	R/W	00h	37.4.1/933
400C_C011	DAC Data High Register (DAC0_DAT8H)	8	R/W	00h	37.4.2/933
400C_C012	DAC Data Low Register (DAC0_DAT9L)	8	R/W	00h	37.4.1/933
400C_C013	DAC Data High Register (DAC0_DAT9H)	8	R/W	00h	37.4.2/933
400C_C014	DAC Data Low Register (DAC0_DAT10L)	8	R/W	00h	37.4.1/933
400C_C015	DAC Data High Register (DAC0_DAT10H)	8	R/W	00h	37.4.2/933
400C_C016	DAC Data Low Register (DAC0_DAT11L)	8	R/W	00h	37.4.1/933
400C_C017	DAC Data High Register (DAC0_DAT11H)	8	R/W	00h	37.4.2/933
400C_C018	DAC Data Low Register (DAC0_DAT12L)	8	R/W	00h	37.4.1/933
400C_C019	DAC Data High Register (DAC0_DAT12H)	8	R/W	00h	37.4.2/933
400C_C01A	DAC Data Low Register (DAC0_DAT13L)	8	R/W	00h	37.4.1/933
400C_C01B	DAC Data High Register (DAC0_DAT13H)	8	R/W	00h	37.4.2/933
400C_C01C	DAC Data Low Register (DAC0_DAT14L)	8	R/W	00h	37.4.1/933
400C_C01D	DAC Data High Register (DAC0_DAT14H)	8	R/W	00h	37.4.2/933
400C_C01E	DAC Data Low Register (DAC0_DAT15L)	8	R/W	00h	37.4.1/933
400C_C01F	DAC Data High Register (DAC0_DAT15H)	8	R/W	00h	37.4.2/933
400C_C020	DAC Status Register (DAC0_SR)	8	R/W	02h	37.4.3/933
400C_C021	DAC Control Register (DAC0_C0)	8	R/W	00h	37.4.4/934
400C_C022	DAC Control Register 1 (DAC0_C1)	8	R/W	00h	37.4.5/935
400C_C023	DAC Control Register 2 (DAC0_C2)	8	R/W	0Fh	37.4.6/936
400C_D000	DAC Data Low Register (DAC1_DAT0L)	8	R/W	00h	37.4.1/933
400C_D001	DAC Data High Register (DAC1_DAT0H)	8	R/W	00h	37.4.2/933

Table continues on the next page...

DAC memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400C_D002	DAC Data Low Register (DAC1_DAT1L)	8	R/W	00h	37.4.1/933
400C_D003	DAC Data High Register (DAC1_DAT1H)	8	R/W	00h	37.4.2/933
400C_D004	DAC Data Low Register (DAC1_DAT2L)	8	R/W	00h	37.4.1/933
400C_D005	DAC Data High Register (DAC1_DAT2H)	8	R/W	00h	37.4.2/933
400C_D006	DAC Data Low Register (DAC1_DAT3L)	8	R/W	00h	37.4.1/933
400C_D007	DAC Data High Register (DAC1_DAT3H)	8	R/W	00h	37.4.2/933
400C_D008	DAC Data Low Register (DAC1_DAT4L)	8	R/W	00h	37.4.1/933
400C_D009	DAC Data High Register (DAC1_DAT4H)	8	R/W	00h	37.4.2/933
400C_D00A	DAC Data Low Register (DAC1_DAT5L)	8	R/W	00h	37.4.1/933
400C_D00B	DAC Data High Register (DAC1_DAT5H)	8	R/W	00h	37.4.2/933
400C_D00C	DAC Data Low Register (DAC1_DAT6L)	8	R/W	00h	37.4.1/933
400C_D00D	DAC Data High Register (DAC1_DAT6H)	8	R/W	00h	37.4.2/933
400C_D00E	DAC Data Low Register (DAC1_DAT7L)	8	R/W	00h	37.4.1/933
400C_D00F	DAC Data High Register (DAC1_DAT7H)	8	R/W	00h	37.4.2/933
400C_D010	DAC Data Low Register (DAC1_DAT8L)	8	R/W	00h	37.4.1/933
400C_D011	DAC Data High Register (DAC1_DAT8H)	8	R/W	00h	37.4.2/933
400C_D012	DAC Data Low Register (DAC1_DAT9L)	8	R/W	00h	37.4.1/933
400C_D013	DAC Data High Register (DAC1_DAT9H)	8	R/W	00h	37.4.2/933
400C_D014	DAC Data Low Register (DAC1_DAT10L)	8	R/W	00h	37.4.1/933
400C_D015	DAC Data High Register (DAC1_DAT10H)	8	R/W	00h	37.4.2/933
400C_D016	DAC Data Low Register (DAC1_DAT11L)	8	R/W	00h	37.4.1/933
400C_D017	DAC Data High Register (DAC1_DAT11H)	8	R/W	00h	37.4.2/933
400C_D018	DAC Data Low Register (DAC1_DAT12L)	8	R/W	00h	37.4.1/933
400C_D019	DAC Data High Register (DAC1_DAT12H)	8	R/W	00h	37.4.2/933
400C_D01A	DAC Data Low Register (DAC1_DAT13L)	8	R/W	00h	37.4.1/933
400C_D01B	DAC Data High Register (DAC1_DAT13H)	8	R/W	00h	37.4.2/933
400C_D01C	DAC Data Low Register (DAC1_DAT14L)	8	R/W	00h	37.4.1/933
400C_D01D	DAC Data High Register (DAC1_DAT14H)	8	R/W	00h	37.4.2/933
400C_D01E	DAC Data Low Register (DAC1_DAT15L)	8	R/W	00h	37.4.1/933
400C_D01F	DAC Data High Register (DAC1_DAT15H)	8	R/W	00h	37.4.2/933
400C_D020	DAC Status Register (DAC1_SR)	8	R/W	02h	37.4.3/933
400C_D021	DAC Control Register (DAC1_C0)	8	R/W	00h	37.4.4/934
400C_D022	DAC Control Register 1 (DAC1_C1)	8	R/W	00h	37.4.5/935
400C_D023	DAC Control Register 2 (DAC1_C2)	8	R/W	0Fh	37.4.6/936

37.4.1 DAC Data Low Register (DAC*x*_DAT*n*L)

Address: Base address + 0h offset + (2d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read Write	DATA0							
Reset	0	0	0	0	0	0	0	0

DAC*x*_DAT*n*L field descriptions

Field	Description
DATA0	DATA0 When the DAC buffer is not enabled, DATA[11:0] controls the output voltage based on the following formula: $V_{out} = V_{in} * (1 + DACDAT0[11:0])/4096$ When the DAC buffer is enabled, DATA is mapped to the 16-word buffer.

37.4.2 DAC Data High Register (DAC*x*_DAT*n*H)

Address: Base address + 1h offset + (2d × i), where i=0d to 15d

Bit	7	6	5	4	3	2	1	0
Read	0				DATA1			
Write								
Reset	0	0	0	0	0	0	0	0

DAC*x*_DAT*n*H field descriptions

Field	Description
7–4 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
DATA1	DATA1 When the DAC Buffer is not enabled, DATA[11:0] controls the output voltage based on the following formula. $V_{out} = V_{in} * (1 + DACDAT0[11:0])/4096$ When the DAC buffer is enabled, DATA[11:0] is mapped to the 16-word buffer.

37.4.3 DAC Status Register (DAC*x*_SR)

If DMA is enabled, the flags can be cleared automatically by DMA when the DMA request is done. Writing 0 to a field clears it whereas writing 1 has no effect. After reset, DACBFRPTF is set and can be cleared by software, if needed. The flags are set only when the data buffer status is changed.

NOTE

Do not use 32/16-bit accesses to this register.

Address: Base address + 20h offset

Bit	7	6	5	4	3	2	1	0
Read	0					DACBFWMF	DACBFRPTF	DACBFRPBF
Write								
Reset	0	0	0	0	0	0	1	0

DACx_SR field descriptions

Field	Description
7–3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
2 DACBFWMF	DAC Buffer Watermark Flag 0 The DAC buffer read pointer has not reached the watermark level. 1 The DAC buffer read pointer has reached the watermark level.
1 DACBFRPTF	DAC Buffer Read Pointer Top Position Flag 0 The DAC buffer read pointer is not zero. 1 The DAC buffer read pointer is zero.
0 DACBFRPBF	DAC Buffer Read Pointer Bottom Position Flag 0 The DAC buffer read pointer is not equal to C2[DACBFUP]. 1 The DAC buffer read pointer is equal to C2[DACBFUP].

37.4.4 DAC Control Register (DACx_C0)

NOTE

Do not use 32- or 16-bit accesses to this register.

Address: Base address + 21h offset

Bit	7	6	5	4	3	2	1	0
Read	DACEN	DACRFS	DACTRGSEL	0	LPEN	DACBWIEN	DACBTIEN	DACBBIEN
Write				DACSWTRG				
Reset	0	0	0	0	0	0	0	0

DACx_C0 field descriptions

Field	Description
7 DACEN	DAC Enable Starts the Programmable Reference Generator operation. 0 The DAC system is disabled. 1 The DAC system is enabled.
6 DACRFS	DAC Reference Select

Table continues on the next page...

DACx_C0 field descriptions (continued)

Field	Description
	0 The DAC selects DACREF_1 as the reference voltage. 1 The DAC selects DACREF_2 as the reference voltage.
5 DACTRGSEL	DAC Trigger Select 0 The DAC hardware trigger is selected. 1 The DAC software trigger is selected.
4 DACSWTRG	DAC Software Trigger Active high. This is a write-only field, which always reads 0. If DAC software trigger is selected and buffer is enabled, writing 1 to this field will advance the buffer read pointer once. 0 The DAC soft trigger is not valid. 1 The DAC soft trigger is valid.
3 LPEN	DAC Low Power Control **NOTE:** See the 12-bit DAC electrical characteristics of the device data sheet for details on the impact of the modes below. 0 High-Power mode 1 Low-Power mode
2 DACBWIEN	DAC Buffer Watermark Interrupt Enable 0 The DAC buffer watermark interrupt is disabled. 1 The DAC buffer watermark interrupt is enabled.
1 DACBTIEN	DAC Buffer Read Pointer Top Flag Interrupt Enable 0 The DAC buffer read pointer top flag interrupt is disabled. 1 The DAC buffer read pointer top flag interrupt is enabled.
0 DACBBIEN	DAC Buffer Read Pointer Bottom Flag Interrupt Enable 0 The DAC buffer read pointer bottom flag interrupt is disabled. 1 The DAC buffer read pointer bottom flag interrupt is enabled.

37.4.5 DAC Control Register 1 (DACx_C1)

NOTE

Do not use 32- or 16-bit accesses to this register.

Address: Base address + 22h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DMAEN	0		DACBFWM		DACBFMD		DACBFEN
Reset	0	0	0	0	0	0	0	0

DACx_C1 field descriptions

Field	Description
7 DMAEN	DMA Enable Select 0 DMA is disabled. 1 DMA is enabled. When DMA is enabled, the DMA request will be generated by original interrupts. The interrupts will not be presented on this module at the same time.
6–5 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
4–3 DACBFWM	DAC Buffer Watermark Select Controls when SR[DACBFWMF] is set. When the DAC buffer read pointer reaches the word defined by this field, which is 1–4 words away from the upper limit (DACBUP), SR[DACBFWMF] will be set. This allows user configuration of the watermark interrupt. 00 1 word 01 2 words 10 3 words 11 4 words
2–1 DACBFMD	DAC Buffer Work Mode Select 00 Normal mode 01 Swing mode 10 One-Time Scan mode 11 Reserved
0 DACBFEN	DAC Buffer Enable 0 Buffer read pointer is disabled. The converted data is always the first word of the buffer. 1 Buffer read pointer is enabled. The converted data is the word that the read pointer points to. It means converted data can be from any word of the buffer.

37.4.6 DAC Control Register 2 (DACx_C2)

Address: Base address + 23h offset

Bit	7	6	5	4	3	2	1	0
Read Write	DACBFRP				DACBFUP			
Reset	0	0	0	0	1	1	1	1

DACx_C2 field descriptions

Field	Description
7–4 DACBFRP	DAC Buffer Read Pointer Keeps the current value of the buffer read pointer.
DACBFUP	DAC Buffer Upper Limit Selects the upper limit of the DAC buffer. The buffer read pointer cannot exceed it.

DACx_C2 field descriptions (continued)

Field	Description

37.5 Functional description

The 12-bit DAC module can select one of the two reference inputs—DACREF_1 and DACREF_2 as the DAC reference voltage, V_{in} by C0 [DACRFS]. See the chip-specific DAC information to determine the source options for DACREF_1 and DACREF_2.

When the DAC is enabled, it converts the data in DACDAT0[11:0] or the data from the DAC data buffer to a stepped analog output voltage. The output voltage range is from V_{in} to V_{in}⁄4096, and the step is V_{in}⁄4096.

37.5.1 DAC data buffer operation

When the DAC is enabled and the buffer is not enabled, the DAC module always converts the data in DAT0 to the analog output voltage.

When both the DAC and the buffer are enabled, the DAC converts the data in the data buffer to analog output voltage. The data buffer read pointer advances to the next word whenever a hardware or software trigger event occurs.

The data buffer can be configured to operate in Normal mode, Swing mode, One-Time Scan mode. When the buffer operation is switched from one mode to another, the read pointer does not change. The read pointer can be set to any value between 0 and C2[DACBFUP] by writing C2[DACBFRP].

37.5.1.1 DAC data buffer interrupts

There are several interrupts and associated flags that can be configured for the DAC buffer. SR[DACBFRPBF] is set when the DAC buffer read pointer reaches the DAC buffer upper limit, that is, C2[DACBFRP] = C2[DACBFUP]. SR[DACBFRPTF] is set when the DAC read pointer is equal to the start position, 0. Finally, SR[DACBFWMF] is set when the DAC buffer read pointer has reached the position defined by C1[DACBFWM]. C1[DACBFWM] can be used to generate an interrupt when the DAC buffer read pointer is between 1 to 4 words from C2[DACBFUP].

37.5.1.2 Modes of DAC data buffer operation

The following table describes the different modes of data buffer operation for the DAC module.

Table 37-1. Modes of DAC data buffer operation

Modes	Description
Buffer Normal mode	This is the default mode. The buffer works as a circular buffer. The read pointer increases by one, every time the trigger occurs. When the read pointer reaches the upper limit, it goes to 0 directly in the next trigger event.
Buffer Swing mode	This mode is similar to the normal mode. However, when the read pointer reaches the upper limit, it does not go to 0. It will descend by 1 in the next trigger events until 0 is reached.
Buffer One-time Scan mode	The read pointer increases by 1 every time the trigger occurs. When it reaches the upper limit, it stops there. If read pointer is reset to the address other than the upper limit, it will increase to the upper address and stop there again. **NOTE:** If the software set the read pointer to the upper limit, the read pointer will not advance in this mode.

37.5.2 DMA operation

When DMA is enabled, DMA requests are generated instead of interrupt requests. The DMA Done signal clears the DMA request.

The status register flags are still set and are cleared automatically when the DMA completes.

37.5.3 Resets

During reset, the DAC is configured in the default mode and is disabled.

37.5.4 Low-Power mode operation

The following table shows the wait mode and the stop mode operation of the DAC module.

Table 37-2. Modes of operation

Modes of operation	Description
Wait mode	The DAC will operate normally, if enabled.

Table continues on the next page...

Table 37-2. Modes of operation (continued)

Modes of operation	Description
Stop mode	If enabled, the DAC module continues to operate in Normal Stop mode and the output voltage will hold the value before stop. In low-power stop modes, the DAC is fully shut down.

NOTE

The assignment of module modes to core modes is chip-specific. For module-to-core mode assignments, see the chapter that describes how modules are configured.