

3.7.4.1 VREF Overview

This device includes a voltage reference (VREF) to supply an accurate 1.2 V voltage output.

The voltage reference can provide a reference voltage to external peripherals or a reference to analog peripherals, such as the ADC, DAC, or CMP.

NOTE

PMC_REGSC[BGEN] bit must be set if the VREF regulator is required to remain operating in VLPx modes.

NOTE

For either an internal or external reference if the VREF_OUT functionality is being used, VREF_OUT signal must be connected to an output load capacitor. Refer the device data sheet for more details.

3.8 Timers

3.8.1 PDB Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

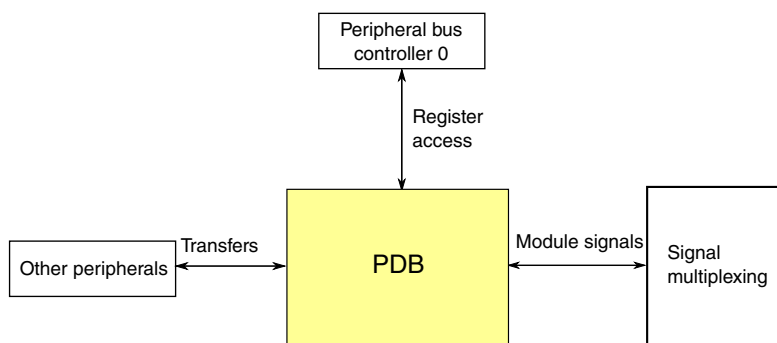


Figure 3-41. PDB configuration

Table 3-54. Reference links to related information

Topic	Related module	Reference
Full description	PDB	PDB
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.8.1.1 PDB Instantiation

3.8.1.1.1 PDB Output Triggers

Table 3-55. PDB output triggers

Number of PDB channels for ADC trigger	2
Number of pre-triggers per PDB channel	2
Number of DAC triggers	2
Number of Pulse Out	3

3.8.1.1.2 PDB Input Trigger Connections

Table 3-56. PDB Input Trigger Options

PDB Trigger	PDB Input
0000	External Trigger
0001	CMP 0
0010	CMP 1
0011	CMP 2
0100	PIT Ch 0 Output
0101	PIT Ch 1 Output

Table continues on the next page...

Table 3-56. PDB Input Trigger Options (continued)

PDB Trigger	PDB Input
0110	PIT Ch 2 Output
0111	PIT Ch 3 Output
1000	FTM0 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1001	FTM1 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1010	FTM2 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1011	FTM3 initialization trigger and channel triggers, as programmed in the FTM external trigger register (EXTTRIG)
1100	RTC Alarm
1101	RTC Seconds
1110	LPTMR Output
1111	Software Trigger

3.8.1.2 PDB Module Interconnections

PDB trigger outputs	Connection
Channel 0 triggers	ADC0 trigger
Channel 1 triggers	ADC1 trigger and synchronous input 1 of FTM0
DAC triggers	DAC0 and DAC1 trigger
Pulse-out	Pulse-out connected to each CMP module's sample/window input to control sample operation

3.8.1.3 Back-to-back acknowledgement connections

In this MCU, PDB back-to-back operation acknowledgment connections are implemented as follows:

- PDB channel 0 pre-trigger 0 acknowledgement input: ADC1SC1B_COCO
- PDB channel 0 pre-trigger 1 acknowledgement input: ADC0SC1A_COCO
- PDB channel 1 pre-trigger 0 acknowledgement input: ADC0SC1B_COCO
- PDB channel 1 pre-trigger 1 acknowledgement input: ADC1SC1A_COCO

So, the back-to-back chain is connected as a ring:

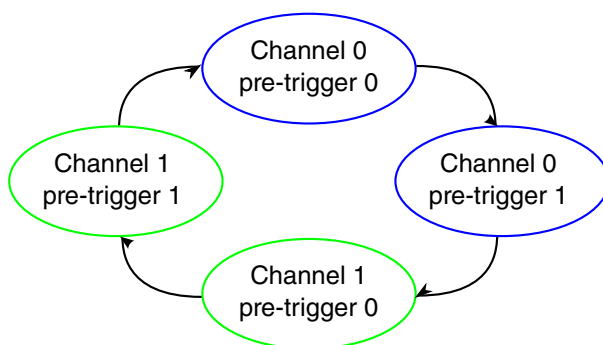


Figure 3-42. PDB back-to-back chain

The application code can set the `PDBx_CHnC1[BB]` bits to configure the PDB pre-triggers as a single chain or several chains.

3.8.1.4 PDB Interval Trigger Connections to DAC

In this MCU, PDB interval trigger connections to DAC are implemented as follows.

- PDB interval trigger 0 connects to DAC0 hardware trigger input.
- PDB interval trigger 1 connects to DAC1 hardware trigger input.

3.8.1.5 DAC External Trigger Input Connections

In this MCU, the following DAC external trigger inputs are implemented.

- DAC external trigger input 1: `ADC1SC1A_COCO`

NOTE

Application code can set the `PDBx_DACINTCn[EXT]` bit to allow DAC external trigger input when the corresponding ADC Conversion complete flag, `ADCx_SC1n[COCO]`, is set.

3.8.1.6 Pulse-Out Connection

Individual PDB Pulse-Out signals are connected to each CMP block and used for sample window.

3.8.1.7 Pulse-Out Enable Register Implementation

The following table shows the comparison of pulse-out enable register at the module and chip level.

Table 3-57. PDB pulse-out enable register

Register	Module implementation	Chip implementation
POnEN	7:0 - POEN 31:8 - Reserved	0 - POEN[0] for CMP0 1 - POEN[1] for CMP1 2 - POEN[2] for CMP2 31:3 - Reserved

3.8.2 FlexTimer Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module’s dedicated chapter.

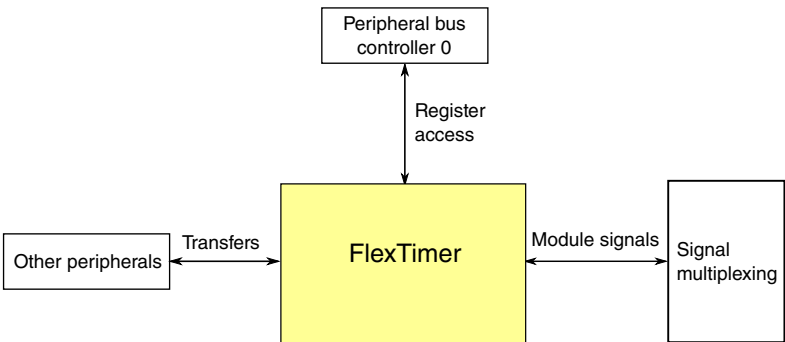


Figure 3-43. FlexTimer configuration

Table 3-58. Reference links to related information

Topic	Related module	Reference
Full description	FlexTimer	FlexTimer
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.8.2.1 Instantiation Information

This device contains four FlexTimer modules.

The following table shows how these modules are configured.

Table 3-59. FTM Instantiations

FTM instance	Number of channels	Features/usage
FTM0	8	3-phase motor + 2 general purpose or stepper motor
FTM1	2 ¹	Quadrature decoder or general purpose
FTM2	2 ¹	Quadrature decoder or general purpose
FTM3	8	3-phase motor + 2 general purpose or stepper motor

1. Only channels 0 and 1 are available.

Compared with the FTM0 and FTM3 configuration, the FTM1 and FTM2 configuration adds the Quadrature decoder feature and reduces the number of channels.

3.8.2.2 External Clock Options

By default each FTM is clocked by the internal bus clock (the FTM refers to it as system clock). Each module contains a register setting that allows the module to be clocked from an external clock instead. There are two external FTM_CLKINx pins that can be selected by any FTM module via the SIM_SOPT4 register.

3.8.2.3 Fixed frequency clock

The fixed frequency clock for each FTM is MCGFFCLK.

3.8.2.4 FTM Interrupts

The FlexTimer has multiple sources of interrupt. However, these sources are OR'd together to generate a single interrupt request per FTM module to the interrupt controller. When an FTM interrupt occurs, read the FTM status registers (FMS, SC, and STATUS) to determine the exact interrupt source.

3.8.2.5 FTM Fault Detection Inputs

The following fault detection input options for the FTM modules are selected via the SIM_SOPT4 register. The external pin option is selected by default.

- FTM0 FAULT0 = FTM0_FLT0 pin or CMP0 output

- FTM0 FAULT1 = FTM0_FLT1 pin or CMP1 output
- FTM0 FAULT2 = FTM0_FLT2 pin or CMP2 output
- FTM0 FAULT3 = FTM0_FLT3 pin
- FTM1 FAULT0 = FTM1_FLT0 pin or CMP0 output
- FTM1 FAULT1 = CMP1 output
- FTM1 FAULT2 = CMP2 output
- FTM2 FAULT0 = FTM2_FLT0 pin or CMP0 output
- FTM2 FAULT1 = CMP1 output
- FTM2 FAULT2 = CMP2 output
- FTM3 FAULT0 = FTM3_FLT0 pin or CMP0 output
- FTM3 FAULT1 = CMP2 output

3.8.2.6 FTM Hardware Triggers

The FTM synchronization hardware triggers are connected in the chip as follows:

- FTM0 hardware trigger 0 = CMP0 Output or FTM1 Match (when enabled in the FTM1 External Trigger (EXTTRIG) register)
- FTM0 hardware trigger 1 = PDB channel 1 Trigger Output or FTM2 Match (when enabled in the FTM2 External Trigger (EXTTRIG) register)
- FTM0 hardware trigger 2 = FTM0_FLT0 pin
- FTM1 hardware trigger 0 = CMP0 Output
- FTM1 hardware trigger 1 = CMP1 Output
- FTM1 hardware trigger 2 = FTM1_FLT0 pin

For the triggers with more than one option, SIM_SOPT4 controls the selection.

3.8.2.7 Input capture options for FTM module instances

The following channel 0 input capture source options are selected via SIM_SOPT4. The external pin option is selected by default.

- FTM1 channel 0 input capture = FTM1_CH0 pin or CMP0 output or CMP1 output or USB start of frame pulse
- FTM2 channel 0 input capture = FTM2_CH0 pin or CMP0 output or CMP1 output

NOTE

When the USB start of frame pulse option is selected as an FTM channel input capture, disable the USB SOF token

interrupt in the USB Interrupt Enable register (INTEN[SOFTOKEN]) to avoid USB enumeration conflicts.

3.8.2.8 FTM output triggers for other modules

FTM output triggers can be selected as input triggers for the PDB and ADC modules. See [PDB Instantiation](#) and [ADC triggers](#).

3.8.2.9 FTM Global Time Base

This chip provides the optional FTM global time base feature (see [Global time base \(GTB\)](#)).

FTM0 provides the only source for the FTM global time base. The other FTM modules can share the time base as shown in the following figure:

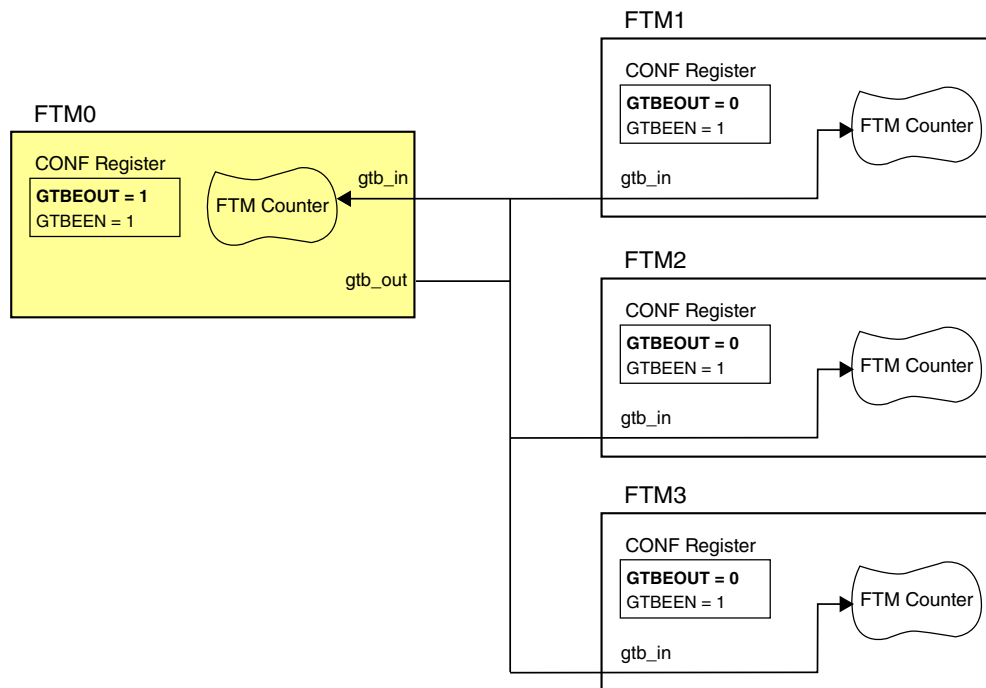


Figure 3-44. FTM Global Time Base Configuration

3.8.2.10 FTM BDM and debug halt mode

In the FTM chapter, references to the chip being in "BDM" are the same as the chip being in "debug halt mode".

3.8.2.11 FTM2 Base Addresses

FTM2 can be accessed through both AIPS0 and AIPS1. When accessed through AIPS0, the base address is 4003_A000h and when accessed through AIPS1, the base address is 400B_8000h.

3.8.2.12 FTM registers

FTM1 and FTM2 do not have the C2SC, C2V, C3SC, C3V, C4SC, C4V, C5SC, C5V, C6SC, C6V, C7SC, and C7V registers. FTM0 has these registers.

3.8.3 PIT Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module’s dedicated chapter.

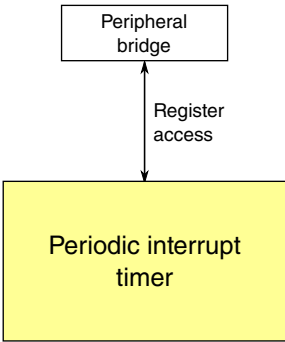


Figure 3-45. PIT configuration

Table 3-60. Reference links to related information

Topic	Related module	Reference
Full description	PIT	PIT
System memory map		System memory map
Clocking		Clock Distribution
Power management		Power management

3.8.3.1 PIT/DMA Periodic Trigger Assignments

The PIT generates periodic trigger events to the DMA Mux as shown in the table below.

Table 3-61. PIT channel assignments for periodic DMA triggering

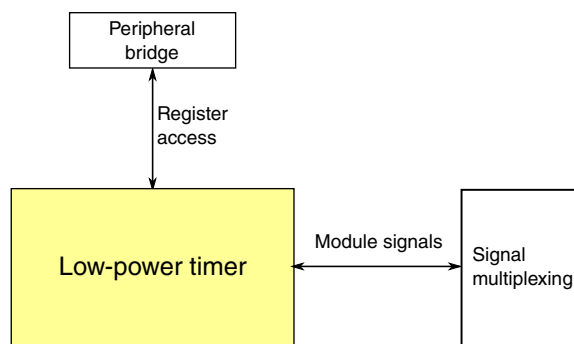
DMA Channel Number	PIT Channel
DMA Channel 0	PIT Channel 0
DMA Channel 1	PIT Channel 1
DMA Channel 2	PIT Channel 2
DMA Channel 3	PIT Channel 3

3.8.3.2 PIT/ADC Triggers

PIT triggers are selected as ADCx trigger sources using the SIM_SOPT7[ADCxTRGSEL] fields. For more details, refer to SIM chapter.

3.8.4 Low-power timer configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

**Figure 3-46. LPTMR configuration****Table 3-62. Reference links to related information**

Topic	Related module	Reference
Full description	Low-power timer	Low-power timer
System memory map		System memory map
Clocking		Clock Distribution
Power management		Power management
Signal Multiplexing	Port control	Signal Multiplexing

3.8.4.1 LPTMR prescaler/glitch filter clocking options

The prescaler and glitch filter of the LPTMR module can be clocked from one of four sources determined by the LPTMR0_PSR[PCS] bitfield. The following table shows the chip-specific clock assignments for this bitfield.

NOTE

The chosen clock must remain enabled if the LPTMR is to continue operating in all required low-power modes.

LPTMR0_PSR[PCS]	Prescaler/glitch filter clock number	Chip clock
00	0	MCGIRCLK — internal reference clock (not available in VLPS/LLS/VLLS modes)
01	1	LPO — 1 kHz clock (not available in VLLS0 mode)
10	2	ERCLK32K — secondary external reference clock
11	3	OSCERCLK — external reference clock (not available in VLLS0 mode)

See [Clock Distribution](#) for more details on these clocks.

3.8.4.2 LPTMR pulse counter input options

The LPTMR_CSR[TPS] bitfield configures the input source used in pulse counter mode. The following table shows the chip-specific input assignments for this bitfield.

LPTMR_CSR[TPS]	Pulse counter input number	Chip input
00	0	CMP0 output
01	1	LPTMR_ALT1 pin
10	2	LPTMR_ALT2 pin
11	3	Reserved

3.8.5 CMT Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

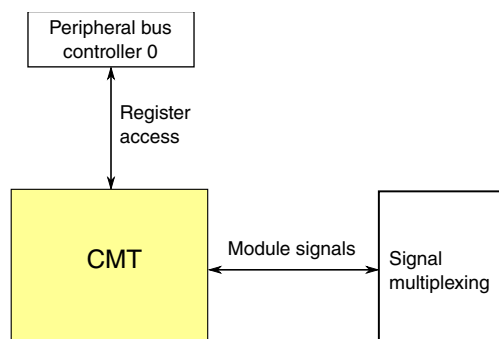


Figure 3-47. CMT configuration

Table 3-63. Reference links to related information

Topic	Related module	Reference
Full description	Carrier modulator transmitter (CMT)	CMT
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.8.5.1 Instantiation Information

This device contains one CMT module.

3.8.5.2 IRO Drive Strength

The IRO pad requires higher current drive than can be obtained from a single pad. For this device, the pin associated with the CMT_IRO signal is doubled bonded to two pads.

SIM_SOPT2[PTD7PAD] can be used to configure the pin associated with the CMT_IRO signal as a higher current output port pin.

3.8.6 RTC configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

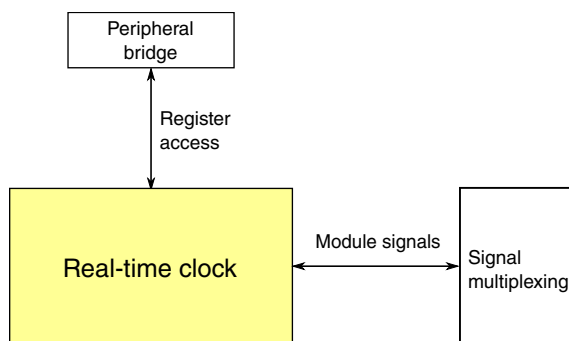


Figure 3-48. RTC configuration

Table 3-64. Reference links to related information

Topic	Related module	Reference
Full description	RTC	RTC
System memory map		System memory map
Clocking		Clock Distribution
Power management		Power management

3.8.6.1 RTC_CLKOUT signal

When the RTC is enabled and the port control module selects the RTC_CLKOUT function, the RTC_CLKOUT signal outputs a 1 Hz or 32 kHz output derived from RTC oscillator as shown below.

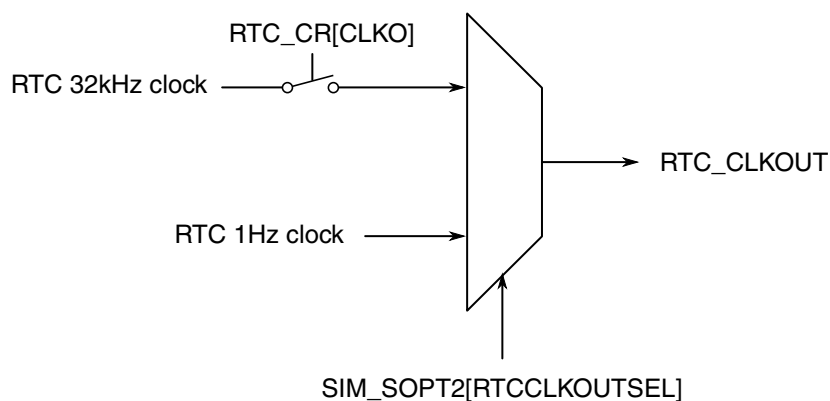


Figure 3-49. RTC_CLKOUT generation

3.9 Communication interfaces