3.6.3 RNG Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

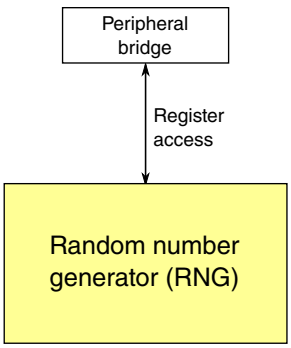

Figure 3-34. RNG configuration

Table 3-47. Reference links to related information

Topic	Related module	Reference
Full description	RNG	RNG
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management

3.6.3.1 RNGA Base Addresses

RNGA can be accessed through both AIPS0 and AIPS1. When accessed through AIPS0, the base address is 4002_9000h and when accessed through AIPS1, the base address is 400A_0000h.

3.7 Analog

3.7.1 16-bit SAR ADC Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

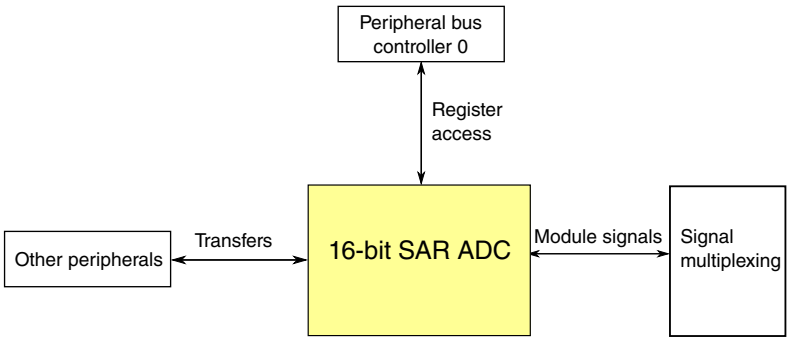

Figure 3-35. 16-bit SAR ADC configuration

Table 3-48. Reference links to related information

Topic	Related module	Reference
Full description	16-bit SAR ADC	16-bit SAR ADC
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.7.1.1 ADC instantiation information

This device contains two ADCs.

3.7.1.1.1 Number of ADC channels

The number of ADC channels present on the device is determined by the pinout of the specific device package. For details regarding the number of ADC channel available on a particular package, refer to the signal multiplexing chapter of this MCU.

3.7.1.2 DMA Support on ADC

Applications may require continuous sampling of the ADC (4K samples/sec) that may have considerable load on the CPU. Though using PDB to trigger ADC may reduce some CPU load, the ADC supports DMA request functionality for higher performance when the ADC is sampled at a very high rate or cases where PDB is bypassed. The ADC can trigger the DMA (via DMA req) on conversion completion.

3.7.1.3 Connections/channel assignment

3.7.1.3.1 ADC0 Connections/Channel Assignment

NOTE

As indicated by the following sections, each ADCx_DPx input and certain ADCx_DMx inputs may operate as single-ended ADC channels in single-ended mode.

3.7.1.3.1.1 ADC0 Channel Assignment for 144-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC0_DP0 and ADC0_DM0[1]	ADC0_DP0[2]
00001	DAD1	ADC0_DP1 and ADC0_DM1[3]	ADC0_DP1
00010	DAD2	ADC0_DP2 and ADC0_DM2	ADC0_DP2
00011	DAD3	ADC0_DP3 and ADC0_DM3[4]	ADC0_DP3[5]
00100[6]	AD4a	Reserved	Reserved
00101[6]	AD5a	Reserved	Reserved
00110[6]	AD6a	Reserved	Reserved
00111[6]	AD7a	Reserved	Reserved
00100[6]	AD4b	Reserved	ADC0_SE4b
00101[6]	AD5b	Reserved	ADC0_SE5b
00110[6]	AD6b	Reserved	ADC0_SE6b
00111[6]	AD7b	Reserved	ADC0_SE7b
01000	AD8	Reserved	ADC0_SE8[7]
01001	AD9	Reserved	ADC0_SE9[8]
01010	AD10	Reserved	ADC0_SE10
01011	AD11	Reserved	ADC0_SE11
01100	AD12	Reserved	ADC0_SE12
01101	AD13	Reserved	ADC0_SE13
01110	AD14	Reserved	ADC0_SE14
01111	AD15	Reserved	ADC0_SE15
10000	AD16	Reserved	ADC0_SE16
10001	AD17	Reserved	ADC0_SE17
10010	AD18	Reserved	ADC0_SE18
10011	AD19	Reserved	ADC0_DM0[9]
10100	AD20	Reserved	ADC0_DM1
10101	AD21	Reserved	ADC0_SE21
10110	AD22	Reserved	ADC0_SE22
10111	AD23	Reserved	12-bit DAC0 Output/ ADC0_SE23
11000	AD24	Reserved	Reserved

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[10]	Bandgap (S.E)[10]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC1_DP3 and ADC1_DM3
2. Interleaved with ADC1_DP3
3. Interleaved with ADC0_DP2 and ADC1_SE6a
4. Interleaved with ADC1_DP0 and ADC1_DM0
5. Interleaved with ADC1_DP0
6. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
7. Interleaved with ADC1_SE8
8. Interleaved with ADC1_SE9
9. Interleaved with ADC1_DM3
10. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.3.1.2 ADC0 Channel Assignment for 121-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC0_DP0 and ADC0_DM0[1]	ADC0_DP0[2]
00001	DAD1	ADC0_DP1 and ADC0_DM1	ADC0_DP1
00010	DAD2	ADC0_DP2 and ADC0_DM2	ADC0_DP2
00011	DAD3	ADC0_DP3 and ADC0_DM3[3]	ADC0_DP3[4]
00100[5]	AD4a	Reserved	Reserved
00101[5]	AD5a	Reserved	Reserved
00110[5]	AD6a	Reserved	Reserved
00111[5]	AD7a	Reserved	Reserved
00100[5]	AD4b	Reserved	ADC0_SE4b
00101[5]	AD5b	Reserved	ADC0_SE5b
00110[5]	AD6b	Reserved	ADC0_SE6b
00111[5] >	AD7b	Reserved	ADC0_SE7b
01000	AD8	Reserved	ADC0_SE8[6]
01001	AD9	Reserved	ADC0_SE9[7]
01010	AD10	Reserved	Reserved
01011	AD11	Reserved	Reserved
01100	AD12	Reserved	ADC0_SE12
01101	AD13	Reserved	ADC0_SE13

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
01110	AD14	Reserved	ADC0_SE14
01111	AD15	Reserved	ADC0_SE15
10000	AD16	Reserved	ADC0_SE16
10001	AD17	Reserved	ADC0_SE17
10010	AD18	Reserved	ADC0_SE18
10011	AD19	Reserved	ADC0_DM0[8]
10100	AD20	Reserved	ADC0_DM1
10101	AD21	Reserved	ADC0_SE21
10110	AD22	Reserved	ADC0_SE22
10111	AD23	Reserved	12-bit DAC0 Output/ ADC0_SE23
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[9]	Bandgap (S.E)[9]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC1_DP3 and ADC1_DM3
2. Interleaved with ADC1_DP3
3. Interleaved with ADC1_DP0 and ADC1_DM0
4. Interleaved with ADC1_DP0
5. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
6. Interleaved with ADC1_SE8
7. Interleaved with ADC1_SE9
8. Interleaved with ADC1_DM3
9. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.3.1.3 ADC0 Channel Assignment for 100-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC0_DP0 and ADC0_DM0[1]	ADC0_DP0[2]
00001	DAD1	ADC0_DP1 and ADC0_DM1	ADC0_DP1
00010	DAD2	ADC0_DP2 and ADC0_DM2	ADC0_DP2
00011	DAD3	ADC0_DP3 and ADC0_DM3[3]	ADC0_DP3[4]
00100[5]	AD4a	Reserved	Reserved
00101[5]	AD5a	Reserved	Reserved
00110[5]	AD6a	Reserved	Reserved

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00111[5]	AD7a	Reserved	Reserved
00100[5]	AD4b	Reserved	ADC0_SE4b
00101[5]	AD5b	Reserved	ADC0_SE5b
00110[5]	AD6b	Reserved	ADC0_SE6b
00111[5]	AD7b	Reserved	ADC0_SE7b
01000	AD8	Reserved	ADC0_SE8[6]
01001	AD9	Reserved	ADC0_SE9[7]
01010	AD10	Reserved	Reserved
01011	AD11	Reserved	Reserved
01100	AD12	Reserved	ADC0_SE12
01101	AD13	Reserved	ADC0_SE13
01110	AD14	Reserved	ADC0_SE14
01111	AD15	Reserved	ADC0_SE15
10000	AD16	Reserved	Reserved
10001	AD17	Reserved	ADC0_SE17
10010	AD18	Reserved	ADC0_SE18
10011	AD19	Reserved	ADC0_DM0[8]
10100	AD20	Reserved	ADC0_DM1
10101	AD21	Reserved	Reserved
10110	AD22	Reserved	Reserved
10111	AD23	Reserved	12-bit DAC0 Output/ ADC0_SE23
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[9]	Bandgap (S.E)[9]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC1_DP3 and ADC1_DM3
2. Interleaved with ADC1_DP3
3. Interleaved with ADC1_DP0 and ADC1_DM0
4. Interleaved with ADC1_DP0
5. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
6. Interleaved with ADC1_SE8
7. Interleaved with ADC1_SE9
8. Interleaved with ADC1_DM3
9. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.3.2 ADC1 Connections/Channel Assignment

NOTE

As indicated in the following tables, each ADCx_DPx input and certain ADCx_DMx inputs may operate as single-ended ADC channels in single-ended mode.

3.7.1.3.2.1 ADC1 Channel Assignment for 144-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC1_DP0 and ADC1_DM0[1]	ADC1_DP0[2]
00001	DAD1	ADC1_DP1 and ADC1_DM1	ADC1_DP1
00010	DAD2	Reserved	Reserved
00011	DAD3	ADC1_DP3 and ADC1_DM3[3]	ADC1_DP3[4]>
00100[5]	AD4a	Reserved	ADC1_SE4a
00101[5]	AD5a	Reserved	ADC1_SE5a
00110[5]	AD6a	Reserved	ADC1_SE6a
00111[5]	AD7a	Reserved	ADC1_SE7a
00100[5]	AD4b	Reserved	ADC1_SE4b
00101[5]	AD5b	Reserved	ADC1_SE5b
00110[5]	AD6b	Reserved	ADC1_SE6b
00111[5]	AD7b	Reserved	ADC1_SE7b
01000	AD8	Reserved	ADC1_SE8[6]
01001	AD9	Reserved	ADC1_SE9[7]
01010	AD10	Reserved	ADC1_SE10
01011	AD11	Reserved	ADC1_SE11
01100	AD12	Reserved	ADC1_SE12
01101	AD13	Reserved	ADC1_SE13
01110	AD14	Reserved	ADC1_SE14
01111	AD15	Reserved	ADC1_SE15
10000	AD16	Reserved	ADC1_SE16
10001	AD17	Reserved	ADC1_SE17
10010	AD18	Reserved	VREF Output/ADC1_SE18
10011	AD19	Reserved	ADC1_DM0[8]
10100	AD20	Reserved	ADC1_DM1
10101	AD21	Reserved	Reserved
10110	AD22	Reserved	Reserved
10111	AD23	Reserved	12-bit DAC1 Output/ ADC1_SE23
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[9]	Bandgap (S.E)[9]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC0_DP3 and ADC0_DM3
2. Interleaved with ADC0_DP3
3. Interleaved with ADC0_DP0 and ADC0_DM0
4. Interleaved with ADC0_DP0
5. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
6. Interleaved with ADC0_SE8
7. Interleaved with ADC0_SE9
8. Interleaved with ADC0_DM3
9. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.3.2.2 ADC1 Channel Assignment for 121-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC1_DP0 and ADC1_DM0[1]	ADC1_DP0[2]
00001	DAD1	ADC1_DP1 and ADC1_DM1	ADC1_DP1
00010	DAD2	Reserved	Reserved
00011	DAD3	ADC1_DP3 and ADC1_DM3[3]	ADC1_DP3[4]
00100[5]	AD4a	Reserved	ADC1_SE4a
00101[5]	AD5a	Reserved	ADC1_SE5a
00110[5]	AD6a	Reserved	ADC1_SE6a
00111[5]	AD7a	Reserved	ADC1_SE7a
00100[5]	AD4b	Reserved	ADC1_SE4b
00101[5]	AD5b	Reserved	ADC1_SE5b
00110[5]	AD6b	Reserved	ADC1_SE6b
00111[5]	AD7b	Reserved	ADC1_SE7b
01000	AD8	Reserved	ADC1_SE8[6]
01001	AD9	Reserved	ADC1_SE9[7]
01010	AD10	Reserved	Reserved
01011	AD11	Reserved	Reserved
01100	AD12	Reserved	ADC1_SE12
01101	AD13	Reserved	ADC1_SE13
01110	AD14	Reserved	ADC1_SE14

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
01111	AD15	Reserved	ADC1_SE15
10000	AD16	Reserved	ADC1_SE16
10001	AD17	Reserved	ADC1_SE17
10010	AD18	Reserved	VREF Output/ADC1_SE18
10011	AD19	Reserved	ADC1_DM0[8]
10100	AD20	Reserved	ADC1_DM1
10101	AD21	Reserved	Reserved
10110	AD22	Reserved	Reserved
10111	AD23	Reserved	12-bit DAC1 Output/ ADC1_SE23
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[9]	Bandgap (S.E)[9]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC0_DP3 and ADC0_DM3
2. Interleaved with ADC0_DP3
3. Interleaved with ADC0_DP0 and ADC0_DM0
4. Interleaved with ADC0_DP0
5. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
6. Interleaved with ADC0_SE8
7. Interleaved with ADC0_SE9
8. Interleaved with ADC0_DM3
9. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.3.2.3 ADC1 Channel Assignment for 100-Pin Package

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00000	DAD0	ADC1_DP0 and ADC1_DM0[1]	ADC1_DP0[2]
00001	DAD1	ADC1_DP1 and ADC1_DM1	ADC1_DP1
00010	DAD2	Reserved	Reserved
00011	DAD3	ADC1_DP3 and ADC1_DM3[3]	ADC1_DP3[4]
00100[5]	AD4a	Reserved	ADC1_SE4a
00101[5]	AD5a	Reserved	ADC1_SE5a
00110[5]	AD6a	Reserved	ADC1_SE6a
00111[5]	AD7a	Reserved	ADC1_SE7a

Table continues on the next page...

ADC Channel (SC1n[ADCH])	Channel	Input signal (SC1n[DIFF]= 1)	Input signal (SC1n[DIFF]= 0)
00100[5]	AD4b	Reserved	ADC1_SE4b
00101[5]	AD5b	Reserved	ADC1_SE5b
00110[5]	AD6b	Reserved	ADC1_SE6b
00111[5]	AD7b	Reserved	ADC1_SE7b
01000	AD8	Reserved	ADC1_SE8[6]
01001	AD9	Reserved	ADC1_SE9[7]
01010	AD10	Reserved	Reserved
01011	AD11	Reserved	Reserved
01100	AD12	Reserved	Reserved
01101	AD13	Reserved	Reserved
01110	AD14	Reserved	ADC1_SE14
01111	AD15	Reserved	ADC1_SE15
10000	AD16	Reserved	Reserved
10001	AD17	Reserved	ADC1_SE17
10010	AD18	Reserved	VREF Output/ADC1_SE18
10011	AD19	Reserved	ADC1_DM0[8]
10100	AD20	Reserved	ADC1_DM1
10101	AD21	Reserved	Reserved
10110	AD22	Reserved	Reserved
10111	AD23	Reserved	Reserved
11000	AD24	Reserved	Reserved
11001	AD25	Reserved	Reserved
11010	AD26	Temperature Sensor (Diff)	Temperature Sensor (S.E)
11011	AD27	Bandgap (Diff)[9]	Bandgap (S.E)[9]
11100	AD28	Reserved	Reserved
11101	AD29	-VREFH (Diff)	VREFH (S.E)
11110	AD30	Reserved	VREFL
11111	AD31	Module Disabled	Module Disabled

1. Interleaved with ADC0_DP3 and ADC0_DM3
2. Interleaved with ADC0_DP3
3. Interleaved with ADC0_DP0 and ADC0_DM0
4. Interleaved with ADC0_DP0
5. ADCx_CFG2[MUXSEL] bit selects between ADCx_SEn channels a and b. Refer to MUXSEL description in ADC chapter for details.
6. Interleaved with ADC0_SE8
7. Interleaved with ADC0_SE9
8. Interleaved with ADC0_DM3
9. This is the PMC bandgap 1V reference voltage not the VREF module 1.2 V reference voltage. Prior to reading from this ADC channel, ensure that you enable the bandgap buffer by setting the PMC_REGSC[BGBE] bit. Refer to the device data sheet for the bandgap voltage (V_{BG}) specification.

3.7.1.4 ADC Channels MUX Selection

The following figure shows the assignment of ADCx_SEn channels a and b through a MUX selection to ADC. To select between alternate set of channels, refer to ADCx_CFG2[MUXSEL] bit settings for more details.

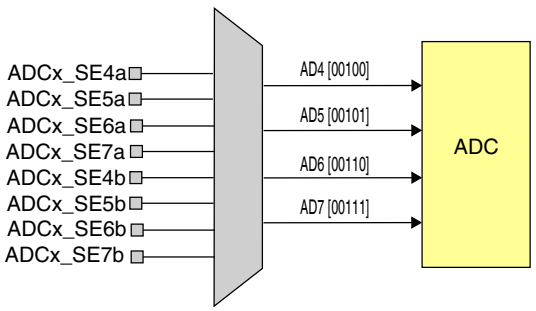

Figure 3-36. ADCx_SEn channels a and b selection

3.7.1.5 ADC Hardware Interleaved Channels

The AD8 and AD9 channels on ADCx are interleaved in hardware using the following configuration.

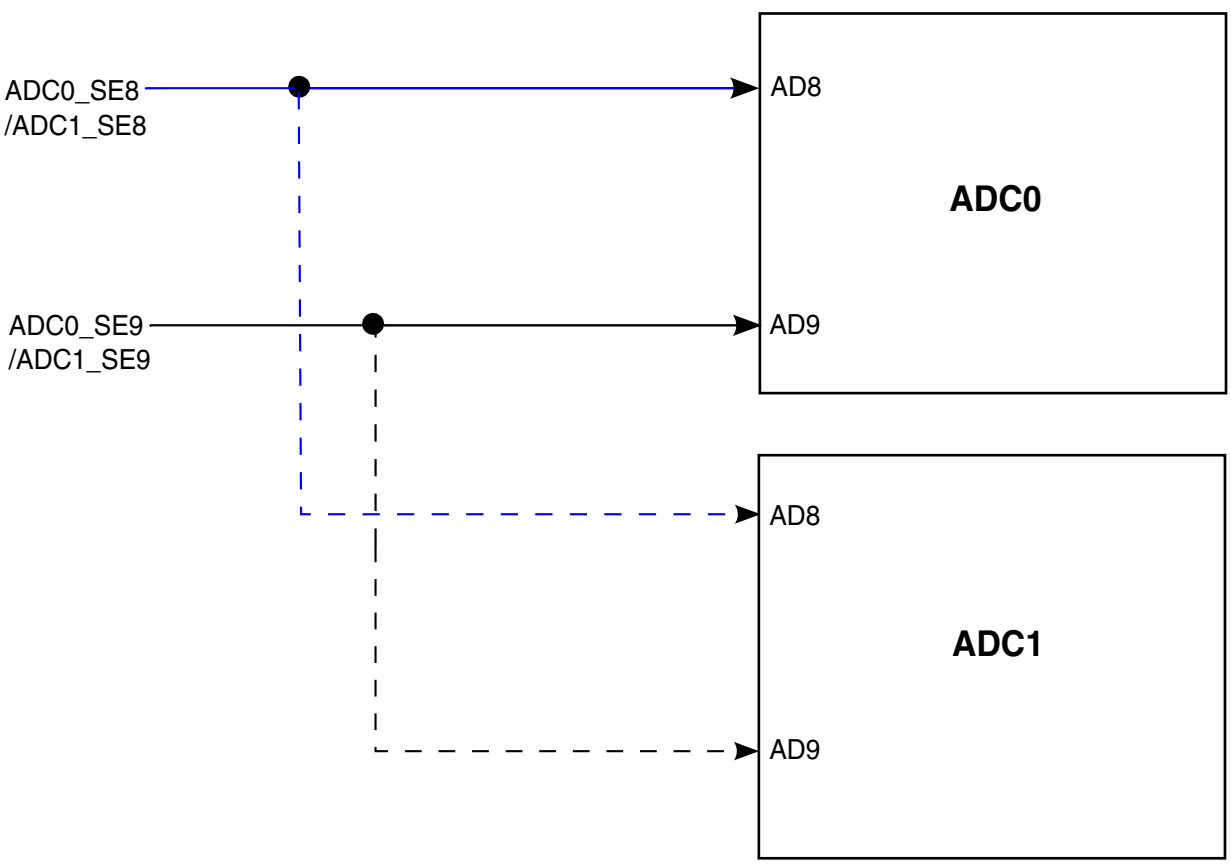

Figure 3-37. ADC hardware interleaved channels integration

3.7.1.6 ADC Reference Options

The ADC supports the following references:

- VREFH/VREFL - connected as the primary reference option
- 1.2 V VREF_OUT - connected as the V_{ALT} reference option

ADCx_SC2[REFSEL] bit selects the voltage reference sources for ADC. Refer to REFSEL description in ADC chapter for more details.

3.7.1.7 ADC triggers

The ADC supports both software and hardware triggers. The primary hardware mechanism for triggering the ADC is the PDB. The PDB itself can be triggered by other peripherals. For example: RTC (Alarm, Seconds) signal is connected to the PDB. The PDB input trigger can receive the RTC (alarm/seconds) trigger forcing ADC conversions in run mode (where PDB is enabled). On the other hand, the ADC can conduct conversions in low power modes, not triggered by PDB. This allows the ADC to do conversions in low power mode and store the output in the result register. The ADC generates interrupt when the data is ready in the result register that wakes the system from low power mode. The PDB can also be bypassed by using the ADCxTRGSEL bits in the SIM_SOPT7 register.

For operation of triggers in different modes, refer to Power Management chapter.

3.7.1.8 Alternate clock

For this device, the alternate clock is connected to OSCERCLK.

NOTE

This clock option is only usable when OSCERCLK is in the MHz range. A system with OSCERCLK in the kHz range has the optional clock source below minimum ADC clock operating frequency.

3.7.1.9 ADC low-power modes

This table shows the ADC low-power modes and the corresponding chip low-power modes.

Table 3-49. ADC low-power modes

Module mode	Chip mode
Wait	Wait, VLPW
Normal Stop	Stop, VLPS
Low Power Stop	LLS, VLLS3, VLLS2, VLLS1, VLLS0

3.7.2 CMP Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

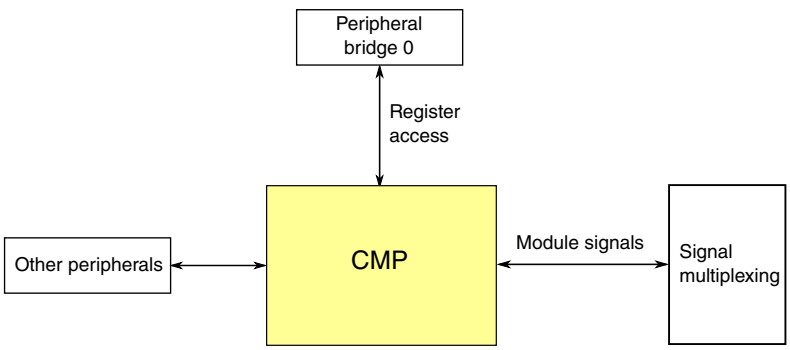

Figure 3-38. CMP configuration

Table 3-50. Reference links to related information

Topic	Related module	Reference
Full description	Comparator (CMP)	Comparator
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.7.2.1 CMP input connections

The following table shows the fixed internal connections to the CMP.

Table 3-51. CMP input connections

CMP Inputs	CMP0	CMP1	CMP2
IN0	CMP0_IN0	CMP1_IN0	CMP2_IN0
IN1	CMP0_IN1	CMP1_IN1	CMP2_IN1

Table continues on the next page...

Table 3-51. CMP input connections (continued)

CMP Inputs	CMP0	CMP1	CMP2
IN2	CMP0_IN2	ADC0_SE16/CMP1_IN2[1]	ADC1_SE16/CMP2_IN2[1]
IN3	CMP0_IN3	12-bit DAC0_OUT/CMP1_IN3	12-bit DAC1_OUT/ CMP2_IN3[1]
IN4	12-bit DAC1_OUT/CMP0_IN4	—	—
IN5	VREF Output/CMP0_IN5	VREF Output/CMP1_IN5	—
IN6	Bandgap	Bandgap	Bandgap
IN7	6b DAC0 Reference	6b DAC1 Reference	—

1. Reserved on the 100 LQFP package.

3.7.2.2 CMP external references

The 6-bit DAC sub-block supports selection of two references. For this device, the references are connected as follows:

- VREF_OUT - V_{in1} input
- VDD - V_{in2} input

3.7.2.3 External window/sample input

Individual PDB pulse-out signals control each CMP Sample/Window timing.

3.7.3 12-bit DAC Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

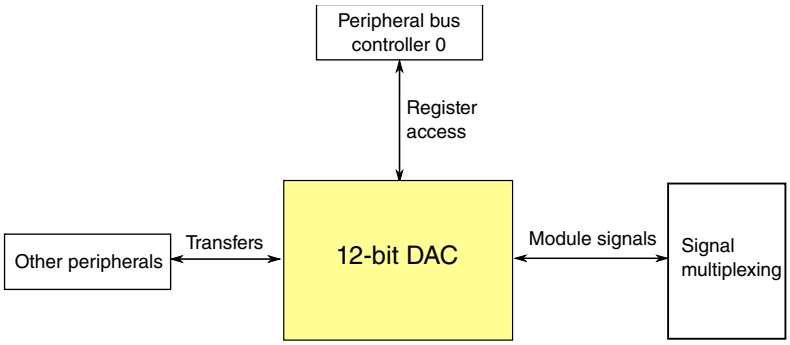

Figure 3-39. 12-bit DAC configuration

Table 3-52. Reference links to related information

Topic	Related module	Reference
Full description	12-bit DAC	12-bit DAC
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.7.3.1 12-bit DAC Overview

This device contains two 12-bit digital-to-analog converters (DAC) with programmable reference generator output. The DAC includes a FIFO for DMA support.

3.7.3.2 12-bit DAC instantiation

In this chip, the 100-pin package has 1 DAC module. The 121-pin and 144-pin packages have 2 DAC modules.

3.7.3.3 12-bit DAC Output

The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.

3.7.3.4 12-bit DAC Reference

For this device VREF_OUT and VDDA are selectable as the DAC reference. VREF_OUT is connected to the DACREF_1 input and VDDA is connected to the DACREF_2 input. Use DACx_C0[DACRFS] control bit to select between these two options.

Be aware that if the DAC and ADC use the VREF_OUT reference simultaneously, some degradation of ADC accuracy is to be expected due to DAC switching.

3.7.3.5 DAC0 Base Addresses

DAC0 can be accessed through both AIPS0 and AIPS1. When accessed through AIPS0, the base address is 4003_F000h and when accessed through AIPS1, the base address is 400C_C000h.

3.7.4 VREF Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.

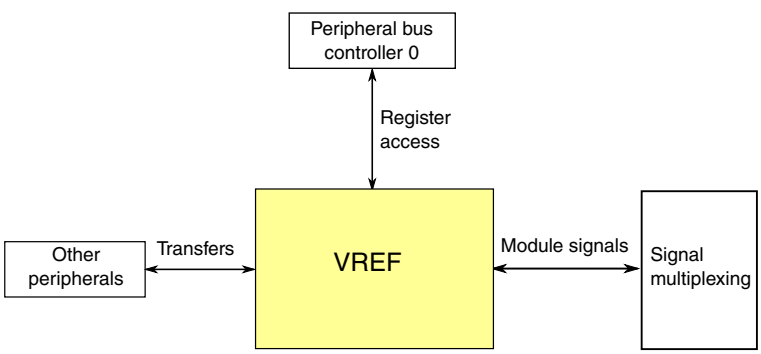

Figure 3-40. VREF configuration

Table 3-53. Reference links to related information

Topic	Related module	Reference
Full description	VREF	VREF
System memory map		System memory map
Clocking		Clock distribution
Power management		Power management
Signal multiplexing	Port control	Signal multiplexing

3.7.4.1 VREF Overview

This device includes a voltage reference (VREF) to supply an accurate 1.2 V voltage output.

The voltage reference can provide a reference voltage to external peripherals or a reference to analog peripherals, such as the ADC, DAC, or CMP.

NOTE

PMC_REGSC[BGEN] bit must be set if the VREF regulator is required to remain operating in VLPx modes.

NOTE

For either an internal or external reference if the VREF_OUT functionality is being used, VREF_OUT signal must be connected to an output load capacitor. Refer the device data sheet for more details.

3.8 Timers

3.8.1 PDB Configuration

This section summarizes how the module has been configured in the chip. For a comprehensive description of the module itself, see the module's dedicated chapter.