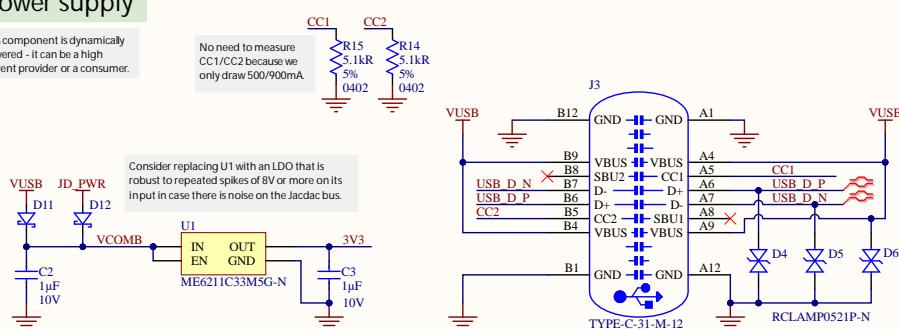


Power supply

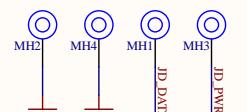
This component is dynamically powered - it can be a high current provider or a consumer.

No need to measure CC1/CC2 because we only draw 500/900mA



Consider replacing U1 with an LDO that is robust to repeated spikes of 8V or more on its input in case there is noise on the Jadcac bus.

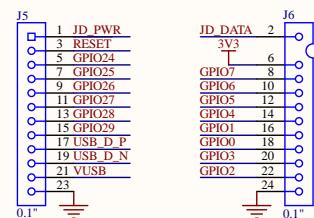
Mounting & expansion holes



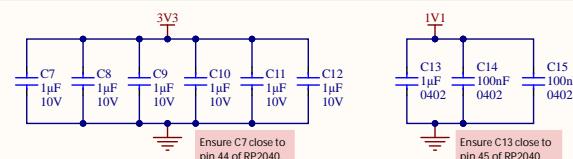
Mounting holes are electrically connected to the Jadcac bus nets so they can be used as part of the PCB edge connector. Use the following reference designators and net mapping:

- MH1: JD_DATA
- MH2 & MH4: JD_PWR
- MH3: JD_PWR

This design uses the Jadcac EC30 spec, see <https://aka.ms/jadcac-ec30>.

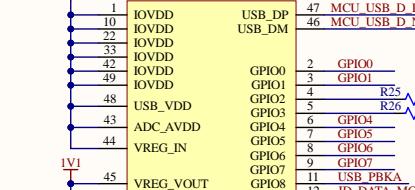


MCU



Ensure C7 close to pin 44 of RP2040.

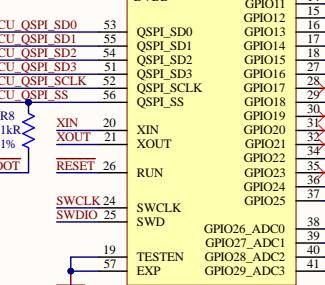
Ensure C13 close to pin 45 of RP2040.



Ensure R3 and R4 are close to RP2040.

R25/26 optional source termination for SPI, but RP2040 current and slew rate limiting sufficient for many applications.

JD_DATA_MCU uses PIO.



R8 1kR 1% is connected to XIN/XOUT.

RESET 26

SWCLK 24

SWDO 25

XIN 20

XIN 21

XOUT 21

XOUT 21

RESET 26

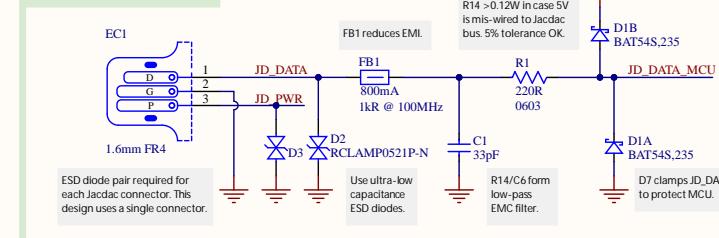
SWCLK 24

SWDO 25

TESTEN 19

EXP 57

Jadcac interface



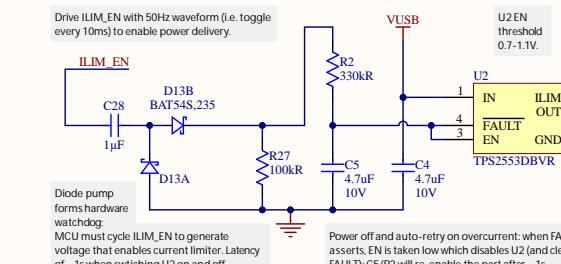
EC1 is a 1.6mm FR4 connector.

ESD diode pair required for each Jadcac connector. This design uses a single connector.

FB1 reduces EMI.

R14 > 0.12W in case 5V is mis-wired to Jadcac bus. 5% tolerance OK.

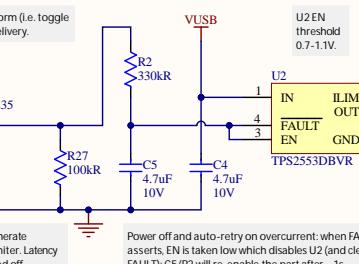
Power provision



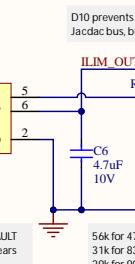
Drive ILIM_EN with 50Hz waveform (i.e. toggle every 10ms) to enable power delivery.

Diode pump forms hardware watchdog.

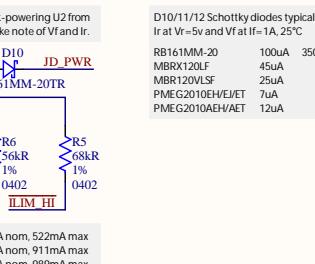
MCU must cycle ILIM_EN to generate voltage that enables current limiter. Latency ~ 1s when switching U2 on and off.



Power off and auto-retry on overcurrent: when FAULT asserts, EN is taken low which disables U2 (and clears FAULT); C5/R2 will re-enable the part after ~1s.



D10 prevents back-powering U2 from Jadcac bus, but take note of Vf and Irf.



D10/11/12 Schottky diodes typical. Irf at Vr=5v and Vf at If=1A, 25°C.

RB161MM-20 100μA 350mV

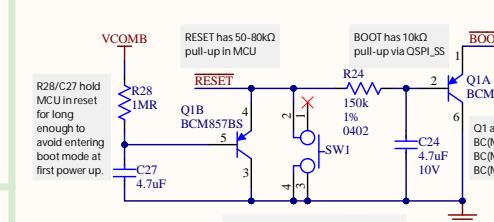
MBR120LF 45μA

MBR120LVS 25μA

PMEG2010FH/E/ET 7μA

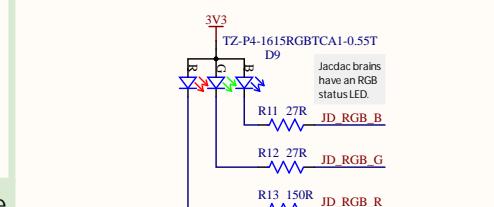
PMEG2010AEH/AET 12μA

Status LEDs & reset/boot button



R28/C27 hold MCU in reset for long enough to avoid entering boot mode at first power up.

short press or power-up: reset long (>2s) press: bootloader



Q1 alternatives: BC(M)857BS, BC(M)857DS, BC(M)856BS

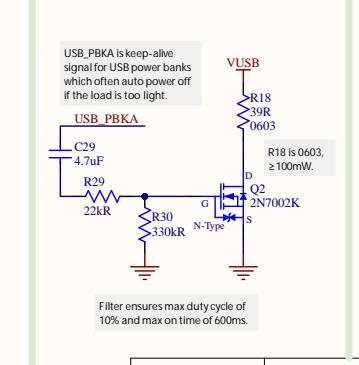
Jadcac brains have an RGB status LED.

R11 27R JD_RGB_B

R12 27R JD_RGB_G

R13 150R JD_RGB_R

USB power bank keep-alive



USB_PBKA is keep-alive signal for USB power banks which often auto power off if the load is too light.

R18 is 0603, ≥100mW.

R16 supports brighter 'blink' to indicate high current power delivery.

R17 56kR 0402

R16 33kR 0402

PD_STATUS

Everlight 19-217/GHC-YR1S2/3T works with tiny currents! Ensure D10/11/12 reverse leakage doesn't light it up.

This reference design is a guideline. Please refer to the Jadcac docs online at <https://aka.ms/jadcac> for the definitive and most up-to-date information.

Silkscreen should include text to identify the module type and revision, and optionally a QR code.

This design uses an EC30 board shape.

Silkscreen / layout notes

Block name

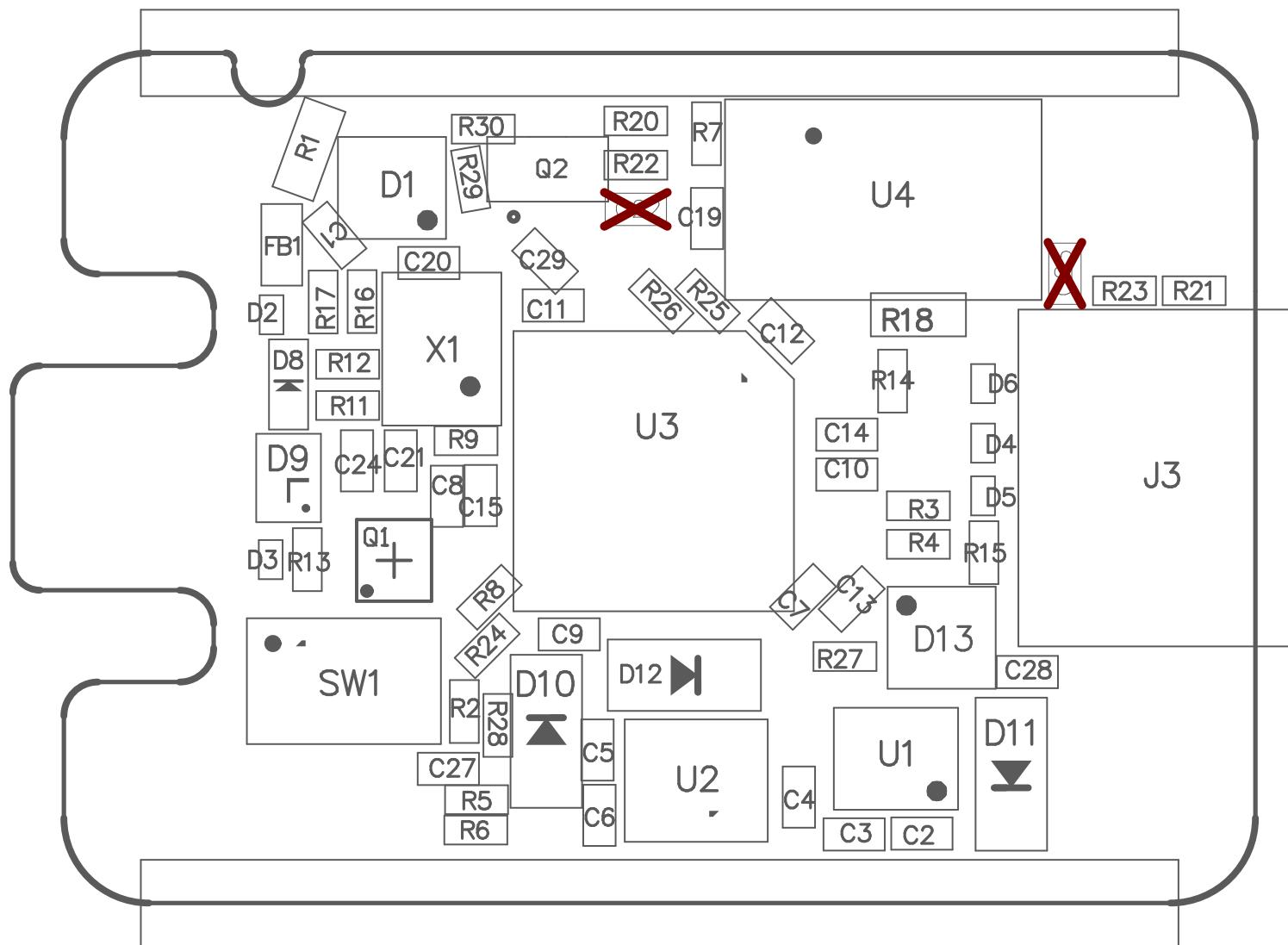
Design notes

This information is provided "as-is". You bear the risk of using it. Some information relates to pre-release specification which may change without notice. Microsoft makes no warranties, express or implied, with respect to the information provided here.

When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.

Board Outline

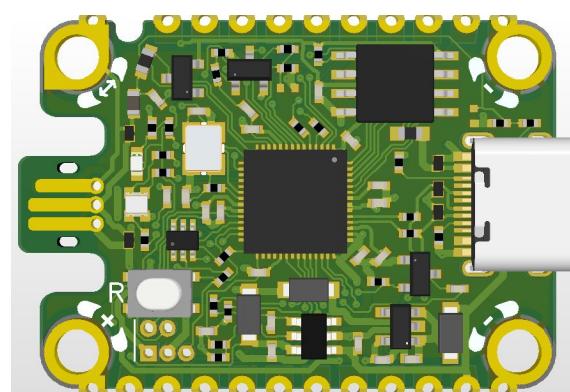
Top Assy

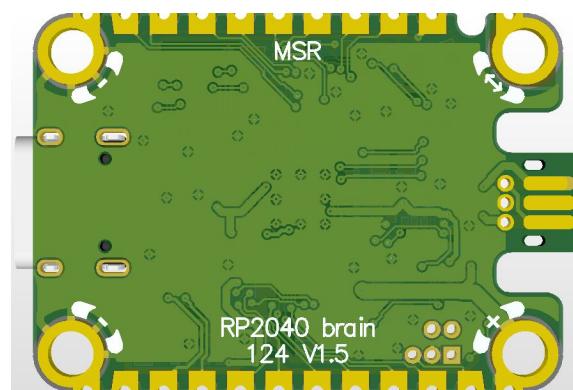


Board Outline

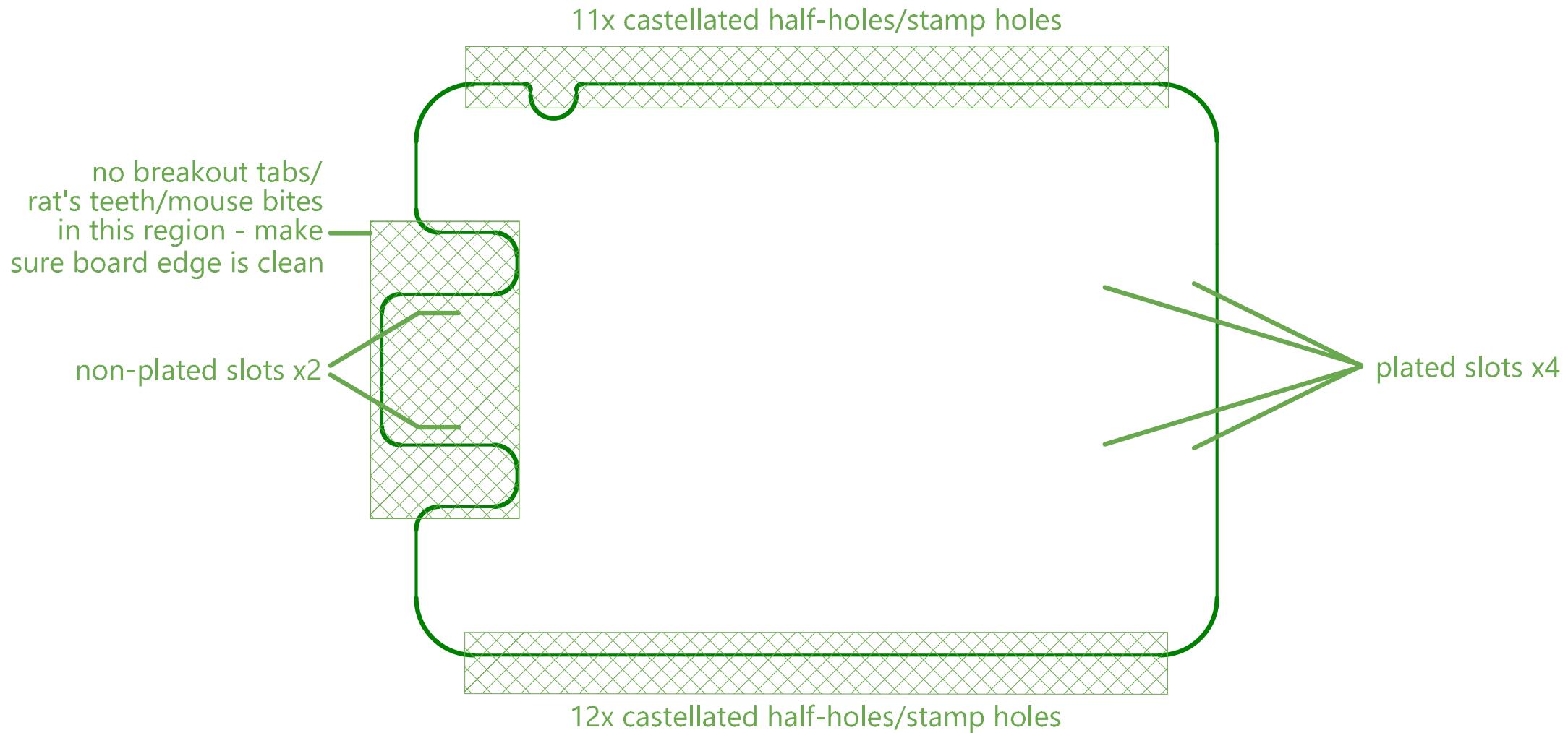
Bottom Assy





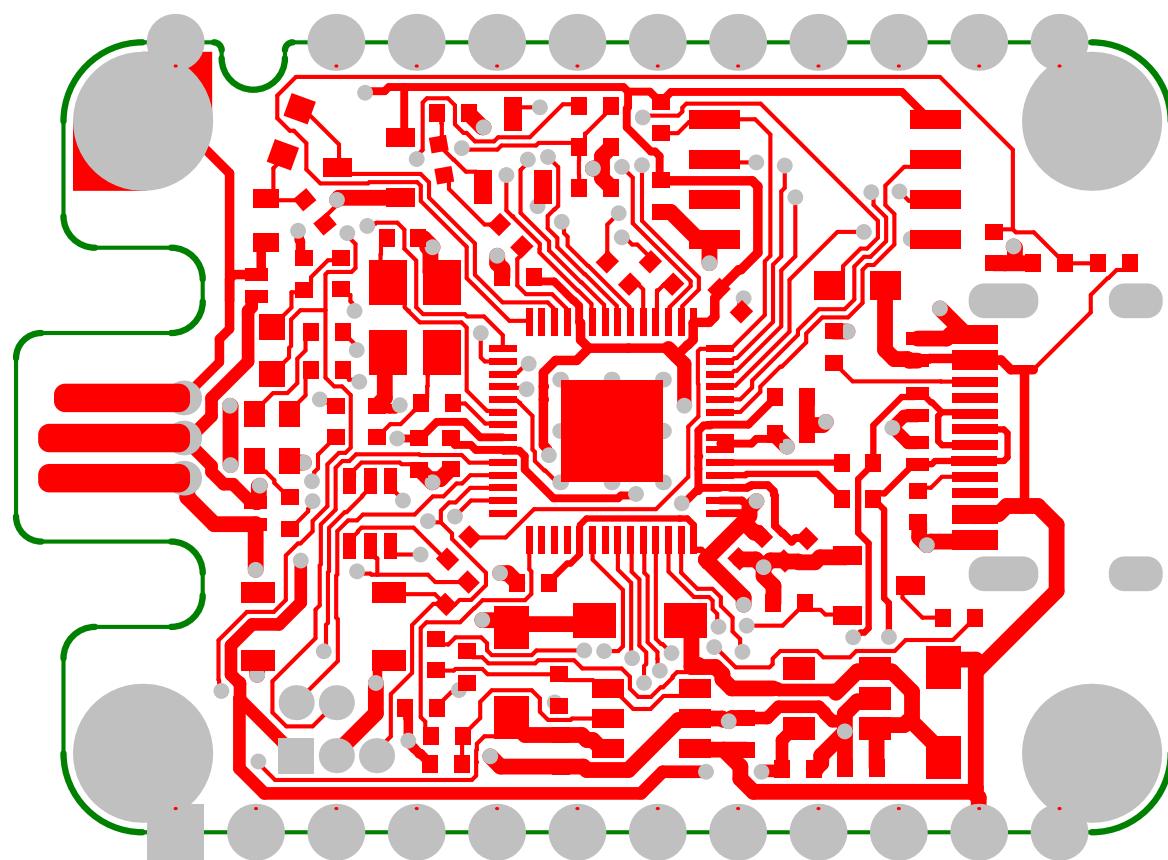


Fabrication Notes
Board Outline



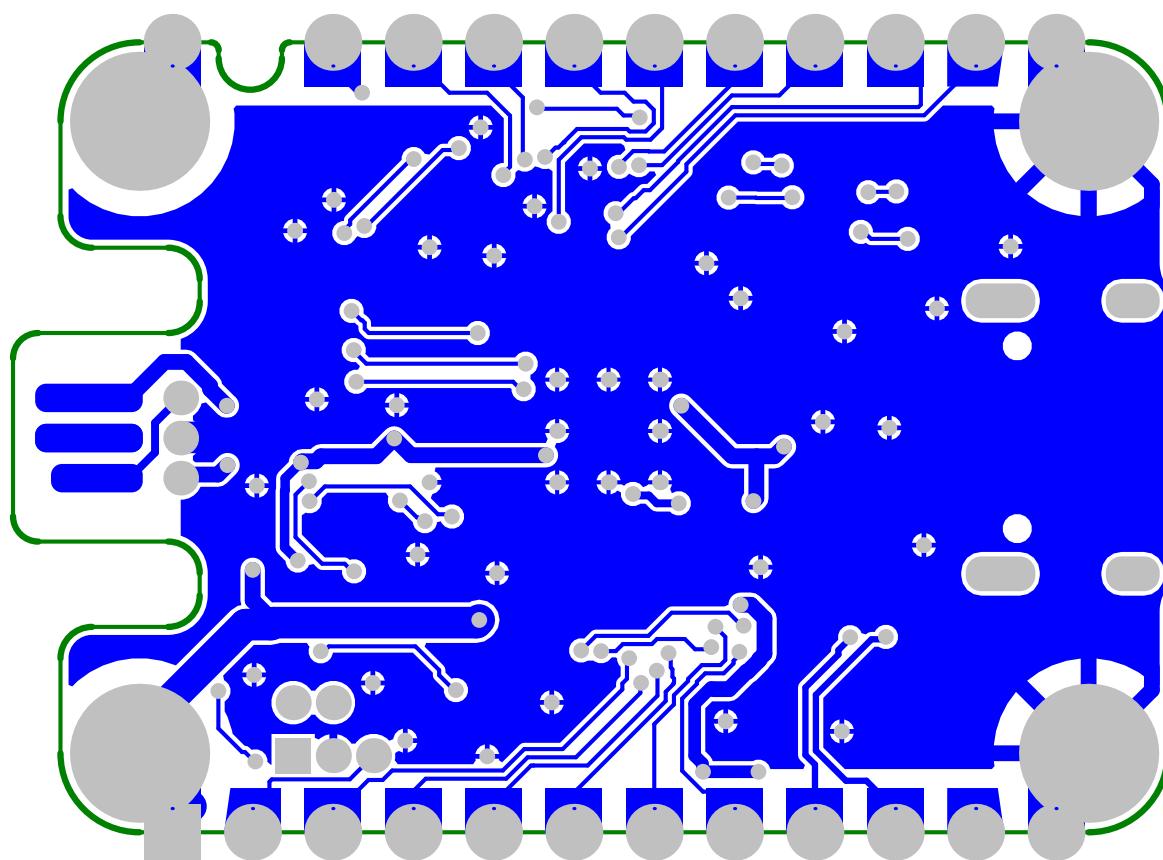
Top Layer

Board Outline

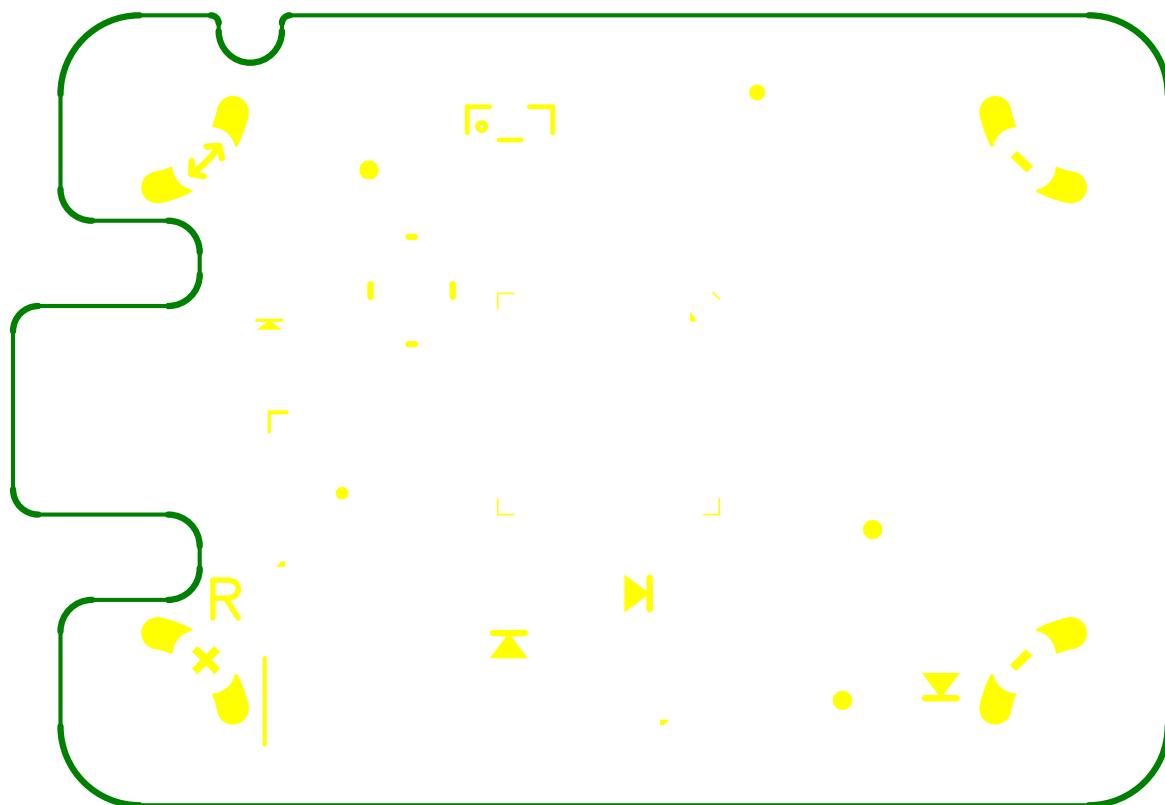


Bottom Layer

Board Outline

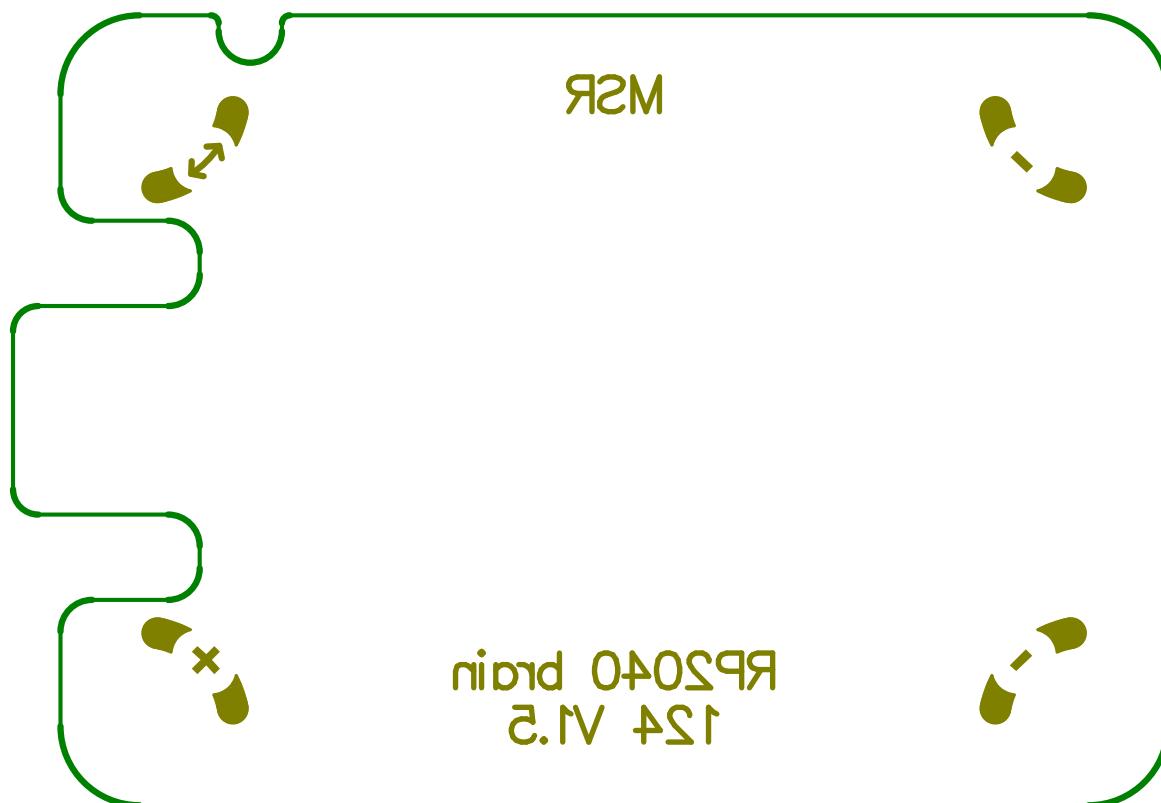


Board Outline



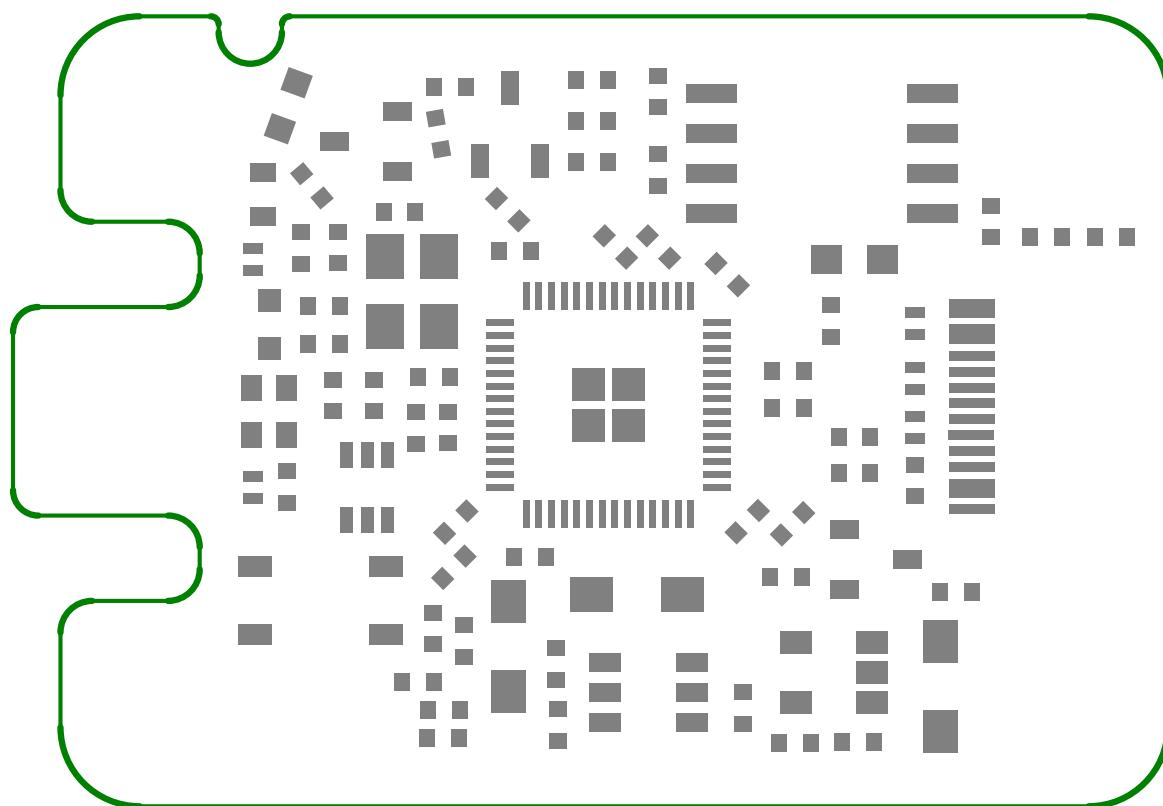
Bottom Overlay

Board Outline



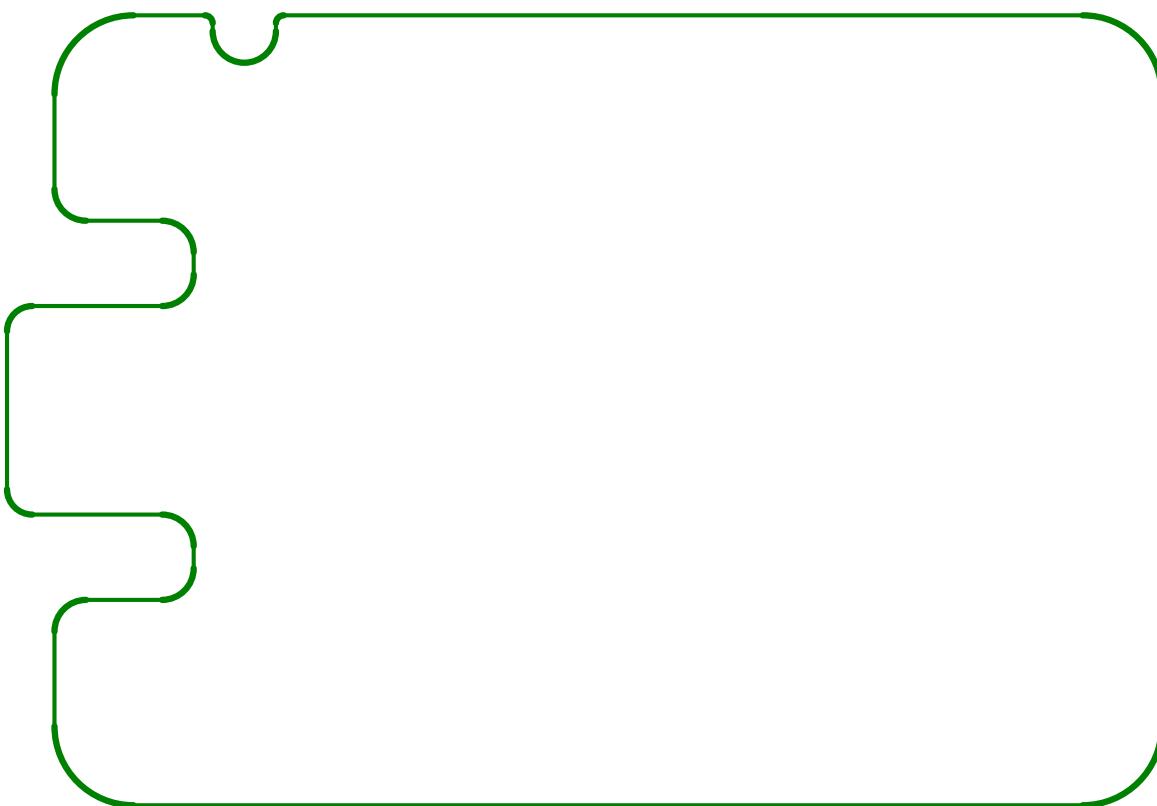
Top Paste

Board Outline



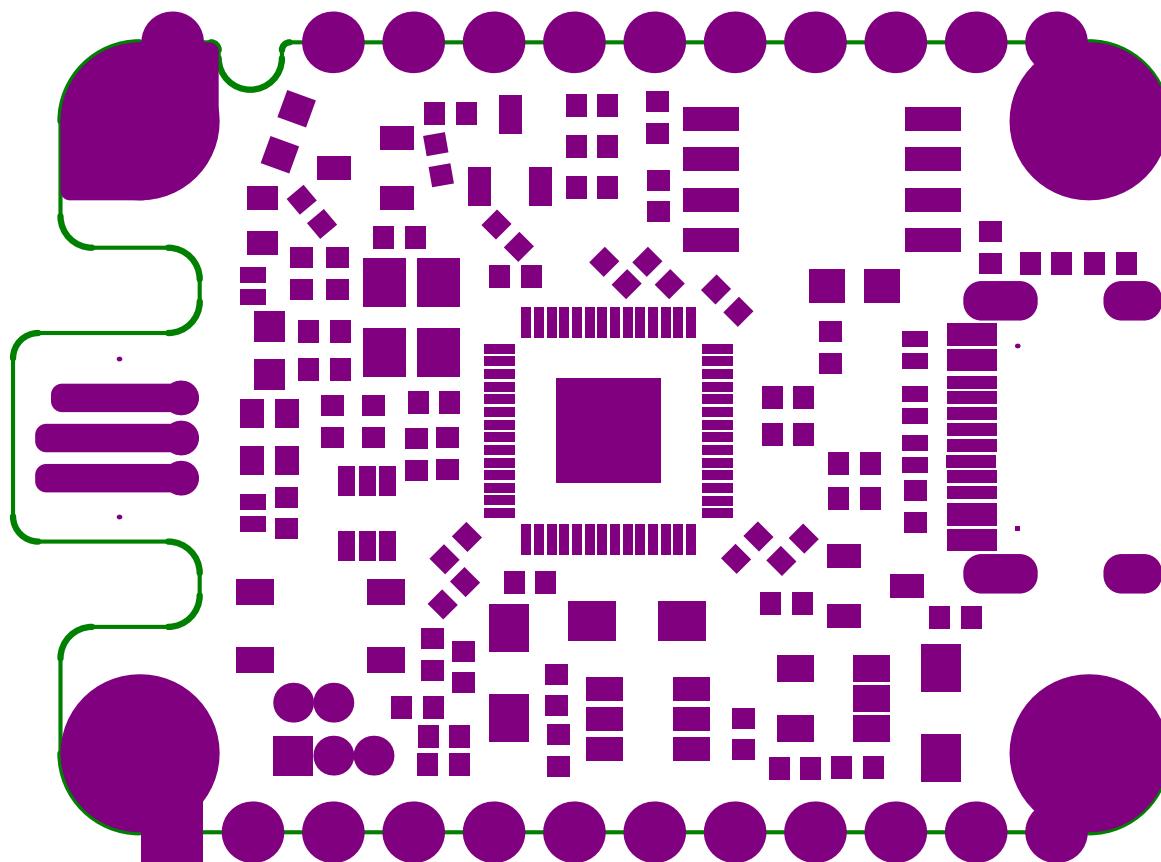
Board Outline

Bottom Paste



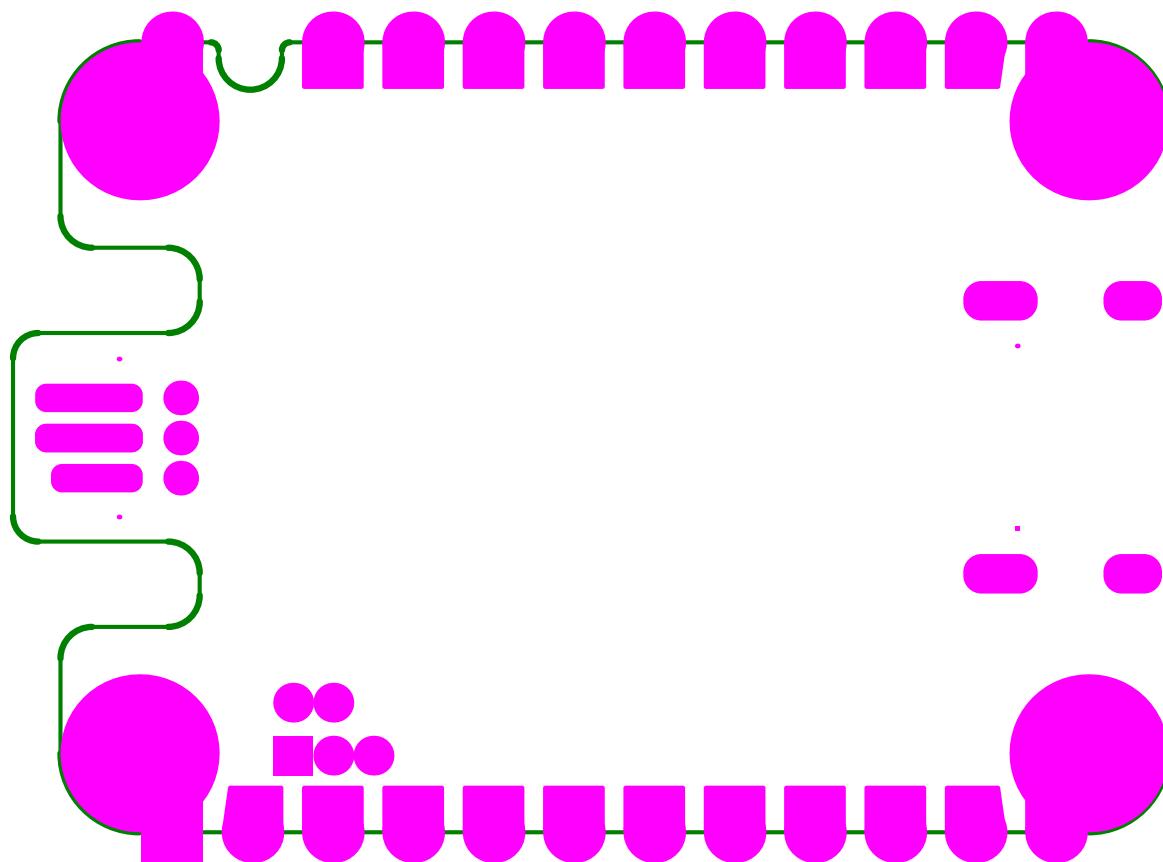
Board Outline

Top Solder (resist)



Board Outline

Bottom Solder (resist)



Board Outline

Drill Drawing

