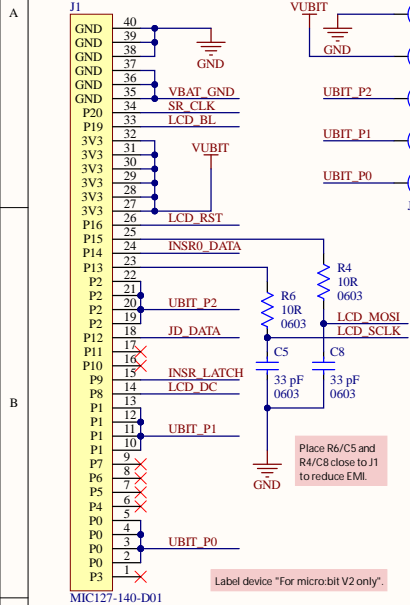
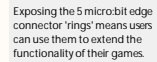


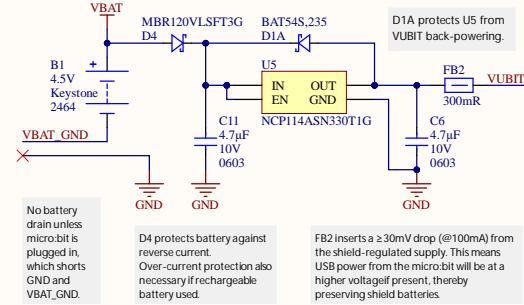
micro:bit connections

190 mA max current draw from micro:bit V2.



On-shield battery supply

Shield display needs 3.3V to operate reliably. If the micro:bit is USB-powered, 3.3V from the edge connector is used. Otherwise, 3x on-board AA cells provide 3.3V for the shield via U5. If the micro:bit is battery powered and the 3x on-shield AA cells provide less than 3.0V, shield operation is unreliable.



Hardware configuration

			HW_CFG0	Display rotation
			0	Rotated 180 degrees.
			1	Not rotated.
HW_CFG3	HW_CFG2	HW_CFG1	Hardware configuration	
0	0	0	Reserved, do not use.	
0	0	1	577735 (CFG1=0x603 or =0x12cd).	
0	1	0	IU9163C with BGR color order (CFG1=0xe14ff).	
0	1	1	577735 inverted color palette (CFG1 as above, CFG0 = 0x1??????).	
1	0	0	Future configuration.	
1	0	1	Future configuration.	
1	1	0	Future configuration.	
1	1	1	Reserved, do not use.	

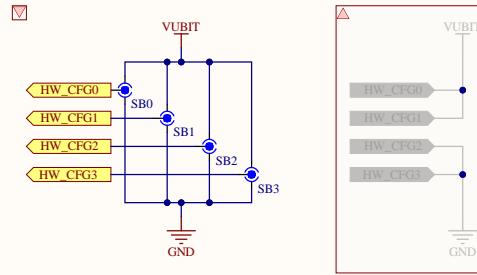
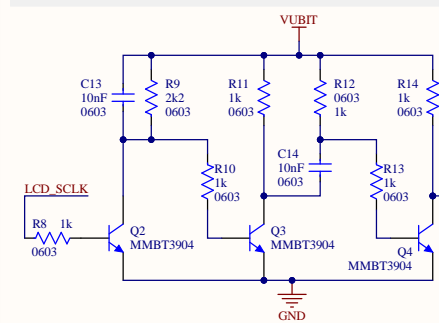
Inputs E-H of U2 (HW_CFG0 - HW_CFG3) are read at power-on to specify Arcade shield hardware configuration. Connect according to these tables.

This reference design uses un-rotated JD-T18003 display with ST7735 controller so HW_CFG0/1 = 1 and HW_CFG2/3 = 0.

If you would like to propose a new configuration please email: arcadehdw@microsoft.com.

Dynamic display enable generator

Kitronik Ltd found that an ESD event can cause the display to freeze if CS is permanently held low, but that the display recovers if CS is periodically taken high. This circuit kindly contributed by Kitronik generates the displayCS signal dynamically based on the SPI clock - It briefly disables communications with the display at the end of each frame of SPI data. Please consider the use of an approach like this to increase robustness of operation.

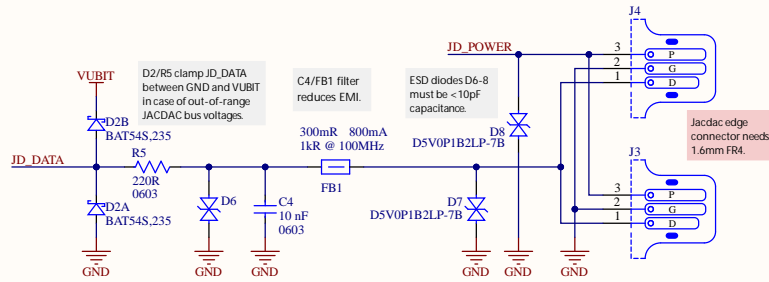


Jacdac interface

Optionally include 1 or more Jaccad connectors. Power delivery optional.

Jacdac (<https://aka.ms/jacdac>) is a "plug and play" protocol for connecting microcontrollers and peripherals. Its flexible topology, dynamic discovery and power delivery provide a great user experience for makers and students.

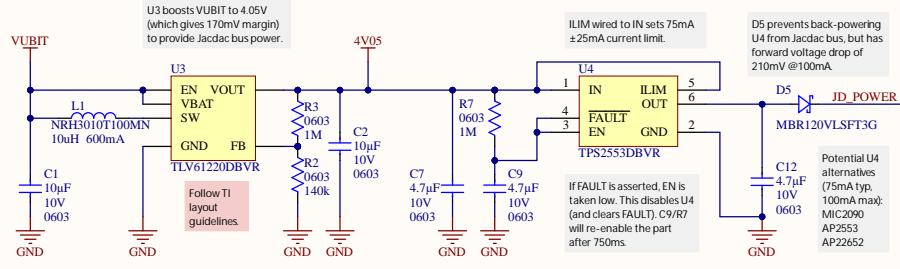
Jaccad provides 1Mbps communications and power delivery. JD_DATA uses 3.3V logic, JD_POWER is nominally 5V.



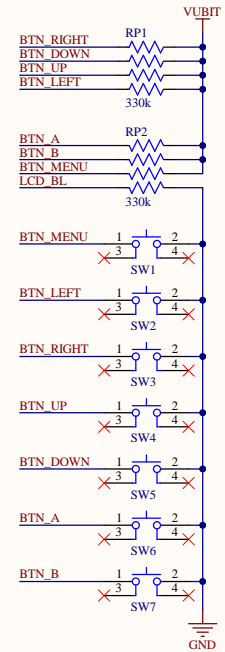
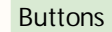
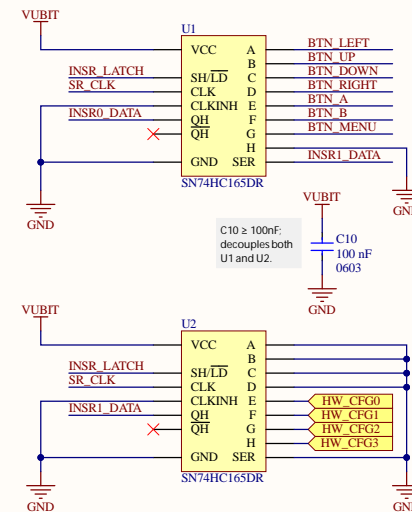
Jacdac power delivery is optional. Spec requires current limiting with auto retry, and that nothing gets hot! This shield delivers 75mA typical, 100mA max.

A Jacdac supply of up to 100mA must be $\geq 3.67V$ at the connector, i.e. U3 output $\geq 3.88V$. 100mA max requires 145mA from 3.3V VUBIT supply. LCD1 takes 45mA to give 190mA total

Check Jacdac spec for voltages required at higher currents and MCU-based 'smart power providers'.



Input shift registers



Key:	Silkscreen & layout notes
	Block name
	Design notes

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When this PDF is viewed with Adobe Reader, clicking on components shows part numbers and other details.